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A Shift-left Methodology for an Early Power Closure Using EDCs and Power Analysis

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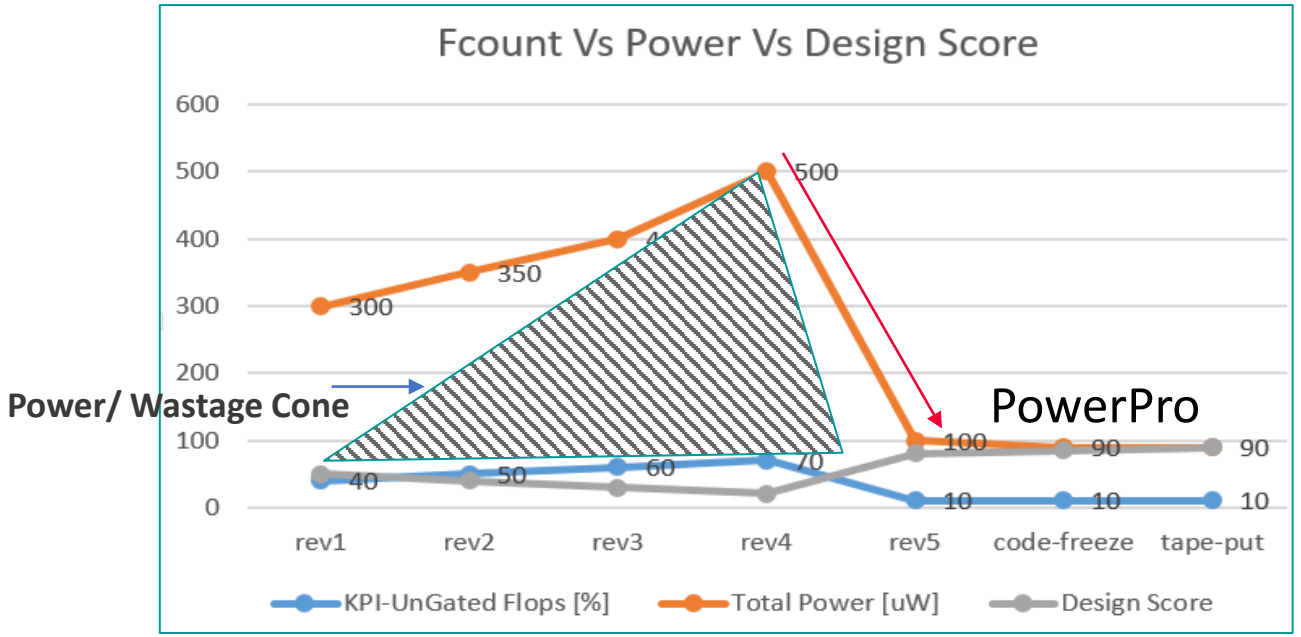
Problem Statement: Current Use Model

The Problem with Addressing Power Late

- Leaving Power to the last minute is not advisable
- Scope for optimization is more during early RTL

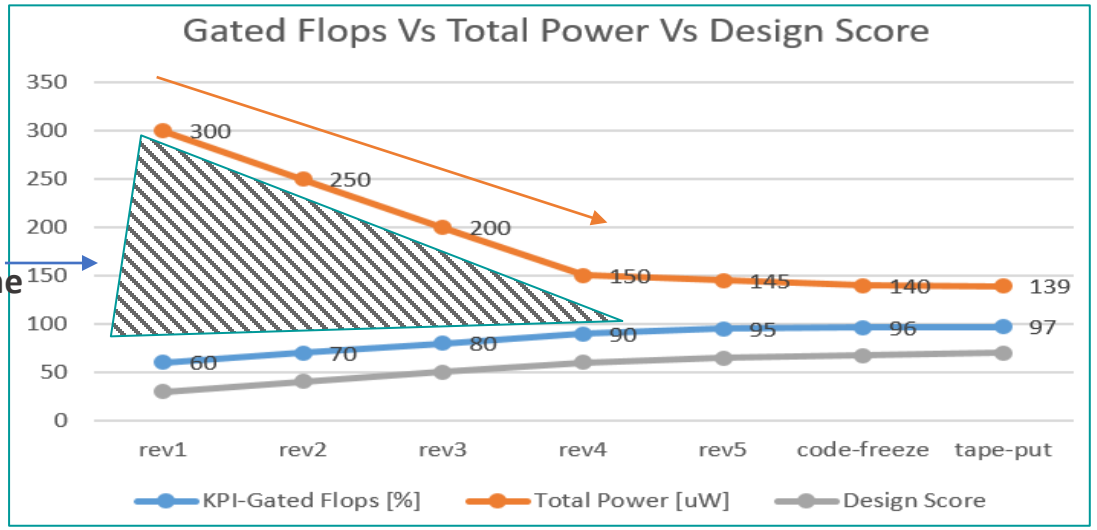


Recommended Use Model: Shift Power Attention Left

Address Power Early – Move it left for more impact

- EDC and iterative Power Analysis help reduce power linearly with incremental revisior of the RTL
- It helps addressing the power early on for more impact on reducing power
- A Methodology that is regression ready

Power/ Wastage Cone



The Challenges

The Challenges Associated with RTL Power Flow

Difficult Tool Setup

- Provide inputs like waveform, physical information etc
- Calibration for Power Estimation

Power Analysis and Large TAT

- May require deeper analysis of reports to understand the problems and fix them, often late in the design cycle

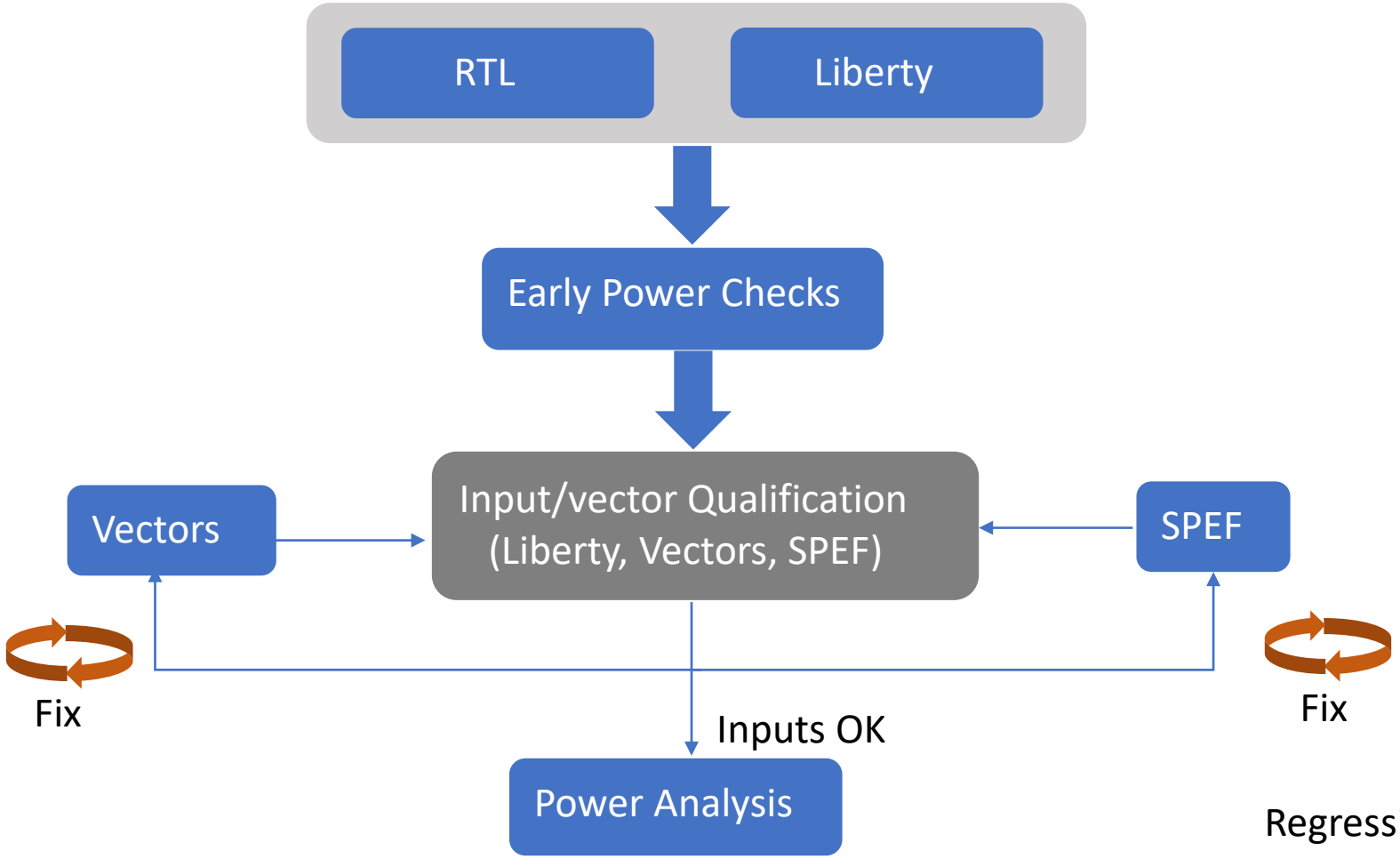
Late Consideration of Power

- Lack of time to find and fix power issues
- Discovering problems late will delay schedules

The Essential Ingredients of the Required Methodology

The Solution: The Proposed *shift-left* Methodology

Methodology Using EDCs and Power Analysis

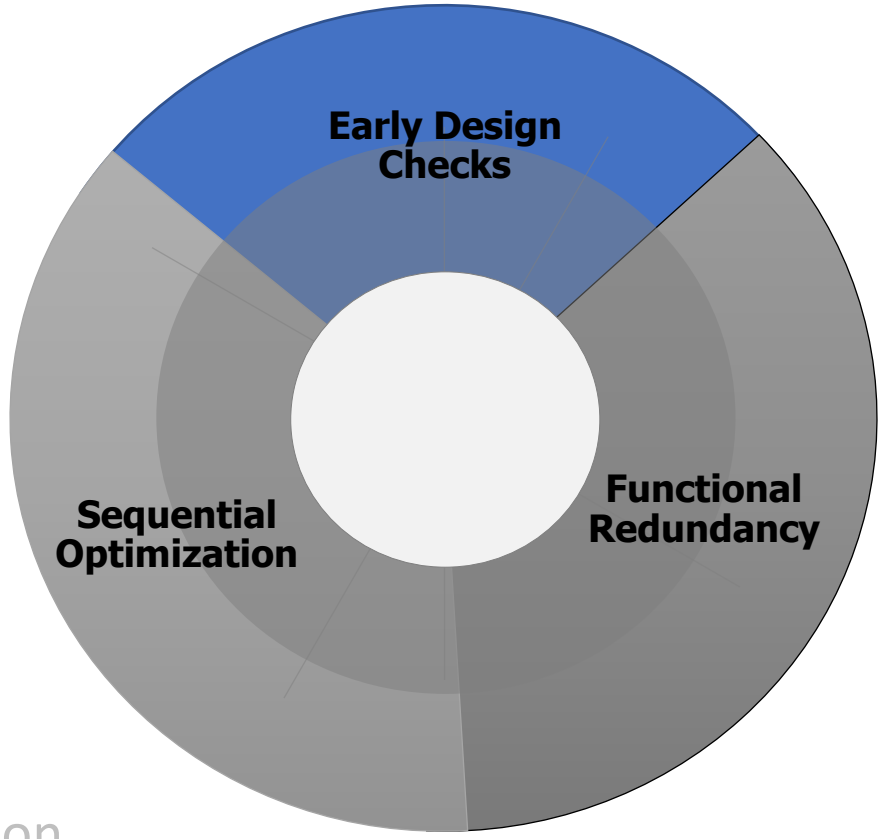


Regression Ready Framework

The Solution: PowerPro Power Optimization Guidance

PowerPro offers a wide variety of Power Optimization Techniques

- Early Design Checks
  - Static Checks
  - No Activity File required
  - Power Linting and Gating Coverage Checks
- Functional Redundancies
  - Micro-architectural and Combinational Redundancies
  - Waveform mining to find Redundant Toggles in the design
  - Leads to opportunities that would allow user to find gating candidates
- Sequential Optimization
  - Based on Sequential Analysis
  - Complete enable expression visualization for implementation



Early Design Checks

Structural Analysis of RTL to reveal power issues upfront

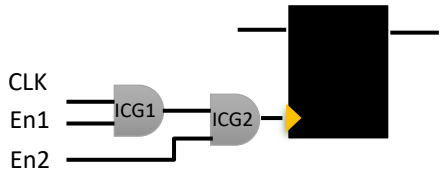
- Can be run without vectors
- Runs extremely fast
- Performs structural analysis of the RTL to find potential issues that can impact power downstream
- EDC metrics can be used to qualify IPs for lowpower

Early Design Checks		
Ungated Memories	9	81.82 %
Ungated Macros	1	50 %
Ungated Memory Inputs	49 Input(s)	100 %
Ungated Operator Inputs	8 Input(s)	
Ungated Flops	613	59.8 %
Ungated MUX Inputs	9 MUX Inputs	
Not Combinationally Enabled Flops	728	71.02 %
Floating Memory Data Outputs	1 Output(s)	0.09 %
Memory Redundant Toggle Inputs	11 Input(s)	73.33 %
Constant CGICs	3	17.65 %
Functionally Redundant CGICs	4	23.53 %
Structurally Redundant CGICs	2	11.76 %

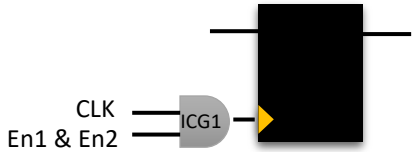
Early Design Checks

Structurally Redundant ICGs example

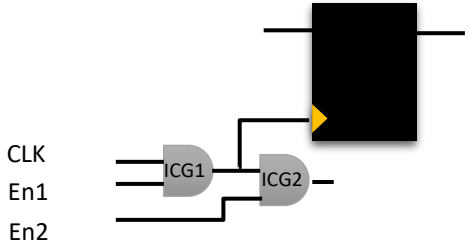
(1) ICG1 does not drive FF directly



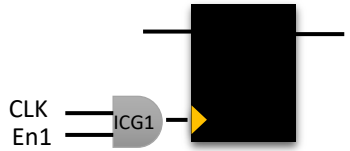
(1`) Merge two ICGs into one



(2) ICG2 gated clock output is floating



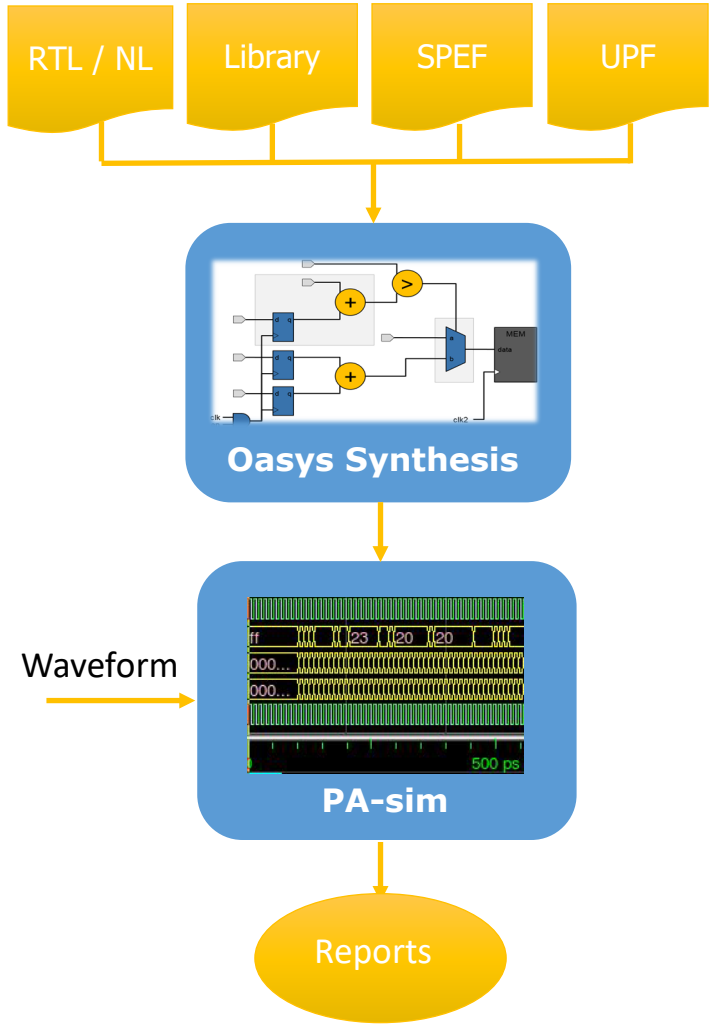
(2`) Remove ICG2



Power Analysis

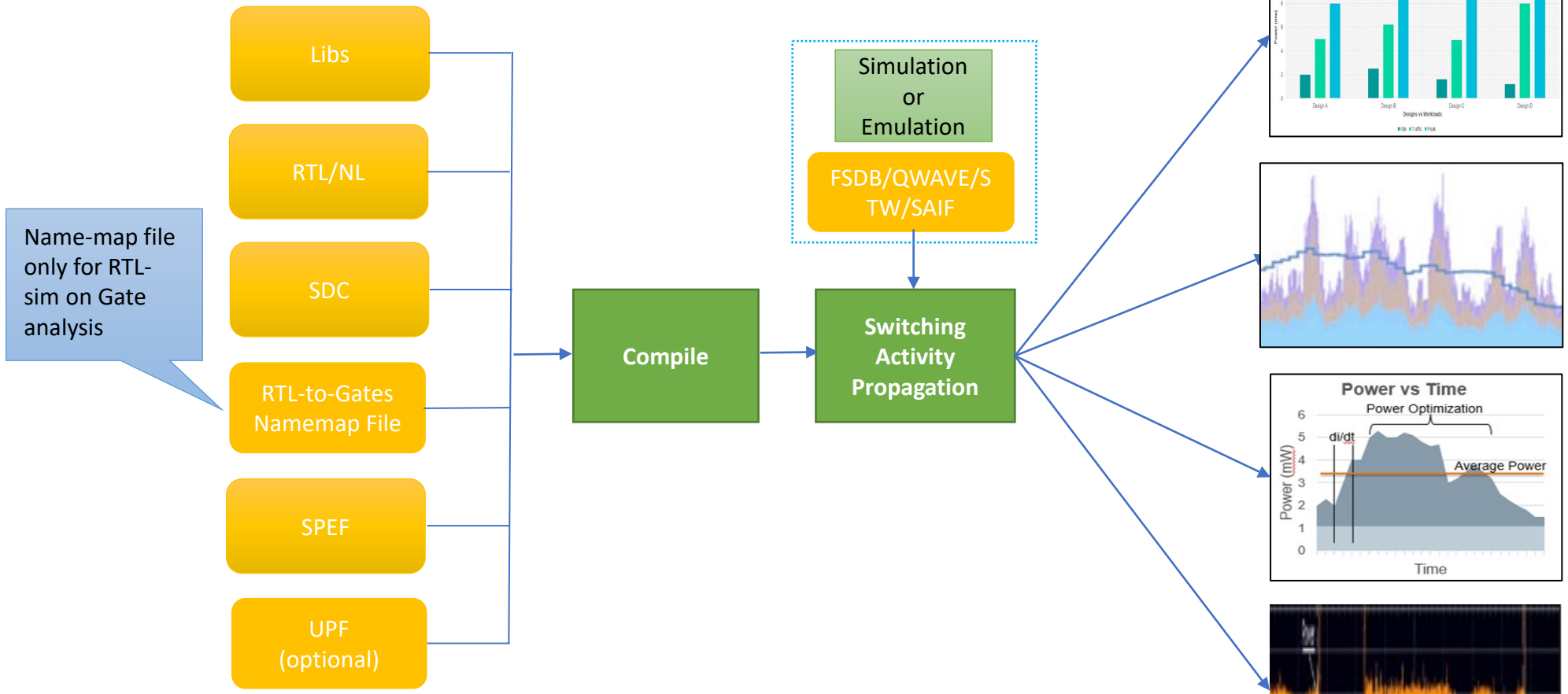
Complete portfolio for Power Analysis, from early RTL to Gate, IP to SoC

- Accurate RTL and Gate-level Power Estimation
  - RTL Power Accuracy within 15% of layout
  - Gate Power Accuracy within 3% of layout
  - Ability to use RTL stimuli to perform Gate-level Power Analysis
- Averaged Power and Time-based Power
  - Averaged Power
  - Time-based Power (Cycle-Accurate)
  - Supported switching activity formats: QWAVE, FSDB, SAIF, STW
- Detailed Reports and Intuitive Debug
  - Summary Power, Hierarchical Power
  - Power by Component/Category
  - Power by Clock Domain
  - Intuitive GUI with cross-probing, querying, filtering etc



Averaged and Time-based Power Analysis

RTL, Gate and RTL-stimulus-on-Gate



Averaged Power/Energy Reports by Summary/Hierarchy

Time-based activity plot

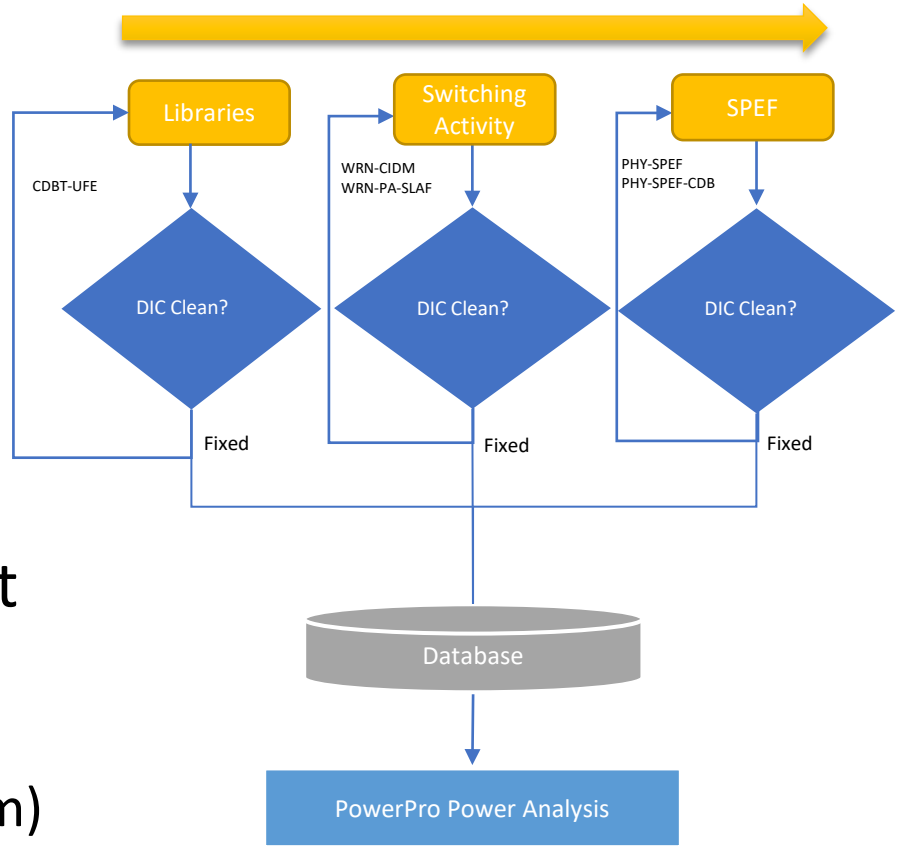
Time-based Power Plot and Reports

Power Waveform for IR-drop analysis

Power Setup and Input Quality Check

Ensure first-time right power estimates with data integrity checking

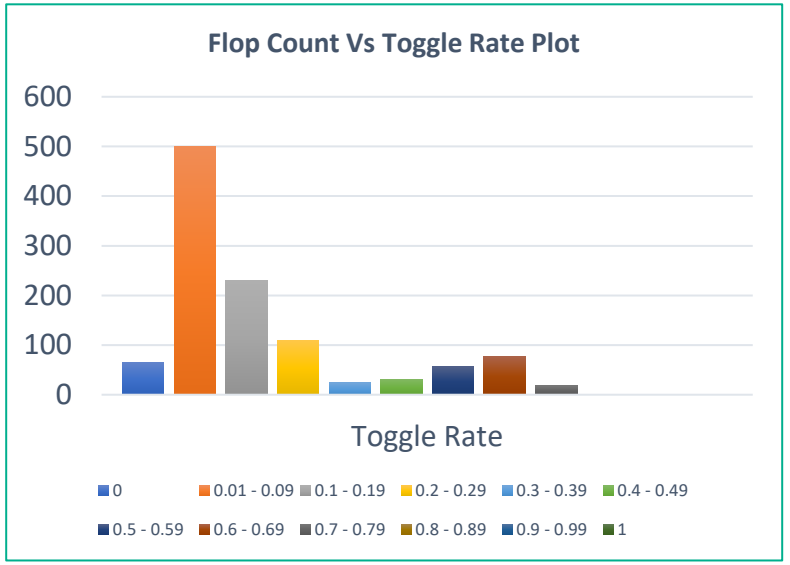
- Correct setup leads to correct power estimates !
  - Incorrect setup and deficient inputs can lead wrong power estimates, longer TAT
- Did I provide the correct setup?
  - Setup can be wrong unintentionally, leading to incorrect power numbers
- Quality of input determines the quality of output
  - Data integrity checks (DICs) ensure that the input provided is not deficient
  - Quality checks at each step (Libraries, SPEF, Waveform)



Power Coverage for Stimulus Qualification

Averaged Toggle Profile and Power Coverage Metrics

- Evaluate power coverage of your vectors
  - All portions of the design must be stressed by given vectors
  - Multiple waveforms stressing same portions of the design with similar toggle profile could be redundant, hence discarded
- Qualify workloads for power
  - Find instances that are always toggling or not toggling at all
  - Establish toggle correlation of the clock with design signals
  - Helpful in catching anomalies in use case



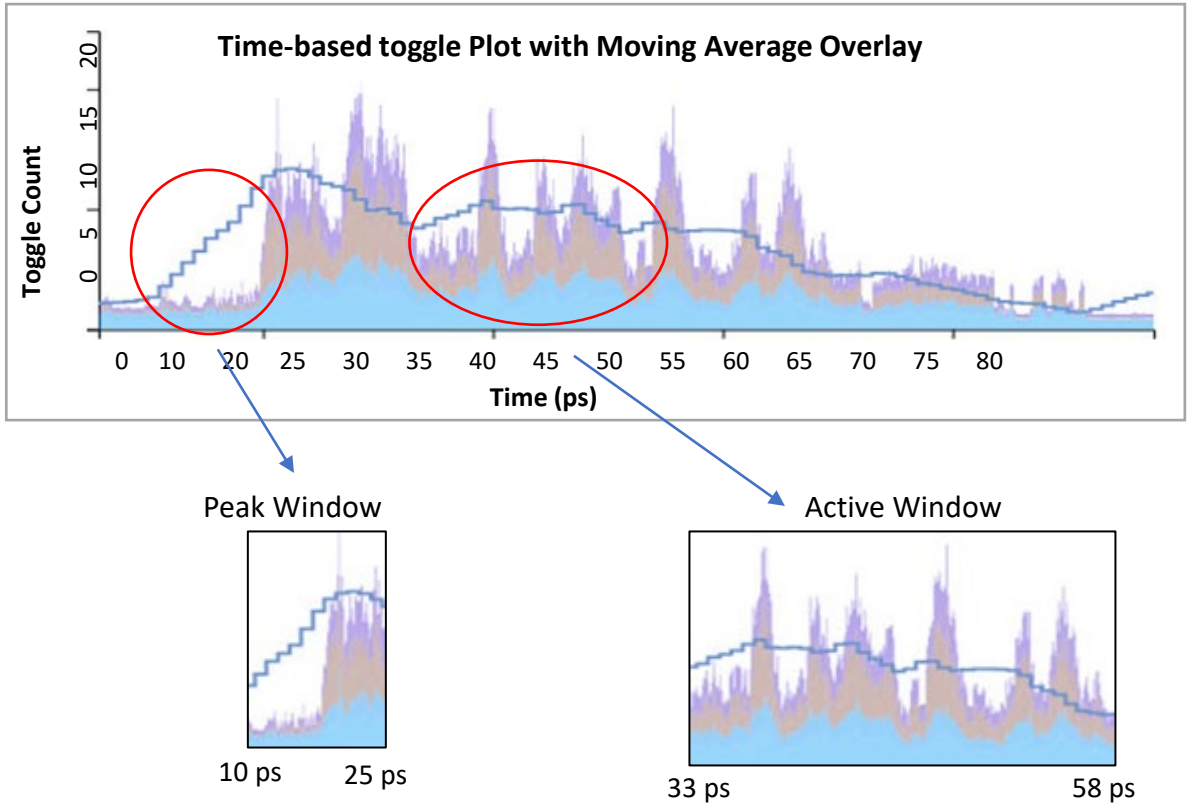
Section-3b: Dead Instances-Clock blocked {top: pci, Total Flops: 790486}	
Clock pin of following instances is not toggling.	
1	ucpu1
2	ucpu1.uif
3	ucpu1.uct1
4	rxmod_u1
5	rxmod_u1.u2

?

Activity Profiling to find Regions-of-Interest

Time-based Toggle Activity Profile

- Identify regions of interest
  - Categorize windows as Idle, Active and Peak scenarios
  - Cut-out windows of interest
- Use for downstream analysis
  - Multi-CPU support enables time-based toggle profiling for billions of cycles (Cycle Accurate profile)
  - Run power analysis and optimization faster by reducing analysis window to millions of cycles from billions



Complete solution for Low-power

From early RTL to System-level Power

Input/Vector Qualification

- Correctness of Inputs (Structural + Functional Issues)
- Toggle Profiling (Mode Qualification, RoI Identification)

Early Power Checking

- Structural Checks
- Functional Checks

Power Analysis

- RTL/Gate Averaged Power
- RTL/Gate Time-based Power
- RTL Stimuli for Gate
- RTL/Gate Glitch Power *

Power Optimization

- Clock Gating
- Memory Gating
- Data Gating

Conclusion and Summary

- Early RTL can be analyzed for Power to determine if IP is good in terms of power or not
- Fast analysis with minimal setup means it can be automated and integrated with regression
- Static and Dynamic checking can quickly point to power issues upfront
- Can be easily adopted by CAD teams for low-power IP qualification

Questions