A Unified Framework for Multilanguage Verification IPs Integration

Surinder Sood, Selvakumar Krishnamoorthy, Gaurav Jalan
SmartPlay Technologies

Introduction
UVM-ML framework combines multi-language IP and make them work together for any verification task. The basic ML setup is as shown below:

Objectives
Deploying ML framework to achieve –
• Reuse existing verification IPs irrespective of IVL used for representation
• Enabling faster bring-up of SoC testbench
• More focus on verification than testbench development at SoC level
• Optimized code with proven verification IPs
• Minimize verification environment bugs
• Faster time to market

Framework to support –
• Heterogeneous Objection Mechanism
• Configuration mechanism across multiple eVCs and UVCs
• Reuse of existing sequences, assertions, coverage and scoreboard

The Setup
Example demonstrating 2 × 1 IP integration: 1 UVC and 2 eVC

SV TOP

generating 2 + 1 IP integration: 1 UVC and 2 eVC

Configuration Mechanism: eVC to UVC and Vice Versa
The Heterogeneous configuration mechanism

Objection Mechanism
UVC – UVM test raises objection in run phase

eVC – Objection Dropped?

Drop UVM-SV test Object in run phase

UVML Framework

eVC

Connect to a top level signal using an Out Port

Specimen test finished

Assert the Out Port on TEST_DONE (e− Objection dropped)

Conclusions
UVML framework helps in achieving –
1. SV based Virtual sequencer to control the multi-eVC sequences
2. Phase propagation across frameworks, e.g. build phase from UVC to underlying eVC
3. Configuration of the eVC from UVM-SV environment both statically and dynamically
4. Phase Synchronization
5. Graceful termination of tests from top-level

Proposed future work –
1. Enhanced Debugging and tracing capabilities
2. Messaging service mechanism at ML level
3. Propagating Errors to the underlying slaves (eVC in this case)
4. A global objection mechanism

References:

© Accelleras Systems Initiative