A NOVEL APPROACH TO REDUCE POWER CONSUMPTION BY BRIDGING THE GAP BETWEEN STANDALONE FUNCTIONAL SCENARIO AND REAL TIME SCENARIO AT SOC

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Introduction

A systematic approach is inculcated to target an efficient and smooth verification flow for low-power simulations for large SOCs.

Analysis of power/voltage/clock domains ➔ Defining verification scope

One time compile ➔ Loading the power information of design

PMIC controller ➔ Mimic the behavior in the test bench

Power operations isolation, level shifters, retention ➔ Checkers to reinforce DV

The fine tuning techniques deployed based on the new verification approach resulted in saving up to 30% power consumption on silicon. The fully configured and powered on module consumed ~41mW (18% less) against the planned 50mW, idling power with power rail on consumption 8.44mW → 5.86mW (30.6%) and the power gated block with minimal functionality to the block was found to consume only 0.58mW against planned 0.65mW (11%).

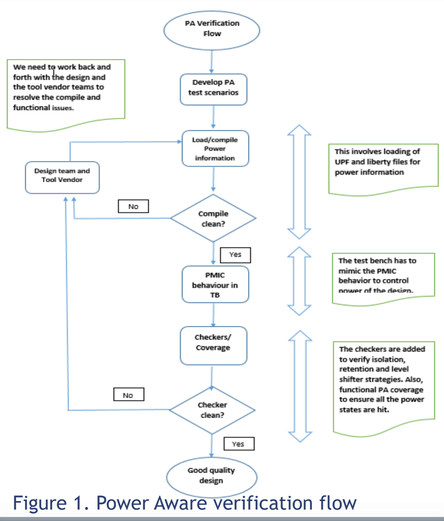

Figure 1. Power Aware verification flow

Proposed Methodology

- SOC consisted of 75 power domains, 79 clock domains and 37 voltage domains
- The SOC consisted of 13 power manager IPs which deployed various low power techniques:
  - Variable voltage level for logic/memories/hard macros ➔ Operating from 0.6V to 3.3V.
  - Switchable power supplies ➔ Power gating using standard library power switch cells.
  - Clock shut off ➔ Clock gating when PD is idle.
  - Isolation cells ➔ Avoid leakage to nearby PDs.
  - Level shifters ➔ Sampling signals that cross voltage levels.
  - Retention ➔ Data saved during power shut off and restored during power on

Implementation Details

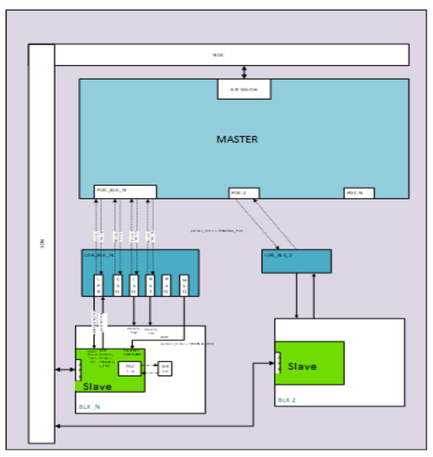

Figure 2. Master Slave Power manager

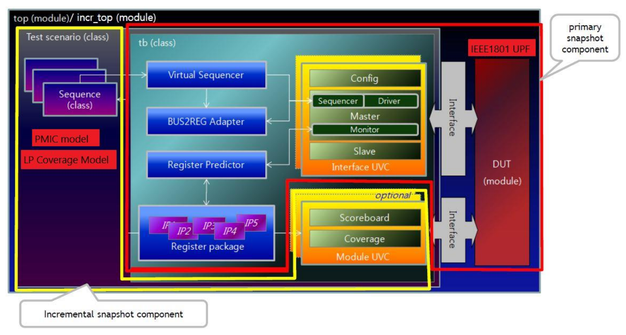

Figure 3. Test Bench structure for Low power simulation

The Master slave power controller handshakes and the basic power domains of the block level power controller and the internal power domains are controlled by the Slave power controller

The slave power controller controls the power domains and decides the power state of each domains in each of the power states. The Slave power controllers have AXI master interfaces which help in clock gearing

Power Domains & Power Down Flow Chart

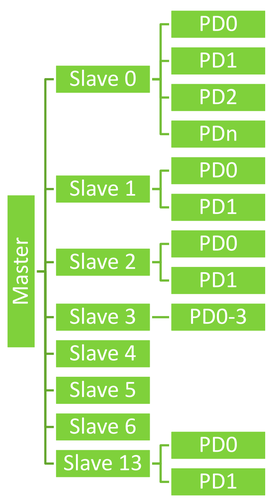

Figure 4. Power Domain distribution and control

Figure 5. Power Down steps

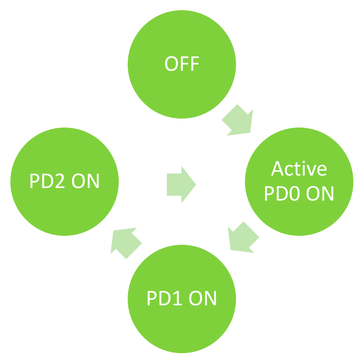

Figure 6. Slave power states

Result

Power Gating(PG)/Clock Gating(CG) from testcase analysis at SOC Level						
		HW Controlled	Software Controlled			
Scenario	Low Power Stages	Master PG	Block PG	MasterCG	IP CG	% Power Saved
A	Level0					0%
B	Level1				Yes	42%
C	Level2		Yes			68%
D	Level3			Yes		52%
E	Level4	Yes	Yes			83%

Table1. Chip level power scenarios and power savings

LEAK POWER	IDLE POWER	POWER GATED IDLE
40mW	5.99mW	0.58mW

Table 2. Power figures at block level

The Software based power down is a slow process as we need multiple writes to multiple registers to achieve the same. The Hardware approach is a permanent process and no of wires increases and so does the fields in registers, this calls for an optimized process of Hardware and software based approach in which we keep a balance of both hardware and software advantages/ disadvantages.

With efforts from architecture and DV sequences we were able to come up with different power states in which the Power is reduced and the wakeup is possible based on need. The power savings constitute to a maximum of 90% for block level idling and around 80% for the chip standby.

The regular SW approaches give only a minimal power reduction of around 40% the major contributor is the power rails turned off. Which here is done by an external FSM based machine which is done by the Test bench.

	Block Level Analysis						
	System Register, NOC	MCU	Camera controller	Image Processor	Display controller	DMA	Power Saving
A	FC, NOP (100Mhz)	FC,NOP (800Mhz)	FC,NOP(800 Mhz)	FC,NOP(800Mhz)	FC,NOP (800Mhz)	FC,NOP (800Mhz)	0%
B	FC, NOP (100Mhz)	FC,NOP (800Mhz)	Clock gearing(100Mhz)	Clock gearing(100Mhz)	Clock gearing(100Mhz)	Clock gearing(100Mhz)	10%
C	FC, NOP (100Mhz)	FC,NOP (800Mhz)	FC,NOP (800Mhz)	FC,NOP (800Mhz)	Clock Gating	FC,NOP (800Mhz)	25%
D	FC, NOP (100Mhz)	FC,NOP (800Mhz)	Clock Gating	Clock gating	Clock Gating	Clock Gating	40%
E	FC, NOP (100Mhz)	Clock Gearing(100Mhz)	Clock Gating	Clock gating	Power Gating	Clock Gating	58%
F	FC, NOP (100Mhz)	FC,NOP (800Mhz)	Power Gating	Power Gating	Power Gating	Power Gating	68%
G	FC, NOP (100Mhz)	Clock Gated	Power Gating	Power Gating	Power Gating	Power Gating	79%
H	Clock Gated	Power Gated	Power Gating	Power Gating	Power Gating	Power Gating	91%

Table 3. Power saving in Block level Power down states/ Scenarios

REFERENCES

- **Harshal Kothari, Eldin Ben Jacob, Sriram Kazhiyur Soundarrajan, Somasunder Kattepura Sreenath, "*Challenges In Power-Aware Verification with Hardware Power Controller and Novel Approach to Harness Xcelium Low-Power Functional Coverage for Complex SoC*", CadenceLive 2021**