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A New Approach to Easily Resolve the Hidden Timing Dangers of False Path Constraints on Clock Domain Crossings

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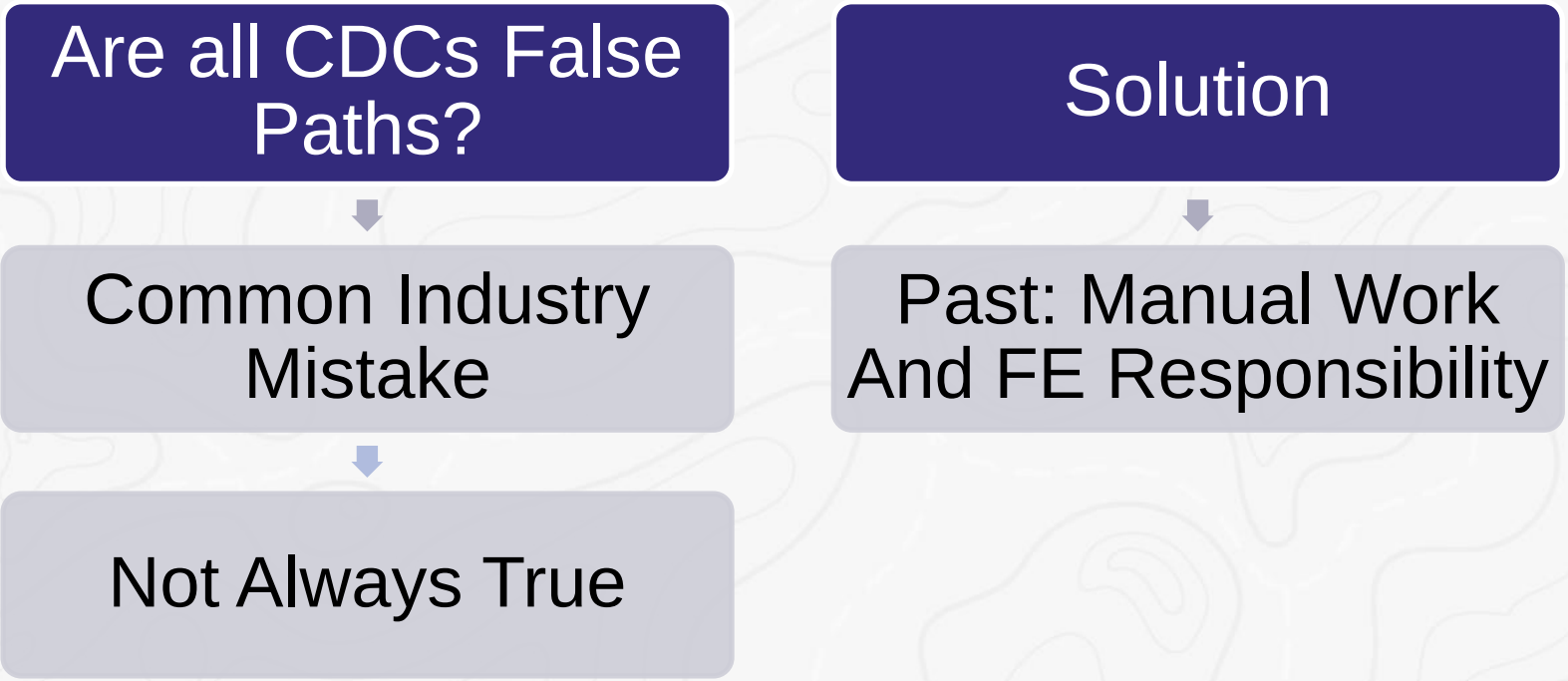
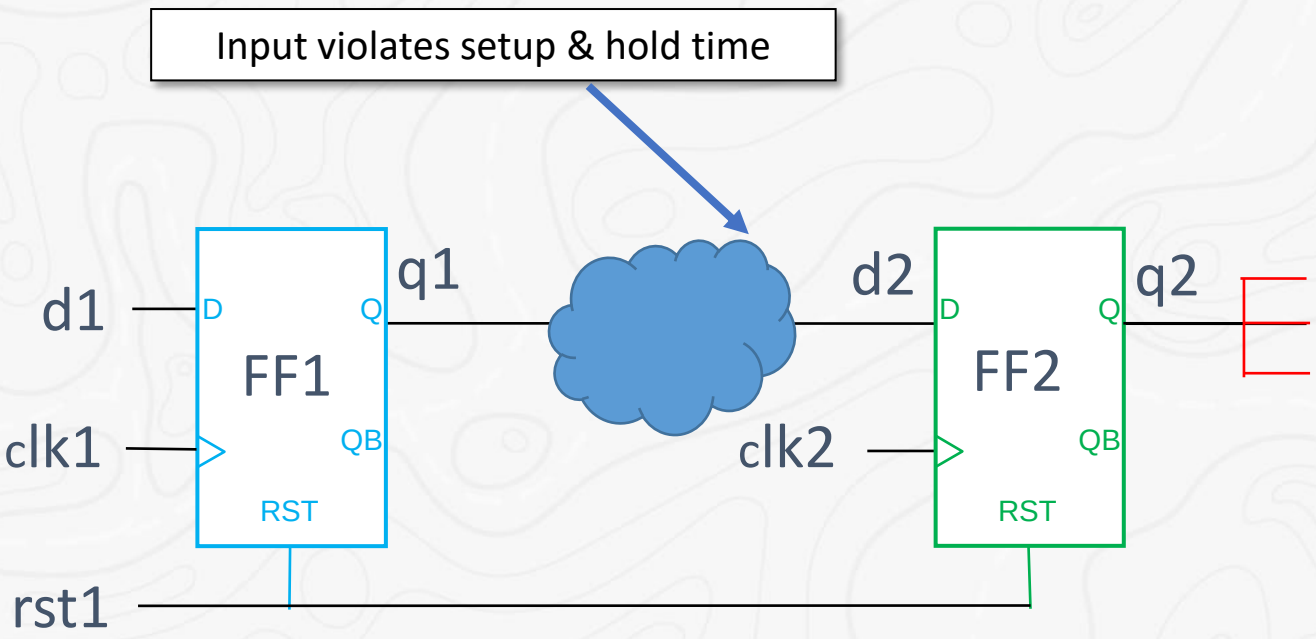
accellera SYSTEMS INITIATIVE

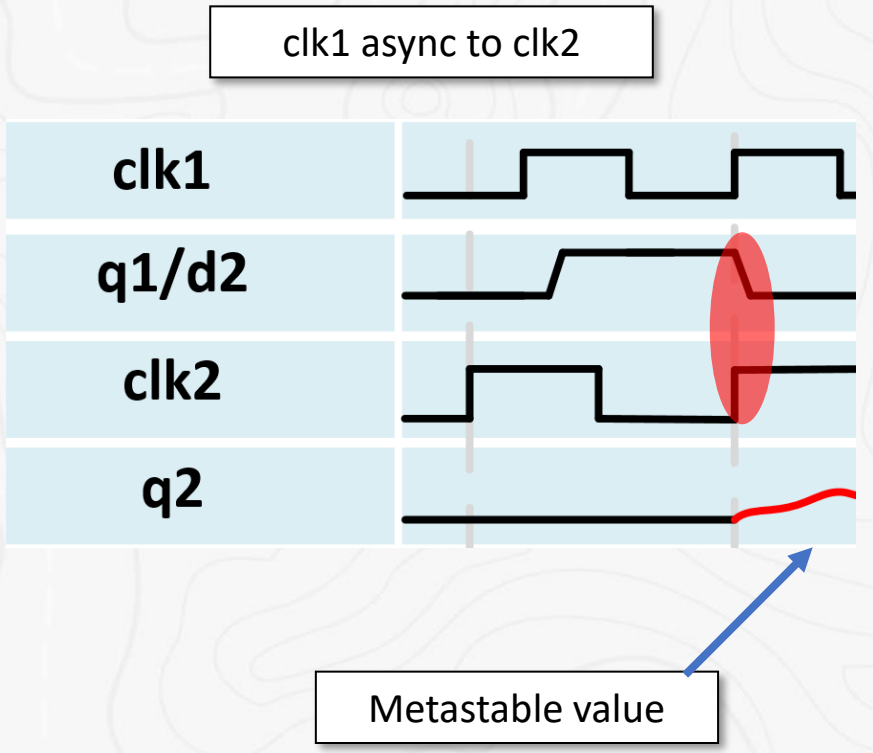
Introduction: CDCs & False Paths



- Agenda
  - CDC Timings Bugs
  - Previous solutions
  - New Solution

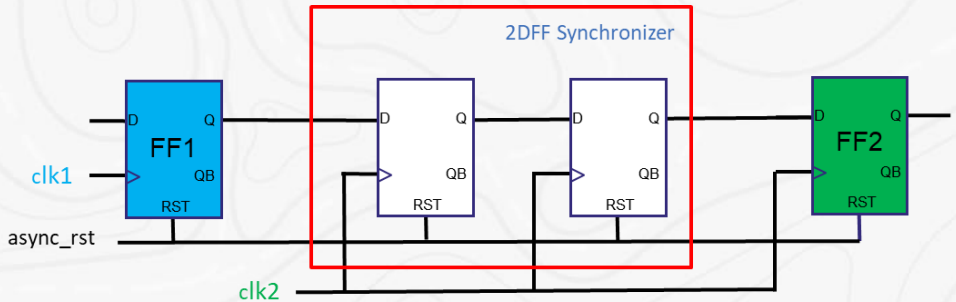
Clock Domain Crossings



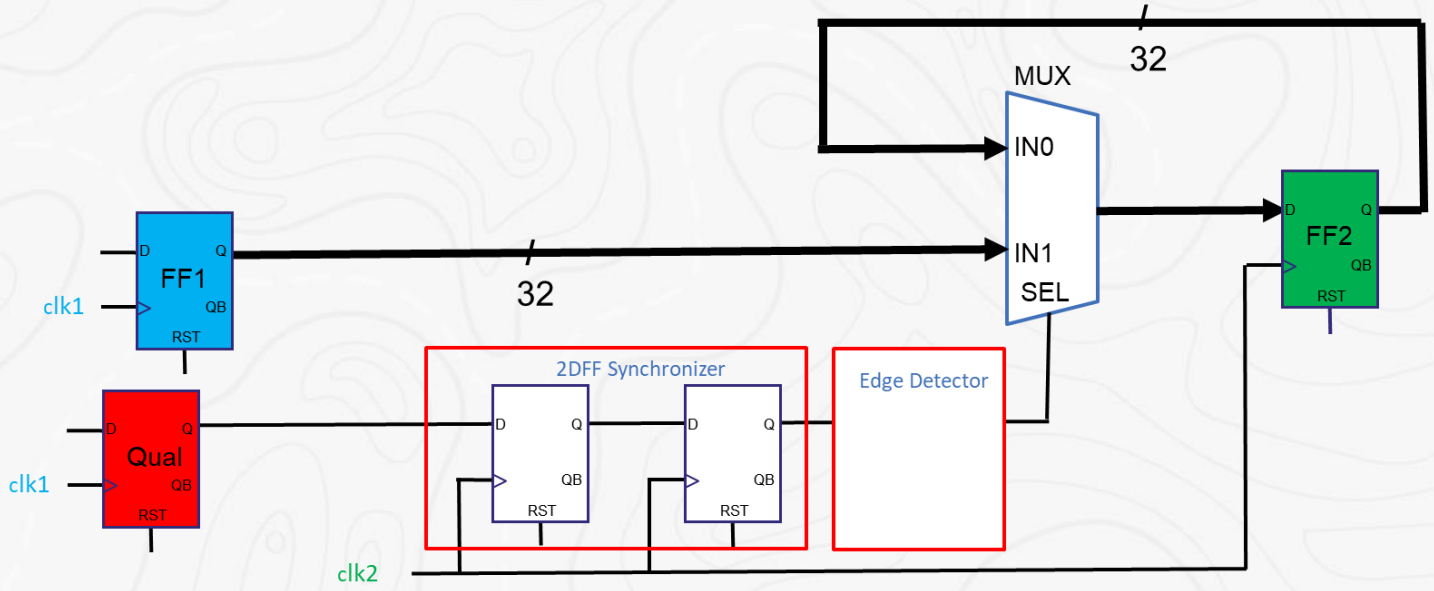


CDC Synchronizers

Simple 1-bit Synchronizer

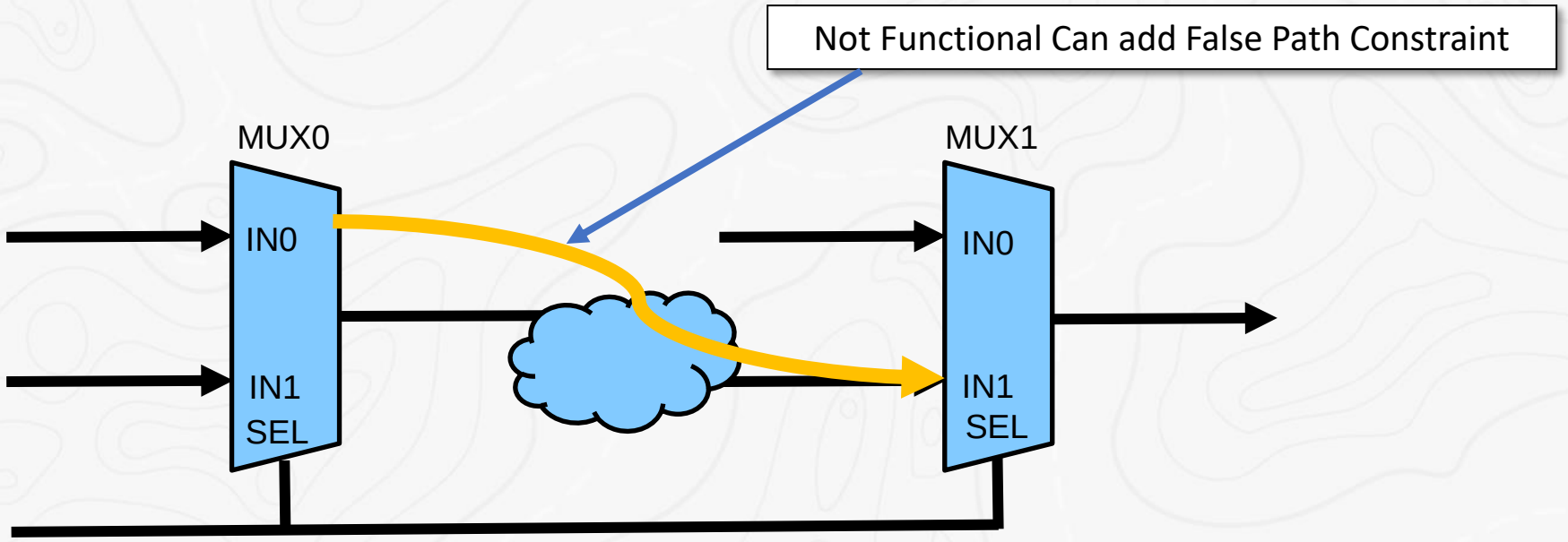


Bus Synchronizer



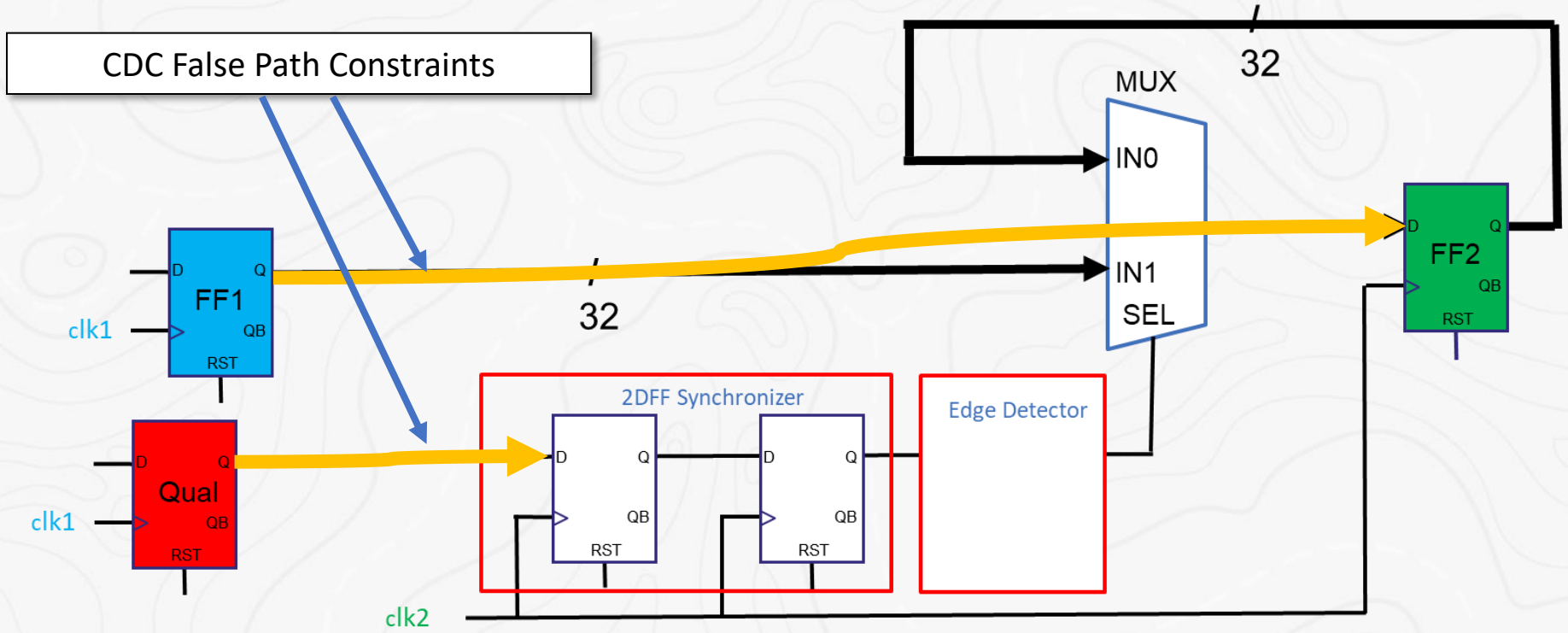
Static Timing Analysis

- Static Timing Analysis (STA) performed on synchronous signals to close setup and hold timing requirements.
- STA takes worst case approach.



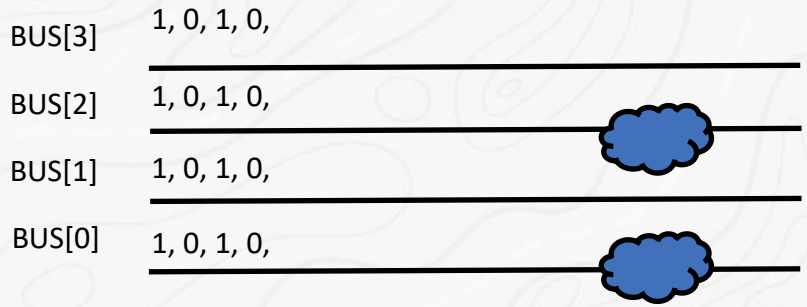
False Paths & CDCs

- CDCs generally labeled as false-paths.

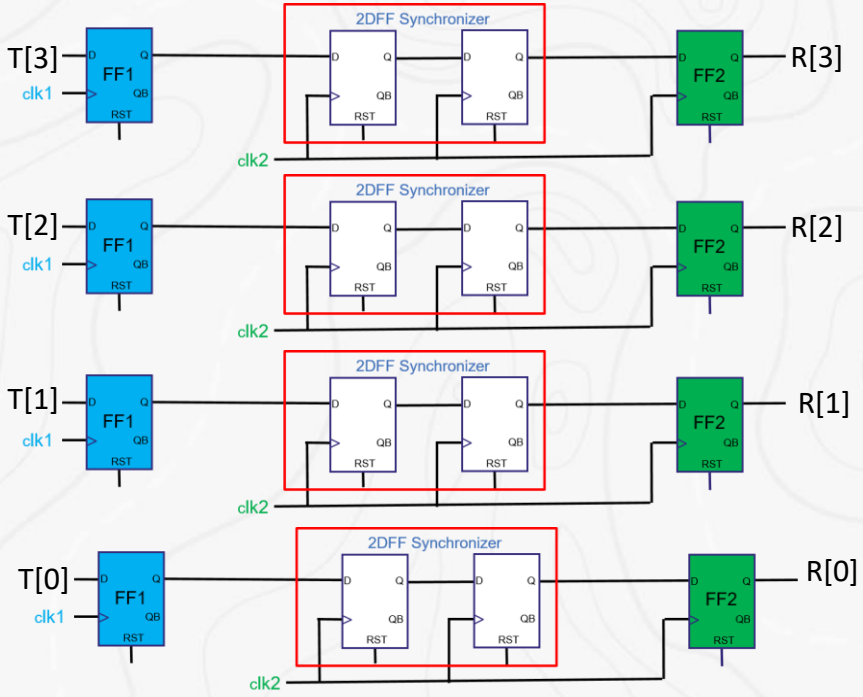


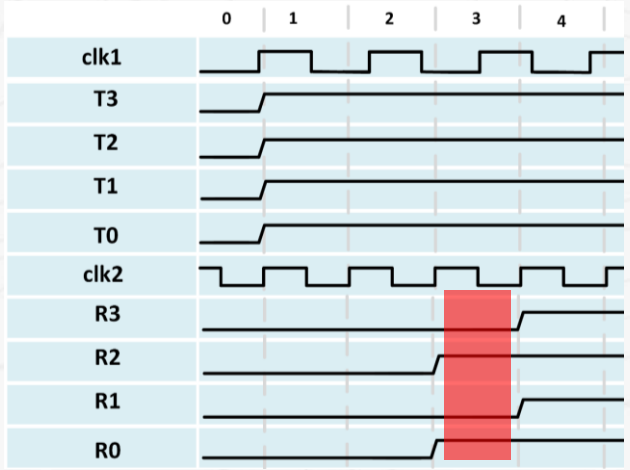
Data Skew

“0000”,”1111”,”0000”,”1111”

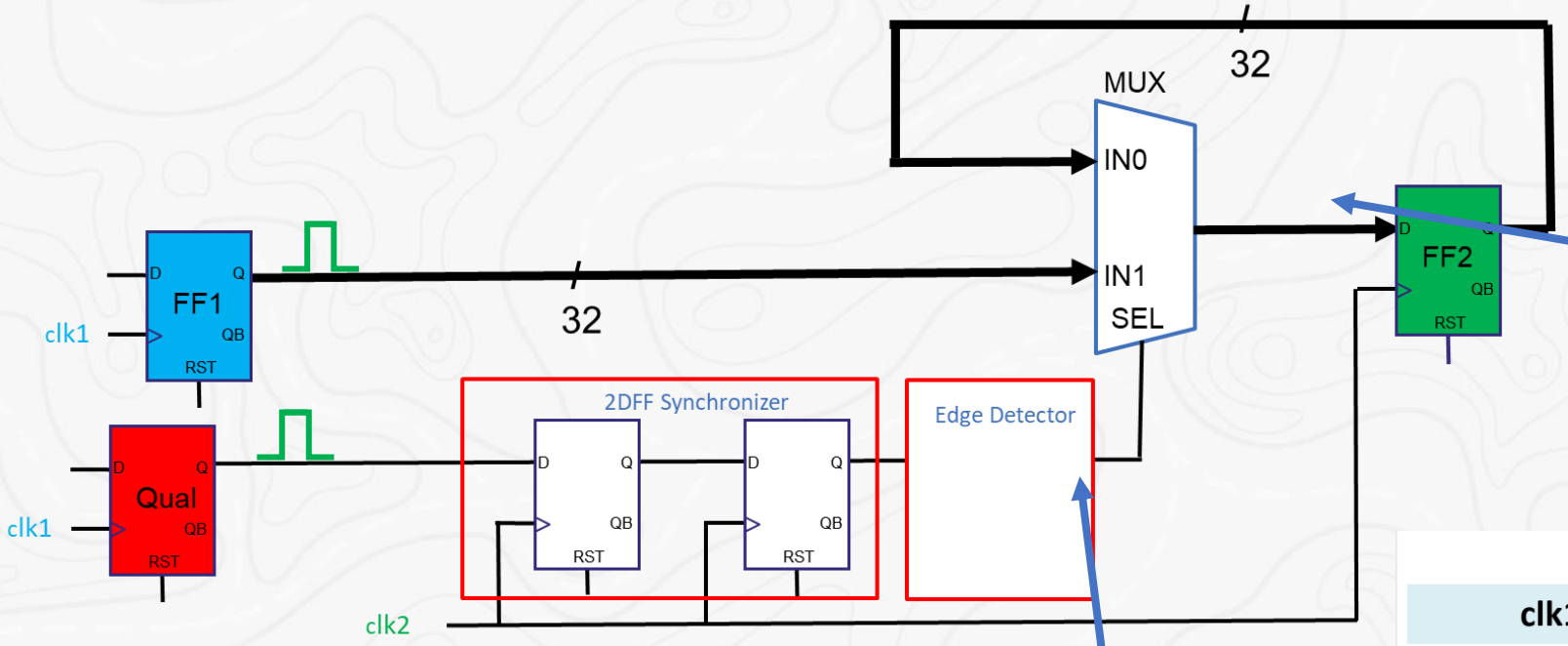


“0000”,”1010”,”0101”,”1010”





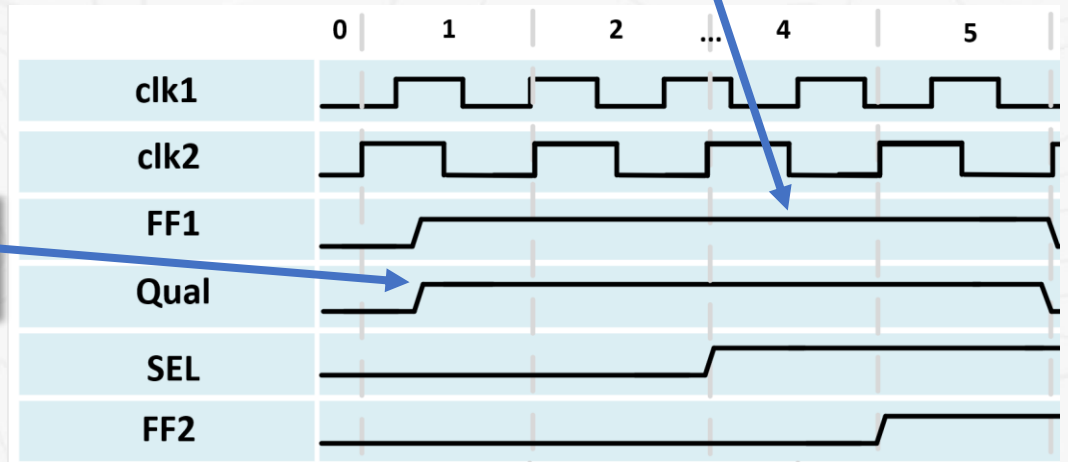
CDC Bus Synchronizer (DMUX) Operation



Bus is sampled

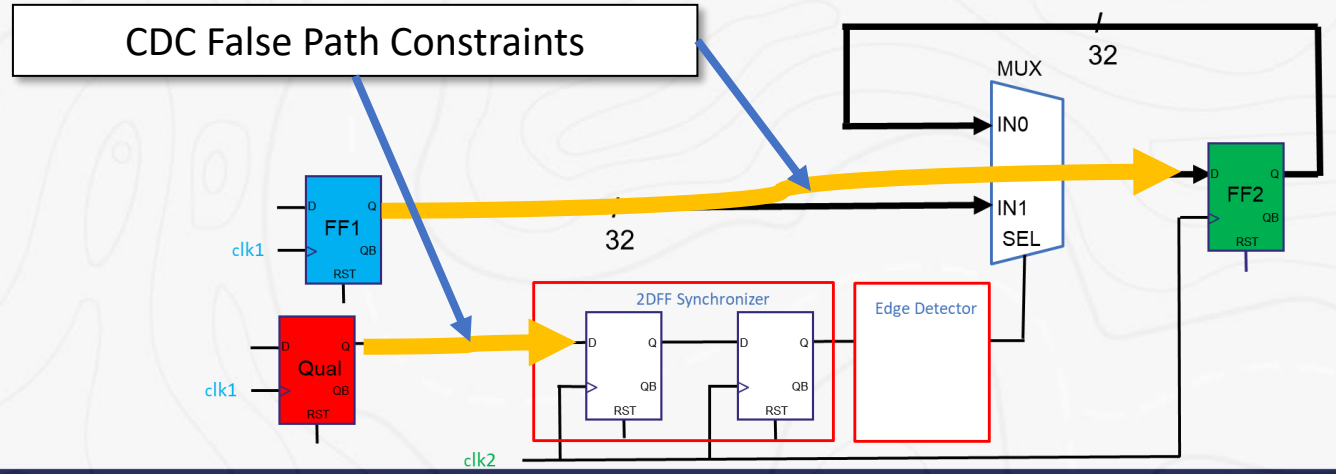
Data bus kept stable minimum 3 Receive Clock Cycles

Qualifier indicates data stable and is synchronized.

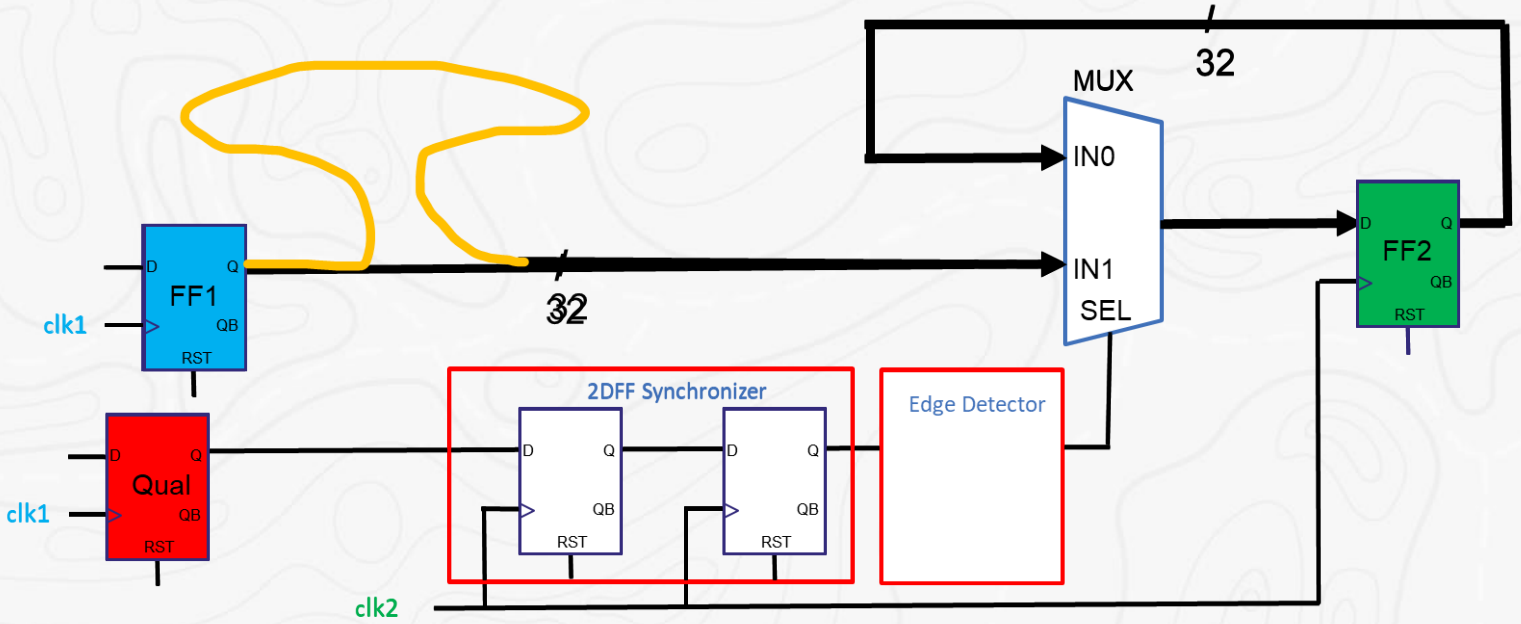


False Paths & CDCs

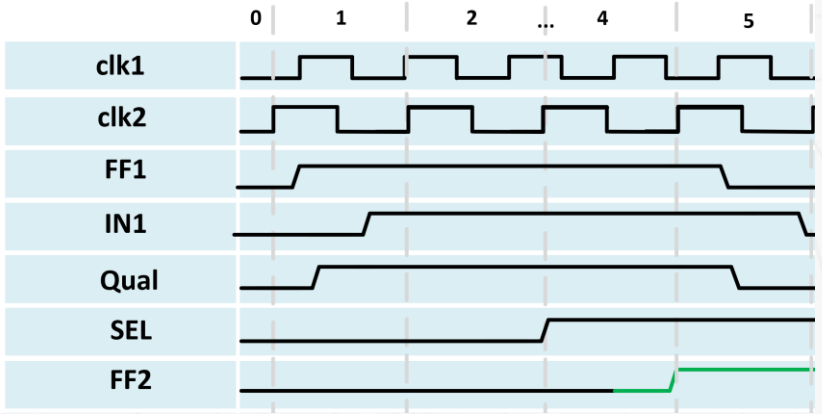
- In large high-speed designs time delay from source FF1 to destination FF2 can be multiple receive clock cycles.
- CDCs are generally constrained as false-paths.
- Global constraints on CDC paths such as *max_delay = 1 receive_clock_cycle* will generally not meet timing.
- Can cause 3 kinds of silicon bugs (not detectable in RTL simulation or front-end CDC checks).



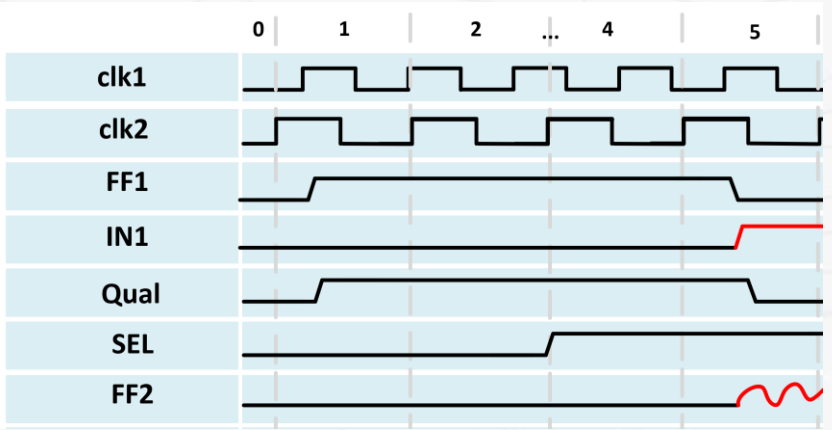
Delayed Data Bus Violation



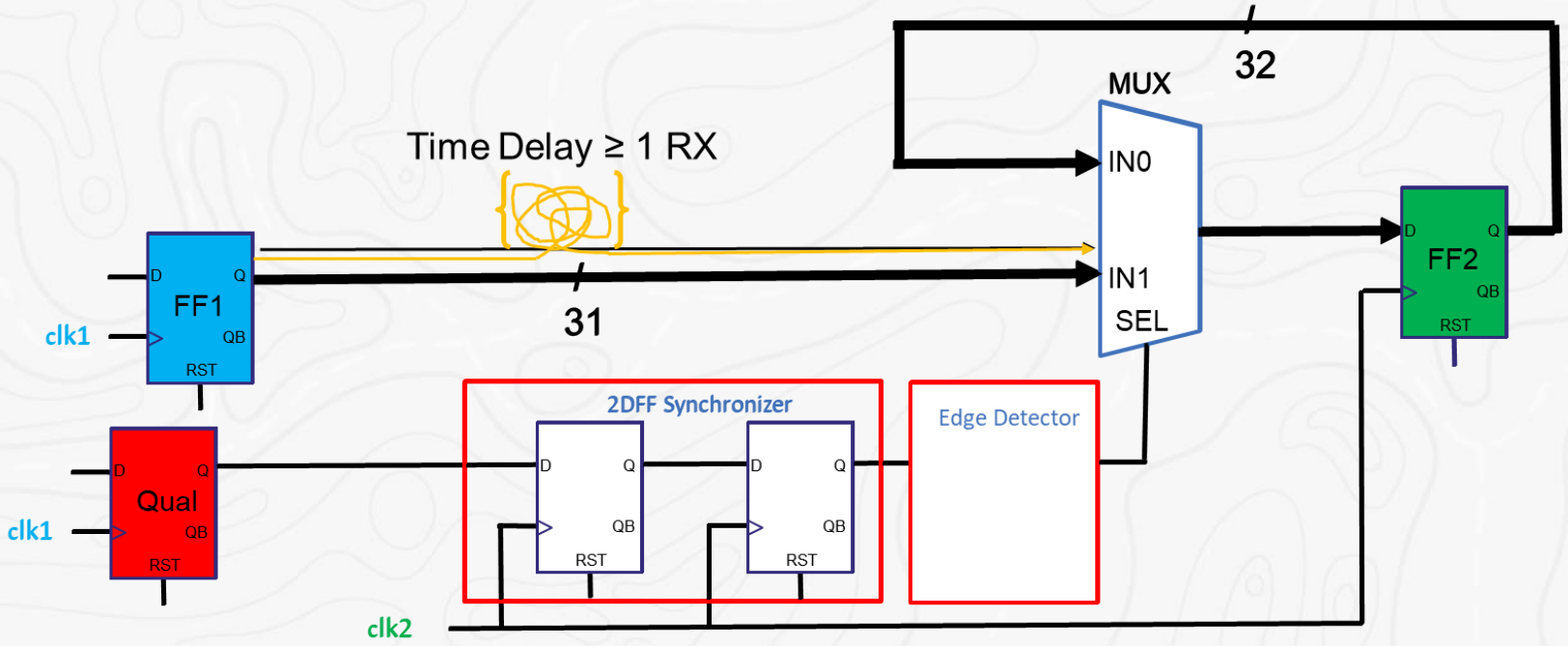
Data Bus Delay < 2 RX Clock Cycle Delay



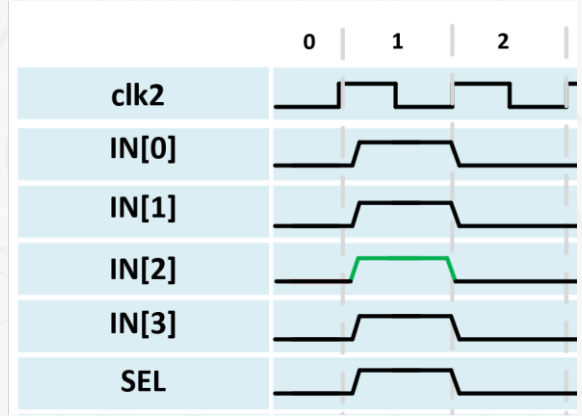
Data Bus Delay > 2 RX Clock Cycle Delay



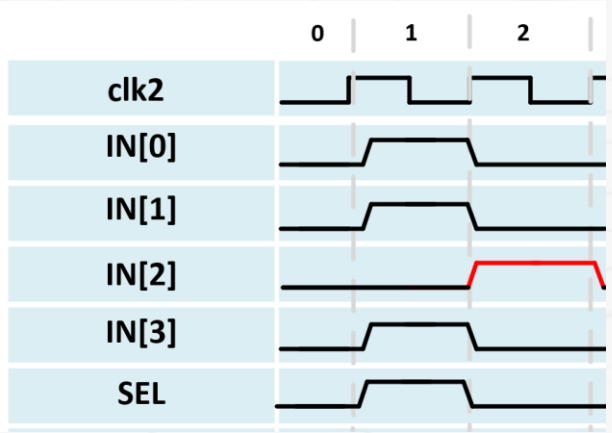
Delayed Data Bit Violation



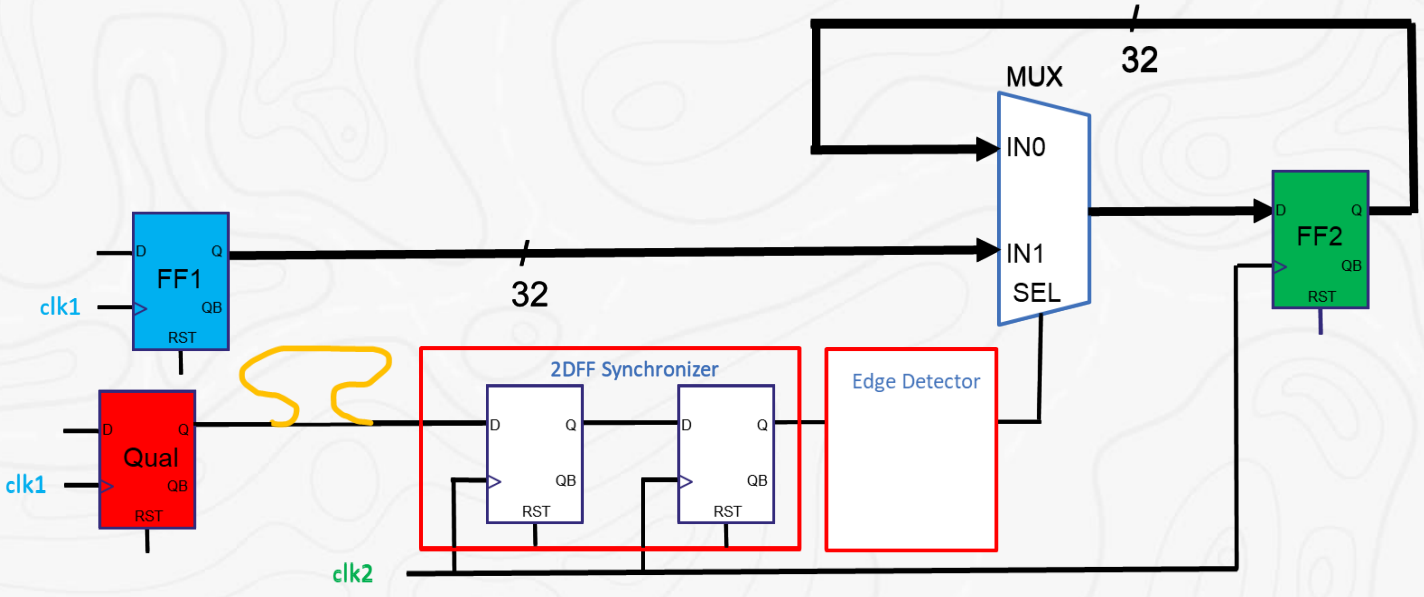
1 bit < 2 Clock Cycle Delay



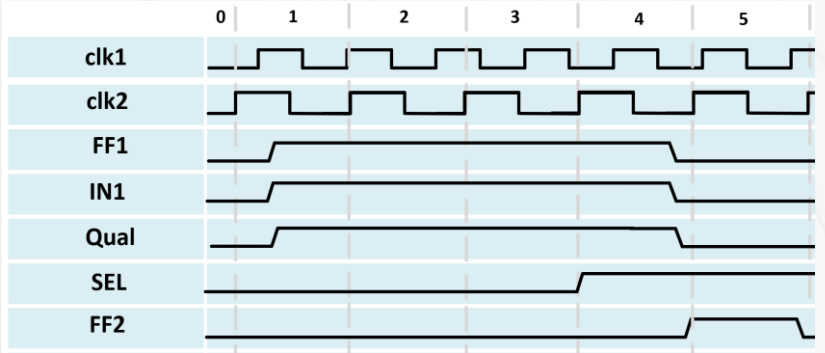
1 bit > 2 Clock Cycle Delay



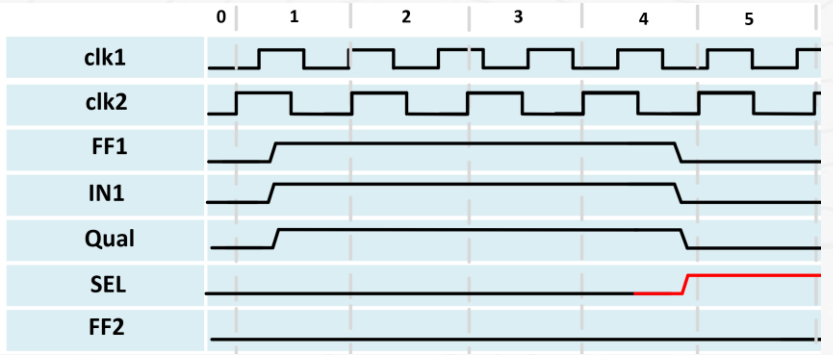
Delayed Qualifier Violation



Qualifier no Clock Cycle Delay

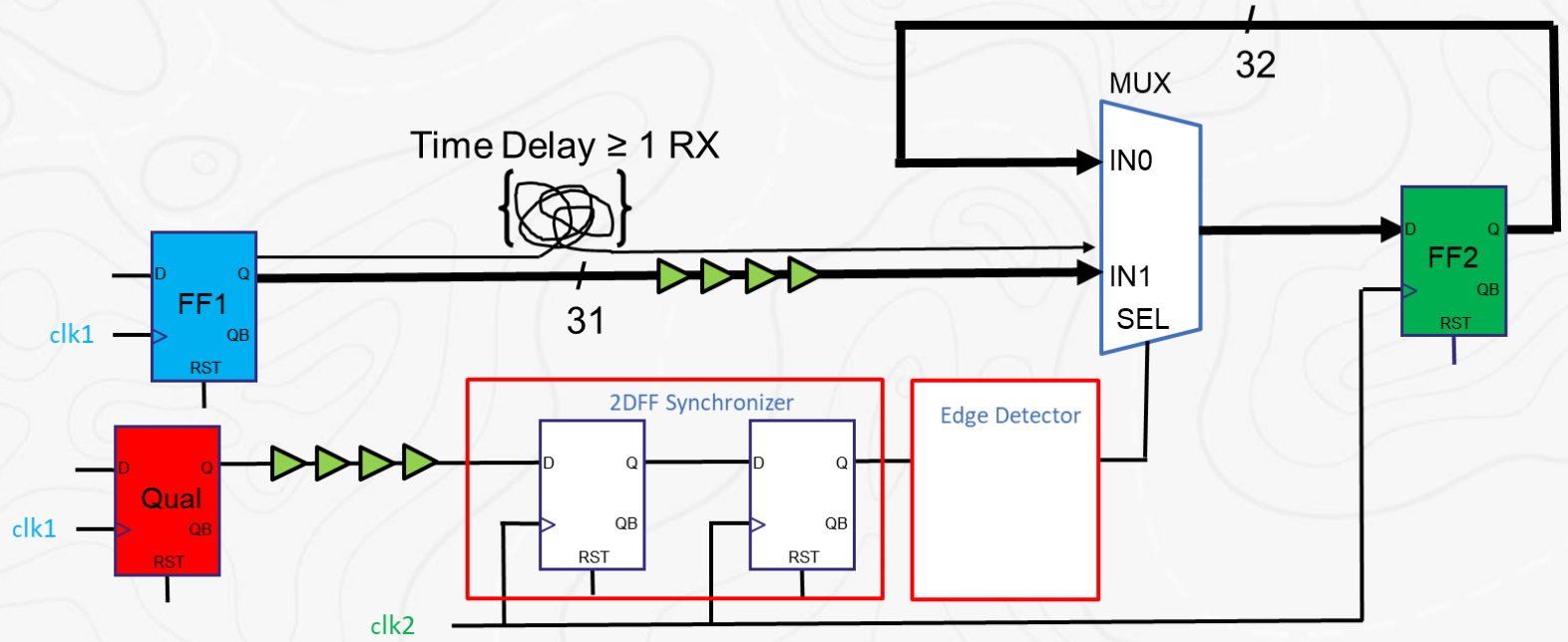


Qualifier > 1 Clock Cycle Delay



Silicon Solution

- Bugs arise because simulation behavior does not match silicon implementation.
- If detected, bugs can be easily resolved with timing fixes such as buffer insertion.



Previous Detection Strategies

Simulation

Gate Level Simulation (GLS)

Timing Analysis

max_delay <= *1 RX* constraint on all async paths

Strict Naming Conventions of CDC path sources and destinations

CDC Reports to analyze groups skew of combined CDC bus and qualifier

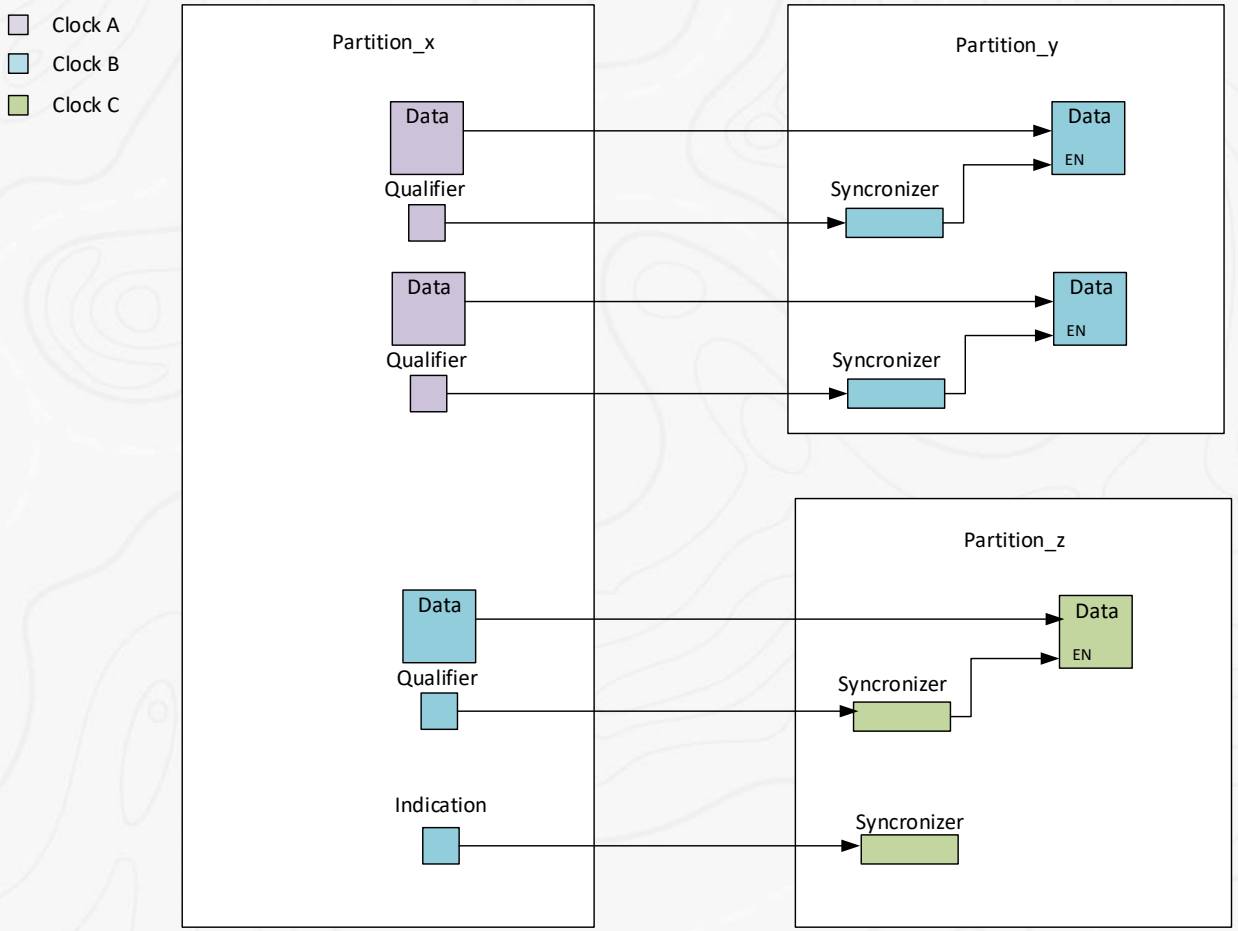
New Solution Assumptions and Goals

- Assumptions:
  - Large designs are divided at the RTL level into multiple partitions.
  - At the partition level timing issues as result of CDC paths are negligible.
  - Between partitions start and endpoints are distant.

- Goals:
  - Minimum effort for both front-end and backend teams.
  - Removes responsibility and work from front-end designers to backend engineers.

New Solution – Path Grouping

- Divide *all* CDC paths into groups according to:
  - Source: partition & clock
  - Destination: partition & clock
- The grouping is done regardless of the path type or functionality.



New Solution – Group Analysis

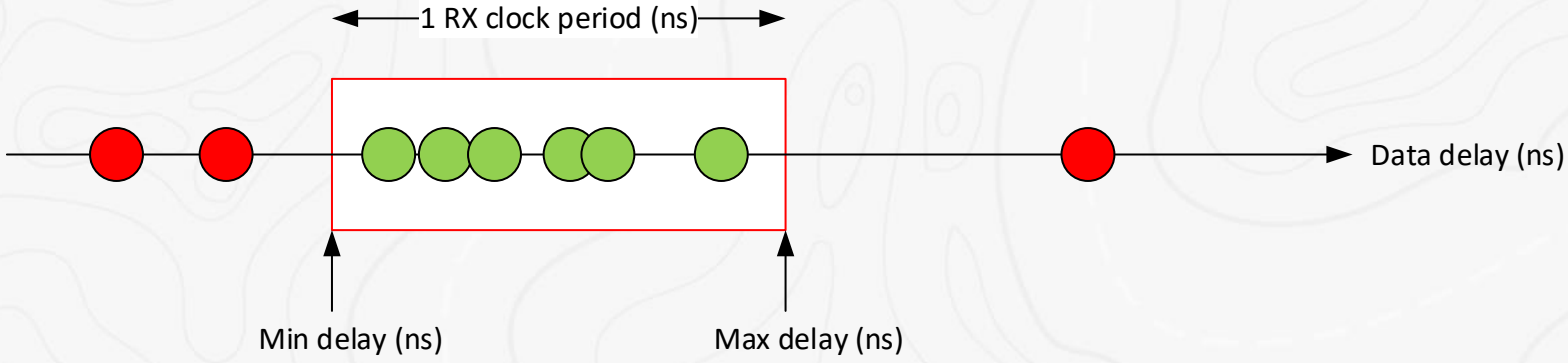
- Gather the actual Datapath delay of each path in the group.
- Define “delay window“ as a timing window the size of the RX clock period.
- Find optimal delay window that contains the largest number of paths.

SP_Par	EP_Par	SP_clk	EP_clk	Datapath Delay(ns)
Par_A	Par_C	Clk_D	Clk_B	0.625305
Par_A	Par_C	Clk_D	Clk_B	0.701674
Par_A	Par_C	Clk_D	Clk_B	0.797138
Par_A	Par_C	Clk_D	Clk_B	0.848277

SP = Start Point , EP = End Point

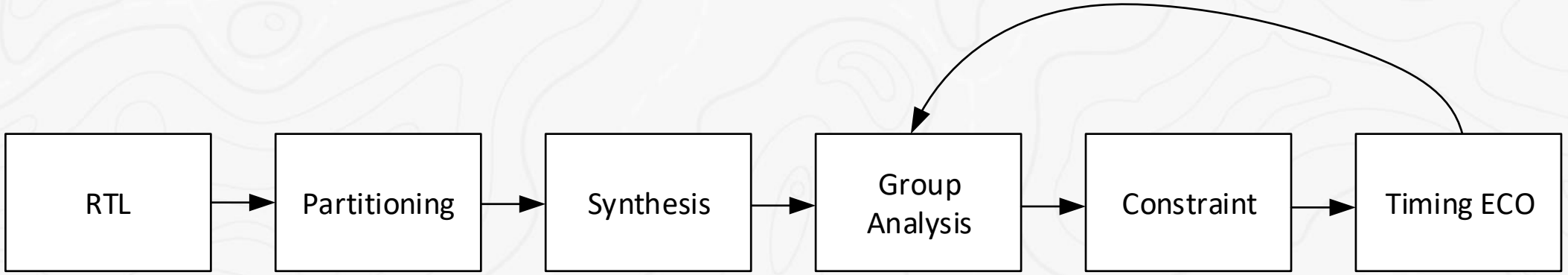
New Solution – Group SD Constraints

- The boundaries of the delay window define the SD constraints for this group.
- SD uses the constraints to perform a timing ECO.
- Paths from the same group usually travel similar distances.



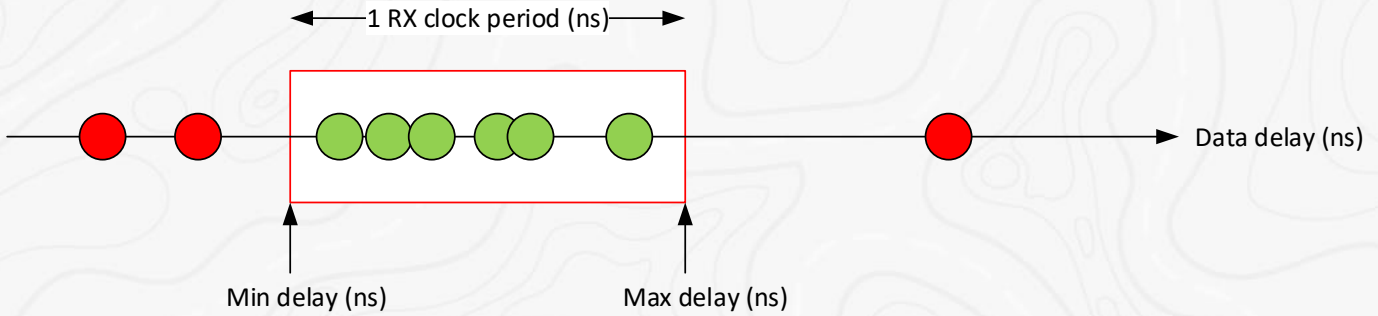
New Solution – Iteration

- Define – Group Analysis + SD Constraint + timing ECO as Iteration
- Perform several iterations until all the group paths fit into the delay window.

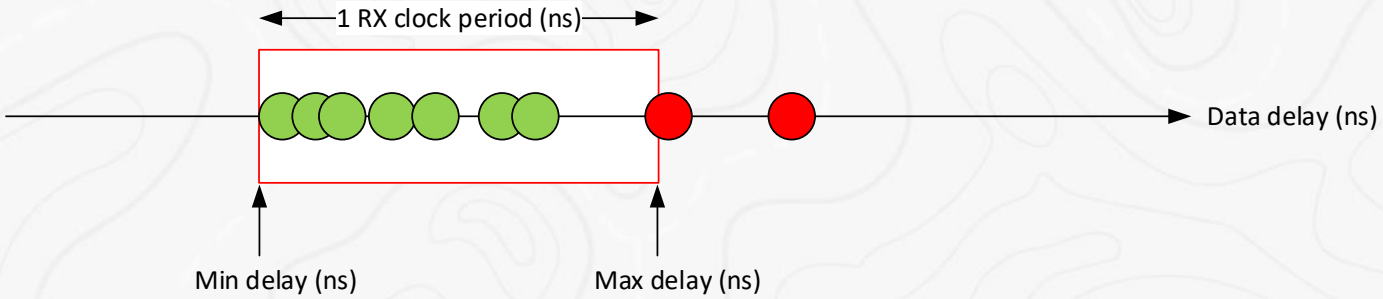


New Solution – Full Solution Per Group

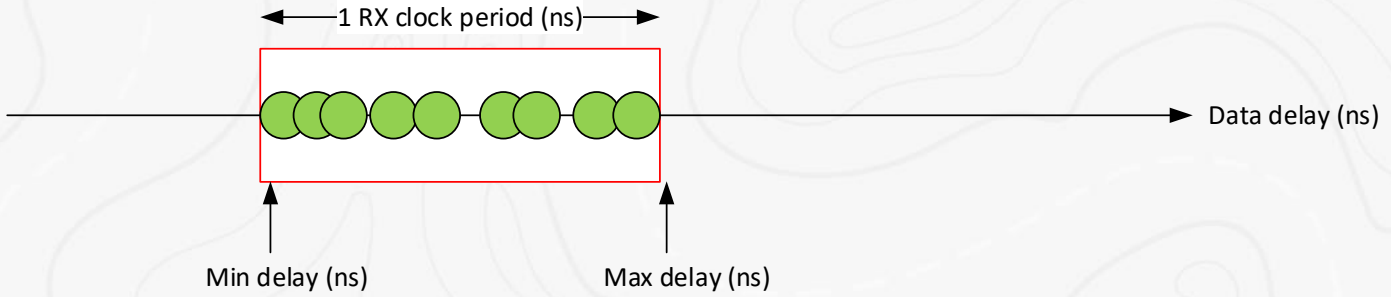
Iteration 1: Several paths won't meet the window



Iteration 2: The path delays are gathered closer together due to the constraints from iteration 1.



Iteration N: The path delays meet the timing constraints.



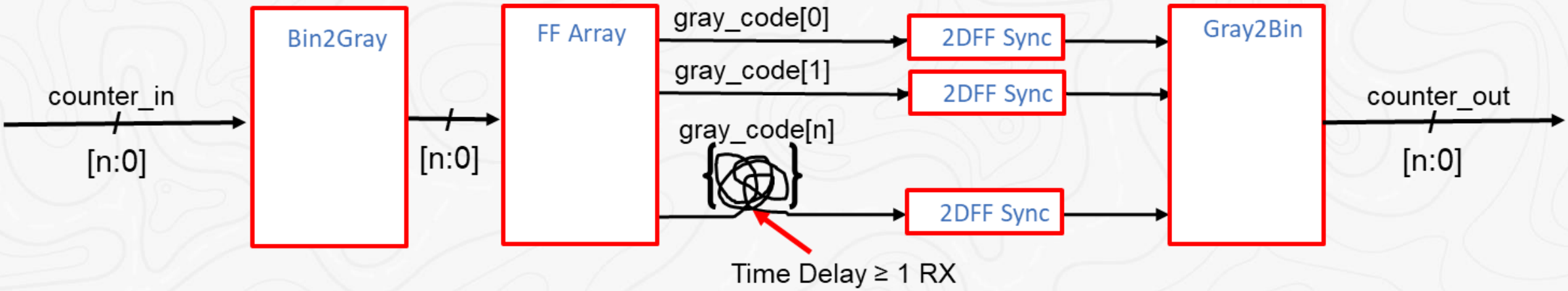
New Solution – Advantages

- Fully automated for the front-end using a script.
- Bulletproof – we won't miss checking skew for a path, as the global constraints per group cover all paths.
- Removes the need for manual review.
- Timing ECOs are already part of SD cycle – no extra effort for backend if used in sync with the SD cycle.

Questions?

Backup

Gray Code


counter_in
[n:0]
Bin2Gray
[n:0]
FF Array
gray_code[0]
gray_code[1]
gray_code[n]
2DFF Sync
2DFF Sync
2DFF Sync
Gray2Bin
counter_out
[n:0]
Time Delay ≥ 1 RX