Empowering Innovation

Harnessing collective wisdom across tools, processes, and people

Harry Foster

Chief Scientist Verification

Digital Verification Technologies

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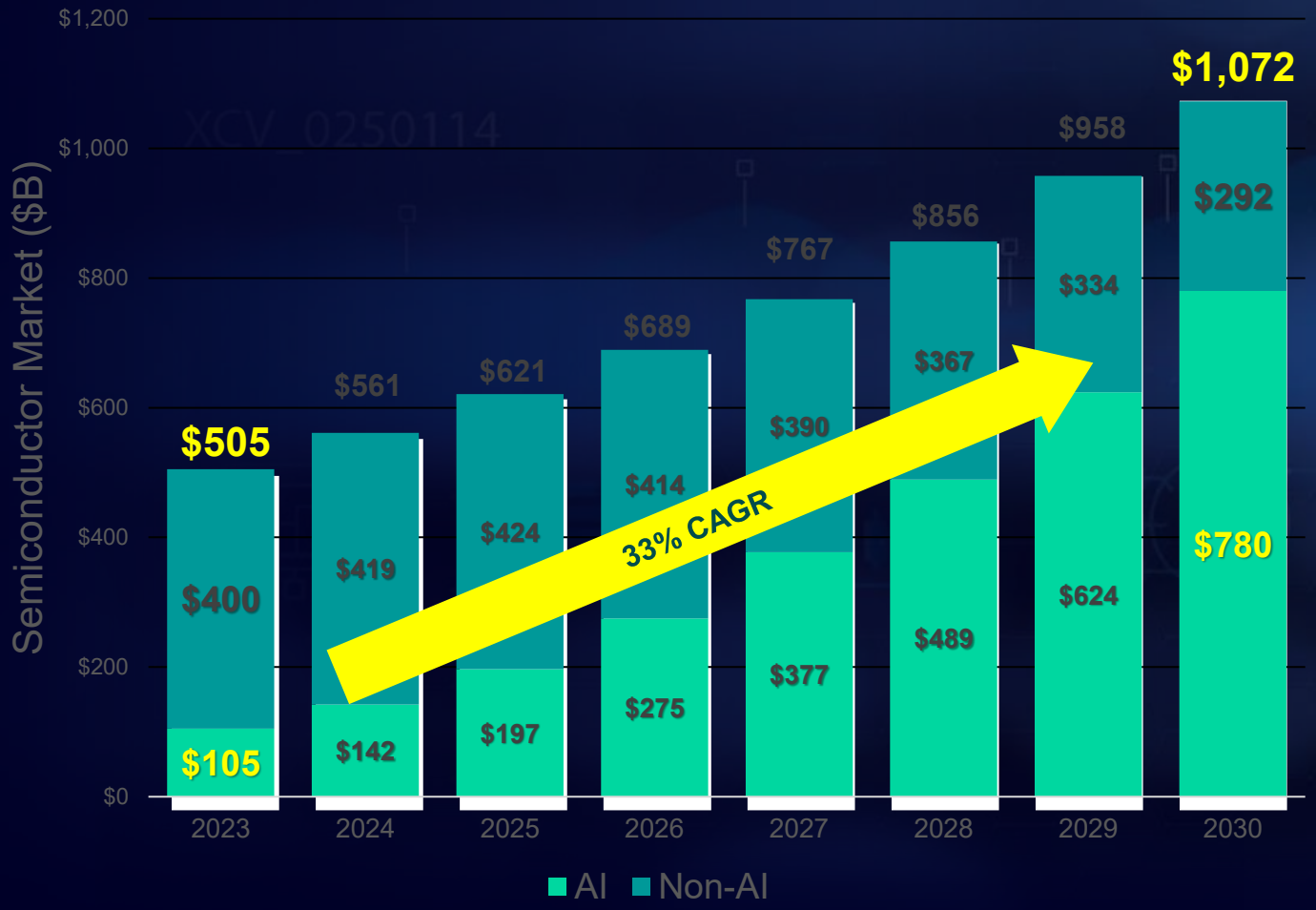
Total Semiconductor Market and AI Semiconductor Market

In 2023 21% of semiconductor market associated with AI and grows to 73% by 2030



Source: IBS Jan 2024 Report: First Generative AI Report: Impact of Generative AI on Semiconductor Industry

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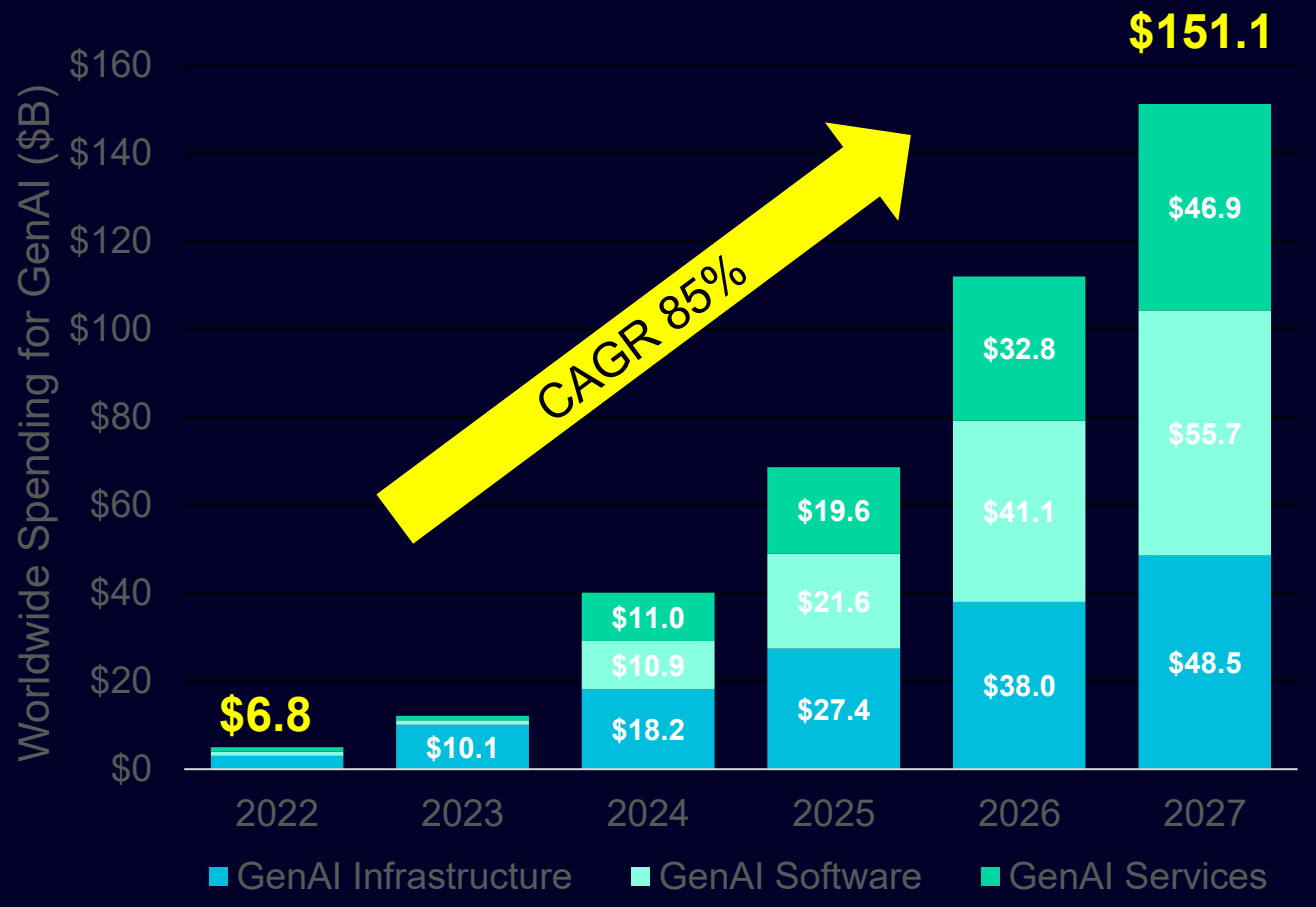
Worldwide Spending for GenAI Infrastructure, Software, and Services

2022-2027 GenAI Spending and Growth Rate

GenAI Growth Rate

- Infrastructure 71.1% CAGR
- Software 99.6% CAGR
- Services 94.2% CAGR



Source: IDC Dec 2023 Report: Core IT and Spending for GenAI Forecast

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Disruptive trends in the global datasphere

Reshaping computing, networking, communication, security, and applications

1^{ZB} = 1,000,000,000,000,000,000,000 (10^{21}) = 250 billion DVDs

Global Datasphere is a measure of how much data is created, captured, replicated, and consumed each year.

Source: IDC Apr 2023 Report: Worldwide IDC Global Datasphere Forecast, 2023-2027

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Macro trends in growing complexity

Reshaping computing, networking, communication, security, and applications

Sensors /
Edge Computing

Collect

5G /
Wireless

Transmit

Cloud /
Networking

Process

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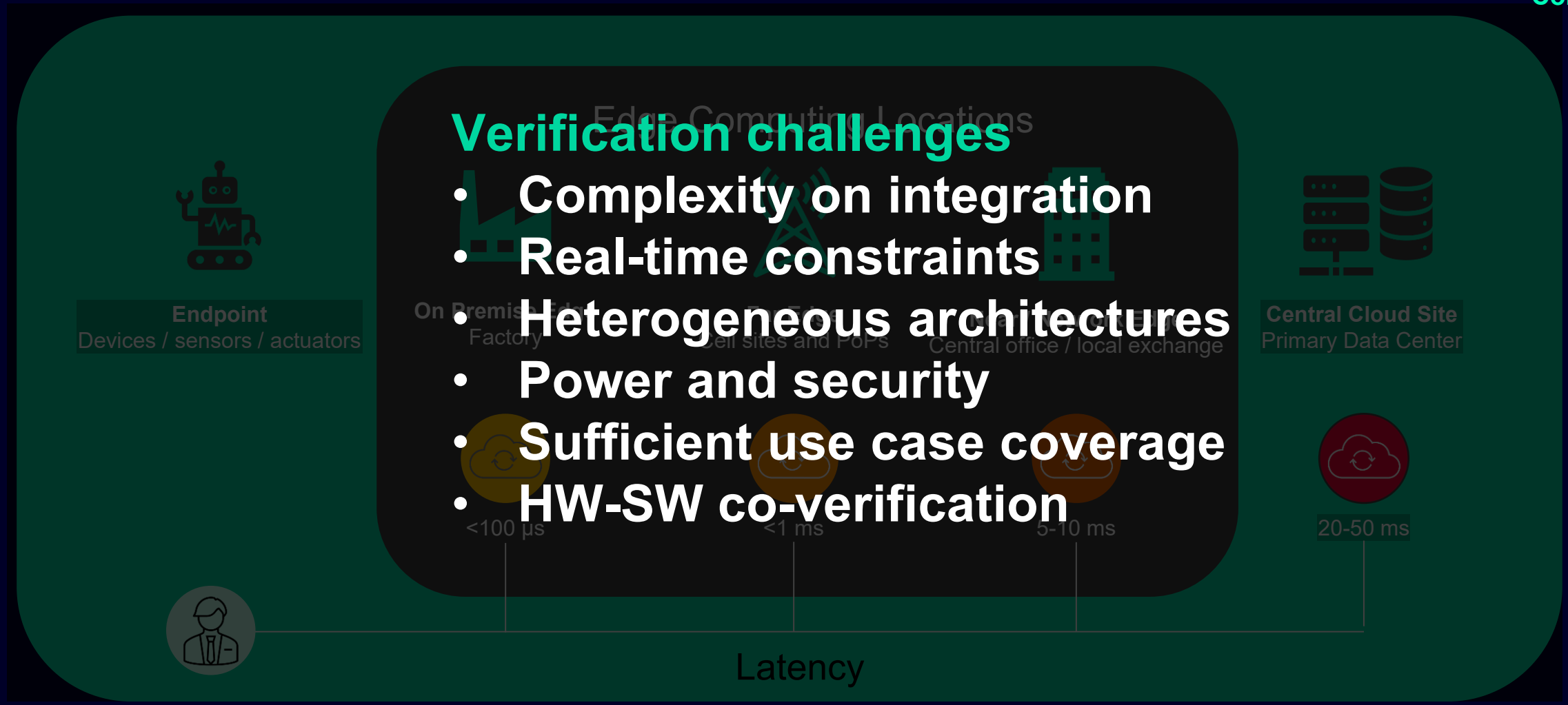
Edge computing trends — it's all about latency!

75% of data compute moves to the edge in the next few years

Collect



Verification challenges

- Complexity on integration
- Real-time constraints
- Heterogeneous architectures
- Power and security
- Sufficient use case coverage
- HW-SW co-verification

Source: Application PerformancemArticles, Digital Experience, Network Performance, Mar 24, 2022
AXIOS, AI drives explosion in edge computing, Feb 16, 2024

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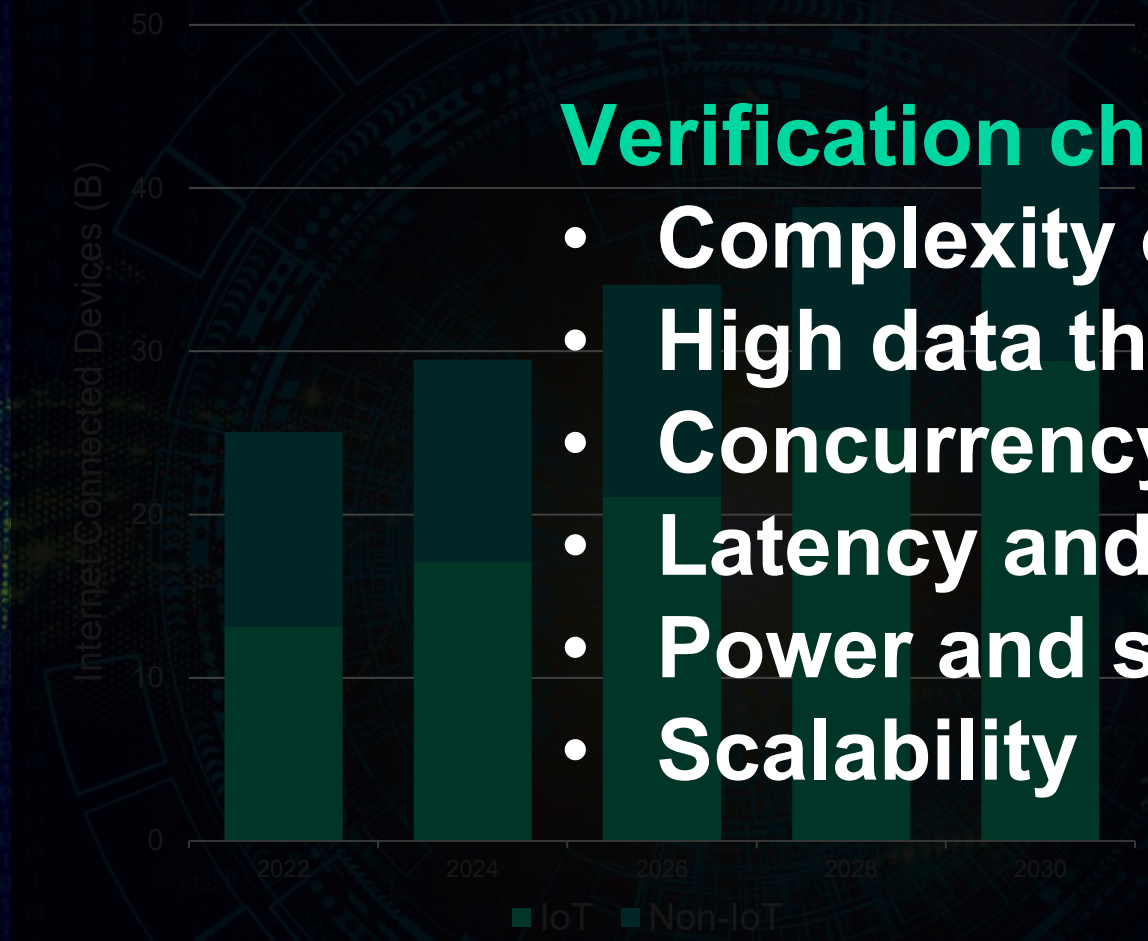
Hyperconnected trends by 2030

44 billion devices connected to the internet by 2030, growing at a 12% CAGR

Transmit



Verification challenges includes

- **Complexity of interconnections**
- **High data throughput**
- **Concurrency**
- **Latency and timing**
- **Power and security**
- **Scalability**

- World population 8.5 billion by 2030
- 44 billion internet devices by 2030

- WiFi 6 improved performance, capacity, battery life, speed in congested areas
- 5G high speed, low latency, massive capacity

- *Cyber security & resilience an issue, and AI critical to monitoring and preventing issues*
- *AI becomes more critical to manage, optimize, and debug networks*

Source: Exploding Topics: Number of IoT Devices (2024), Feb 19, 2024

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Hyperscale computing — it's all about scalability!

Cost-effectiveness, high performance, reliability and resilience, support big data

Process

Verification challenges includes

- Immense scale
- Stringent performance
- Complex concurrency
- Power requirements
- Robust security and reliability

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Security and Privacy in a Hyperconnected World

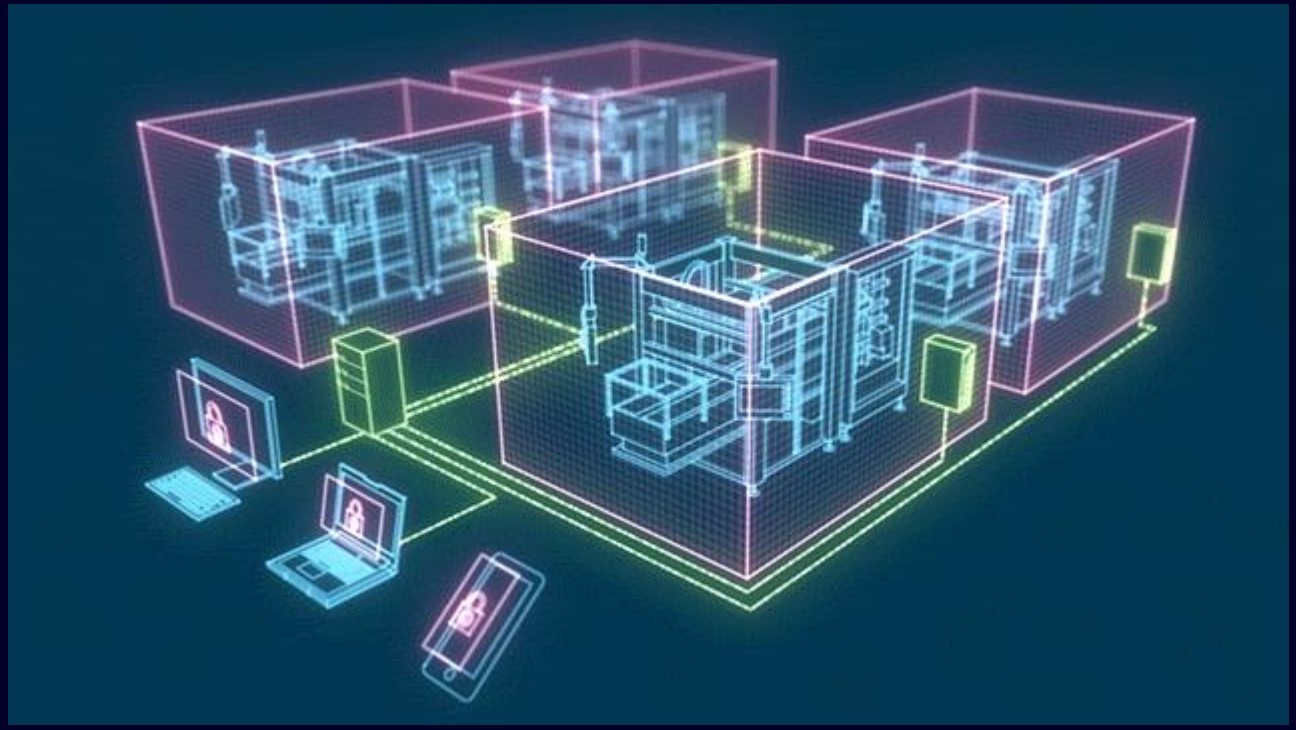
Security must be a foundational consideration, and verification key

8,214,886,660

Data breaches in 2023

$4,450,000

Average cost of major data breach



Source: IT Governance, List of Data Breaches and Cyber Attacks in 2023, Jan 5, 2024

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Environmental Sustainability
Data growth and energy consumption

Energy consumption link:

- Datacenters alone consume about 4% of the world's total energy
- Energy consumption will triple in the next decade

Energy consumption and AI:

- Training GPT-3 consumed 1300 megawatt hours (MWh) of energy
  - As much power consumed annually by 130 US homes
  - Streaming an hour of Netflix requires around 0.8 kWh
    You'd have to watch 1,625,000 hours to consume the same amount of power

Low-power design and verification:

- Growing complexity in power-management
- Advanced low-power verification techniques and tools a necessity

LLM Market

33.2% CAGR

$6.4B 2024
$36.1B 2030

Source: GlobalNewsWire, Global Large Language Model (LLM) Research, April 10, 2024

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Emerging Challenges and Opportunities

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Industry Challenge for New Generation ICs
Ever-increasing Levels of Complexity

ASIC

Number of spins before production

ONLY

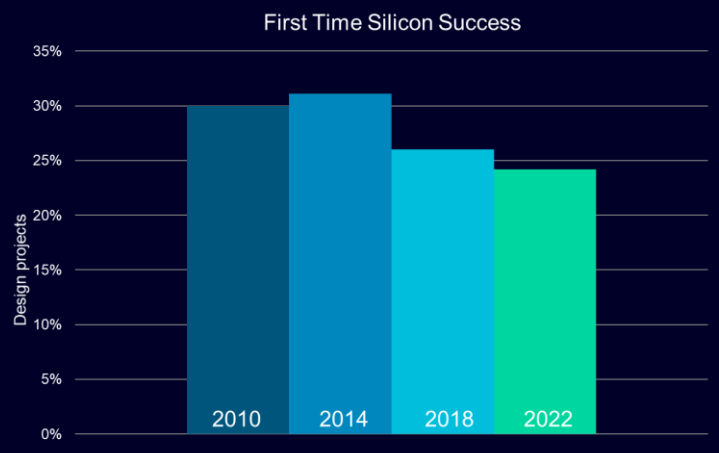
24%

Achieve first time silicon success

ONLY

36%

Projects finish on Schedule



Decline in first silicon success combined with increasing wafer and mask cost

FPGA

Number of Non-trivial Bug Escapes

ONLY

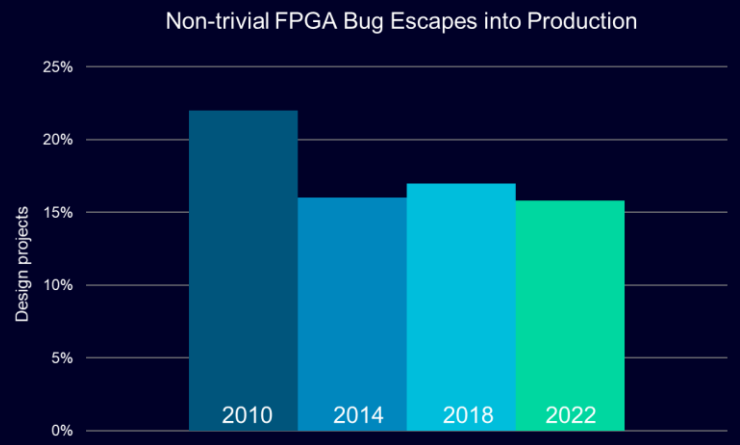
16%

Achieve zero bug escapes

ONLY

30%

Projects finish on Schedule



FPGA projects are performing no better than ASIC

Source: Wilson Research Group and Siemens EDA, 2022 Functional Verification Study

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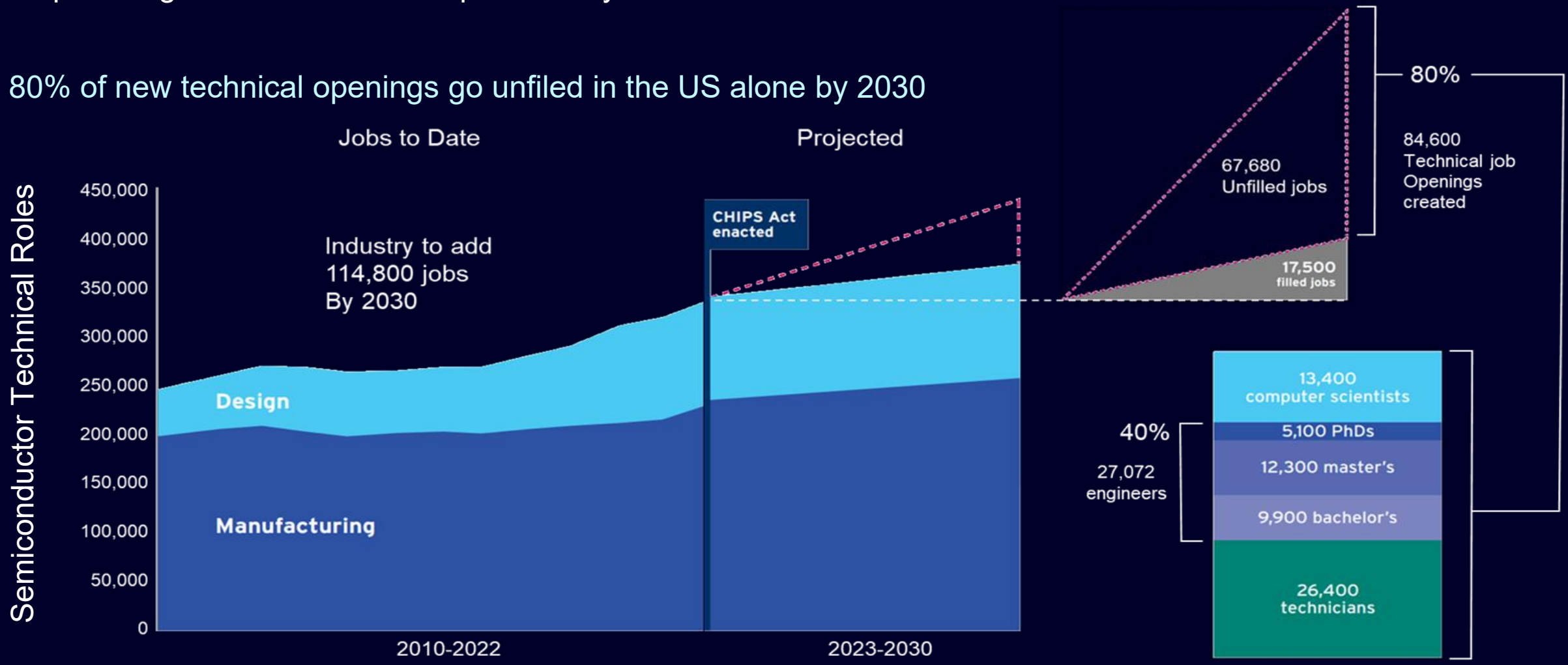
Fewer skilled workers available to meet demand

Requires significant increases in productivity to address this issue

80% of new technical openings go unfiled in the US alone by 2030



Sources: US Bureau of Labor Statistics; National Science Foundation; American Society of Engineering Education; US Citizen and Immigration Services; BCG analysis (Dec 13, 2023)

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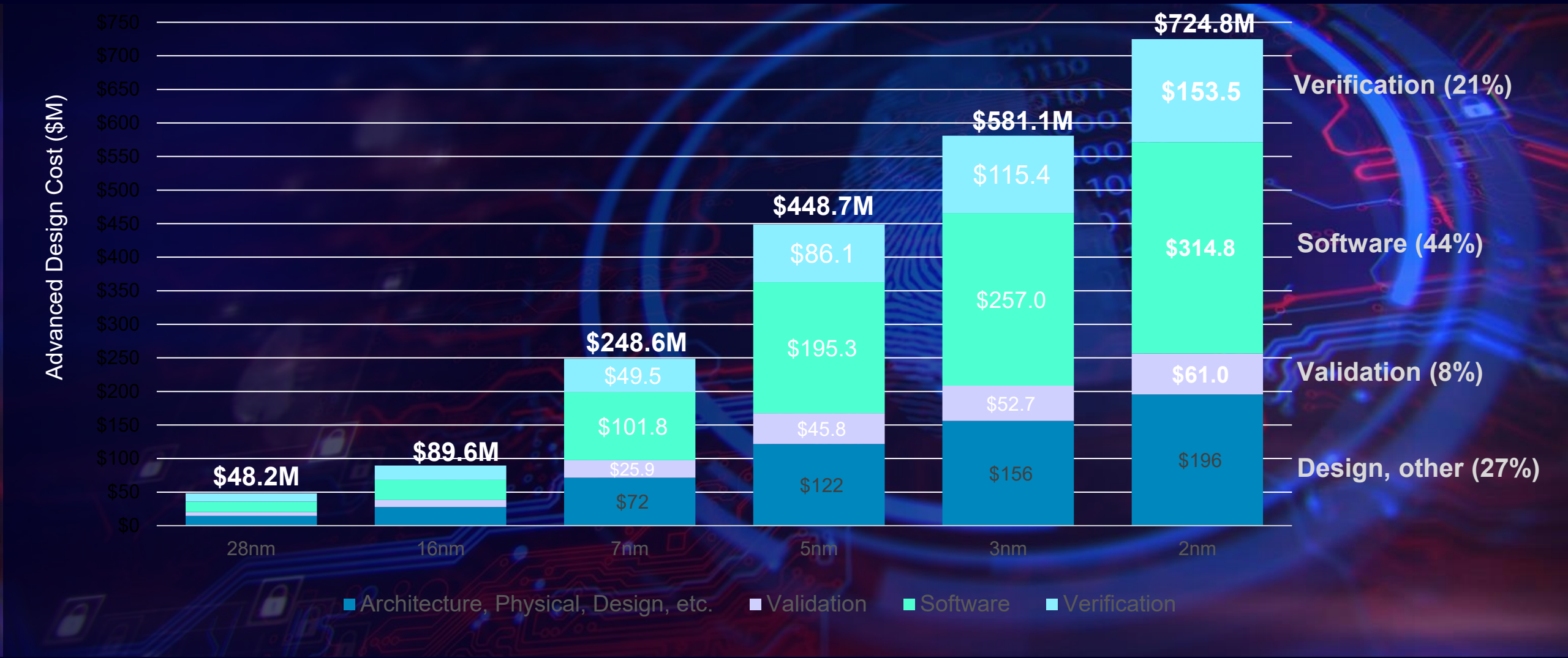
Design complexity driving cost!
Average cost for advanced design



Source: IBS Report, Design Activities and Strategies Implications, July 2022

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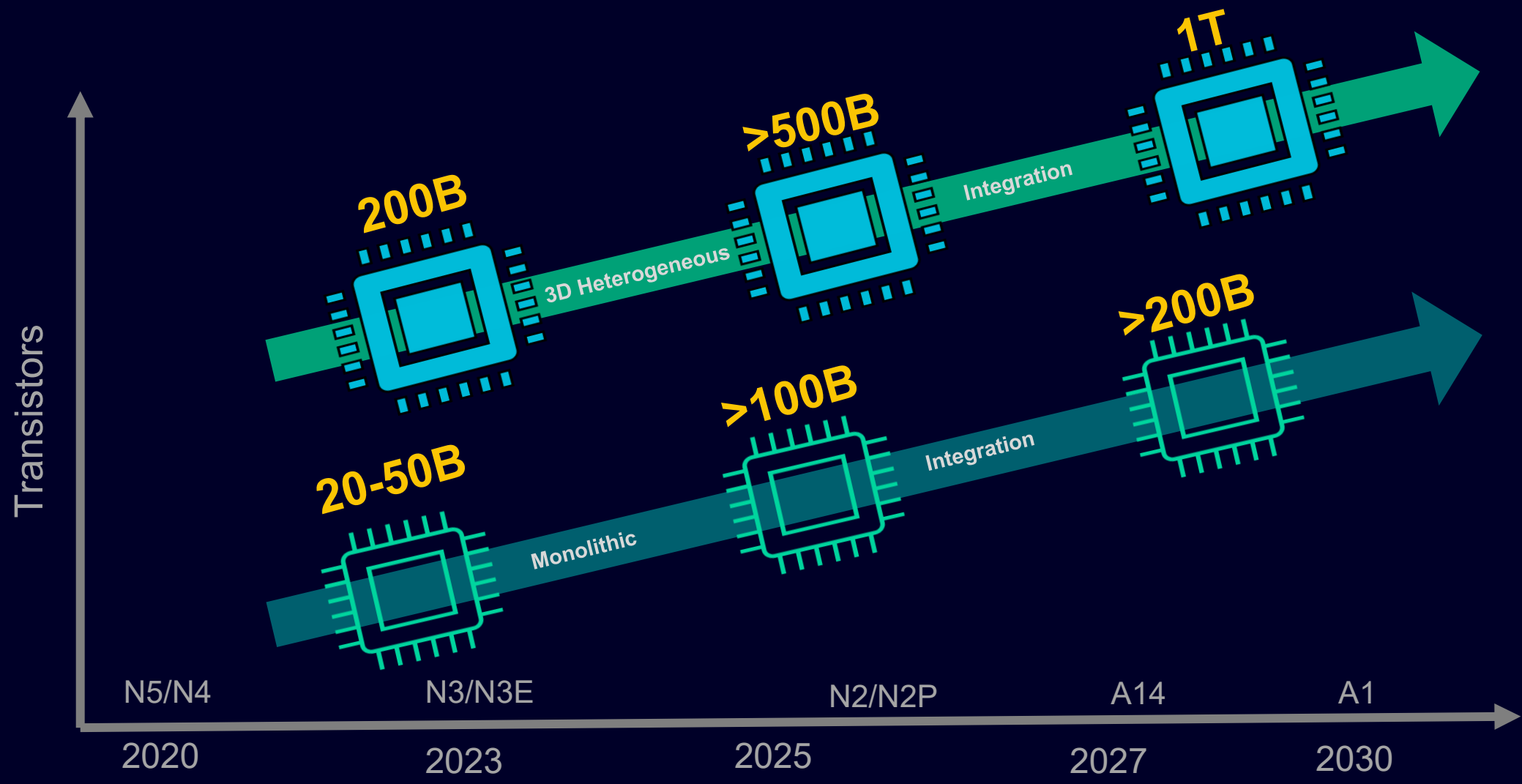
Chiplets and 3DIC

Moving monolithic SoCs to 3DIC and chiplet-based design



Source: WCCF Tech, TSMC Aims to Integrate Over 1 Trillion Transistors, Dec 2023

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Chiplets and 3DIC
Moving monolithic SoCs to 3DIC and chiplet-based design

Cost-effective scaling
- Alternative to traditional Moore's Law scaling through higher integration

Enhanced performance
- Increases processing power and speed by reducing interconnect

Reduce power consumption
- Shorter interconnects reduce power loss and improve energy efficiency

Interconnect protocol challenges
- Verifying complex UCIe 2.0 interconnect protocol adheres to specification
- Verifying compatibility between different chiplets from various vendors or design team

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Software defines and differentiates successful products

Development & validation must start as early as possible

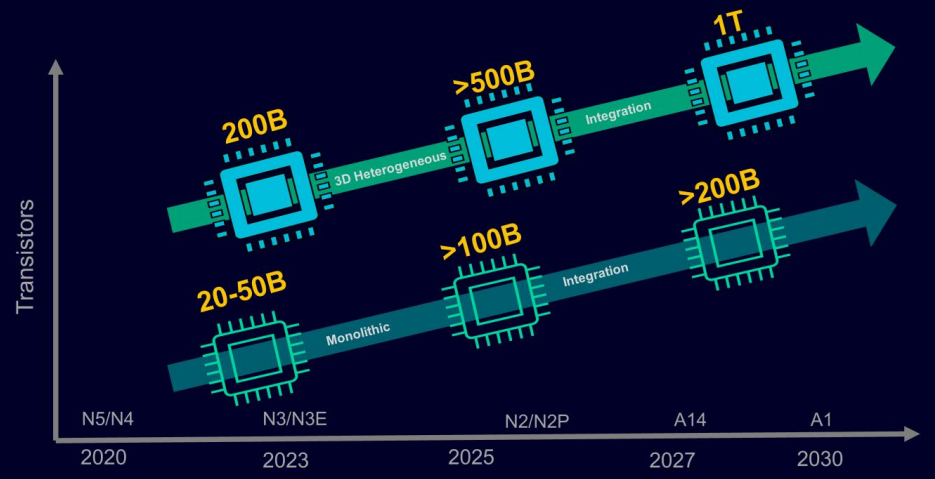
Software Key Component of Chip Architecture

- Increasing transistor count
- Rise in workload-optimized chips
- High mask and fab costs; first silicon success is crucial

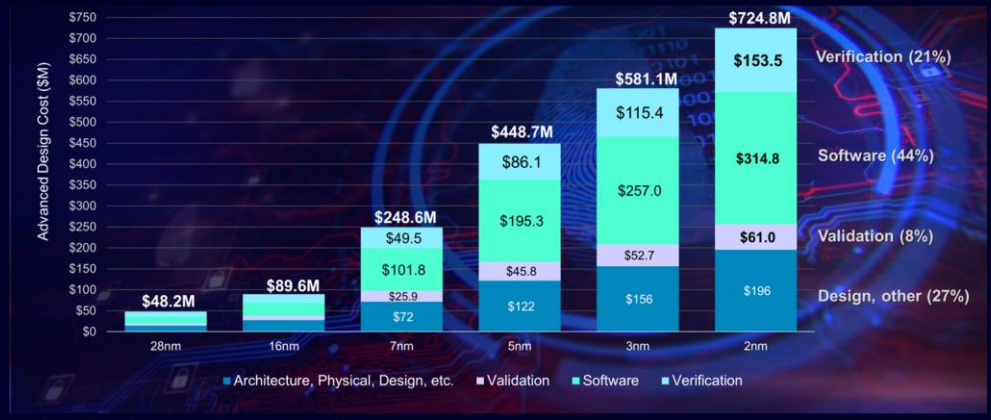
Software Dominates Costs

- Software is a key differentiator
- Delays in software readiness are costly
- Essential for silicon sales

Chiplets and 3DIC
Moving monolithic SoCs to 3DIC and chiplet-based design



Design complexity driving cost!
Average cost for advanced design



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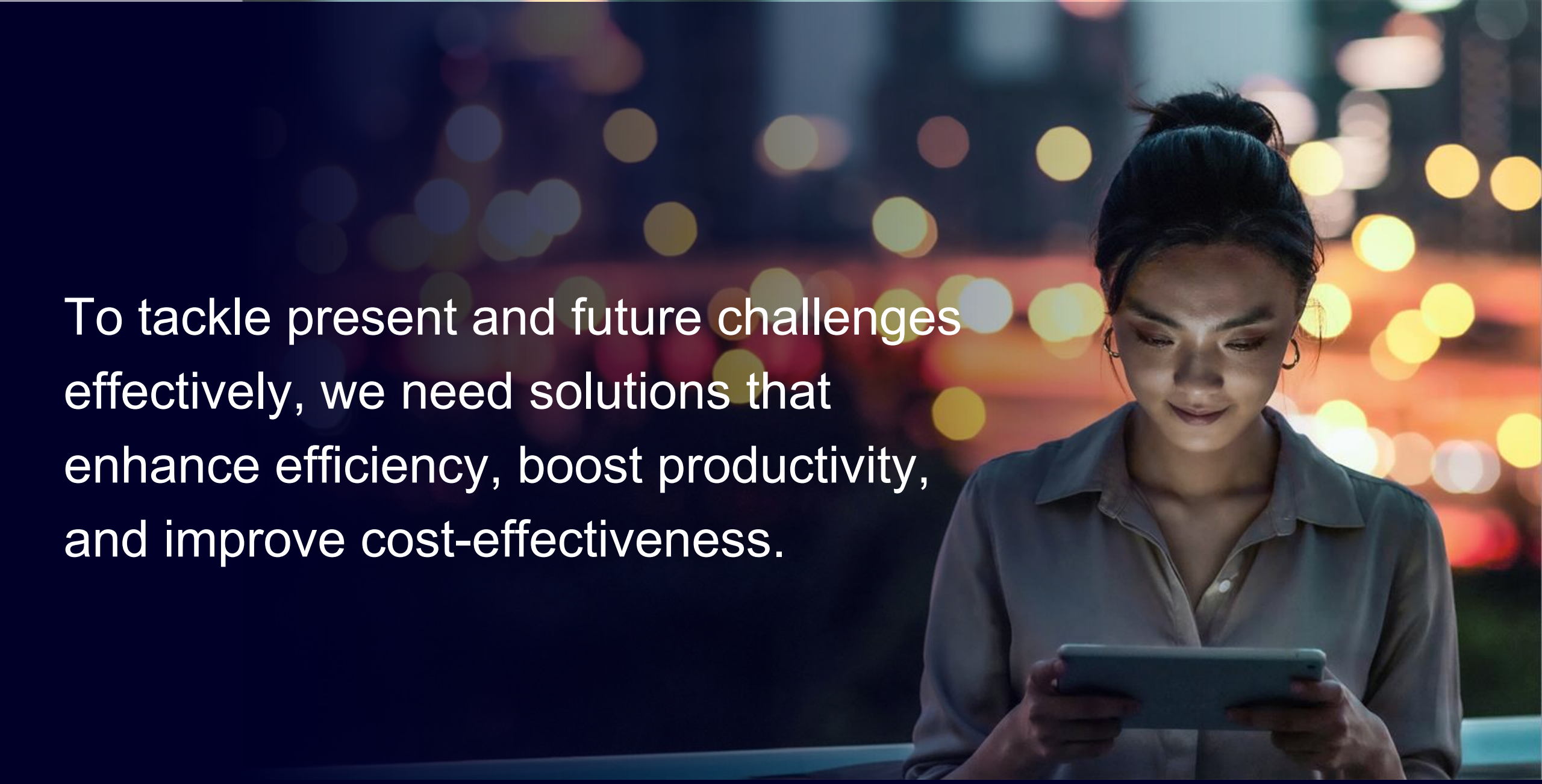

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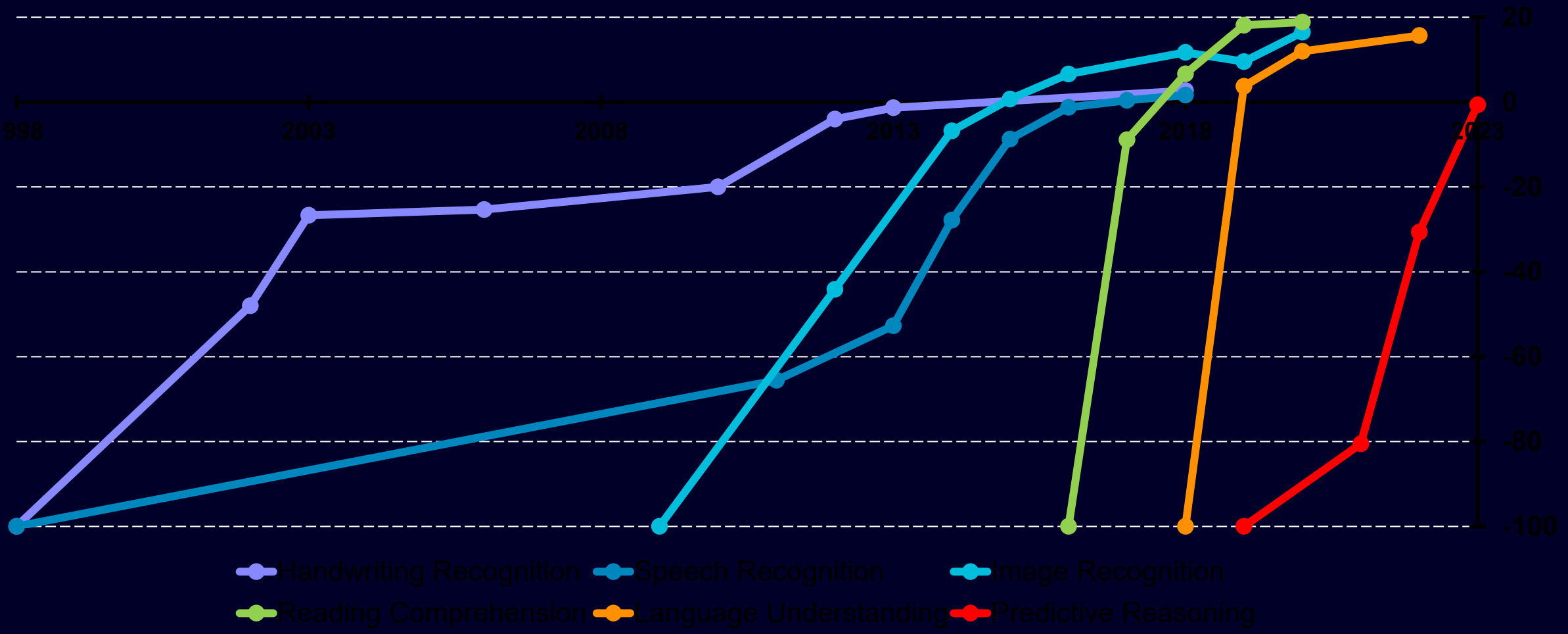
Why now?

Test scores of AI systems on various capabilities relative to human performance



Data Source: Kiela et al. (2023) – with minor processing by Our World in Data

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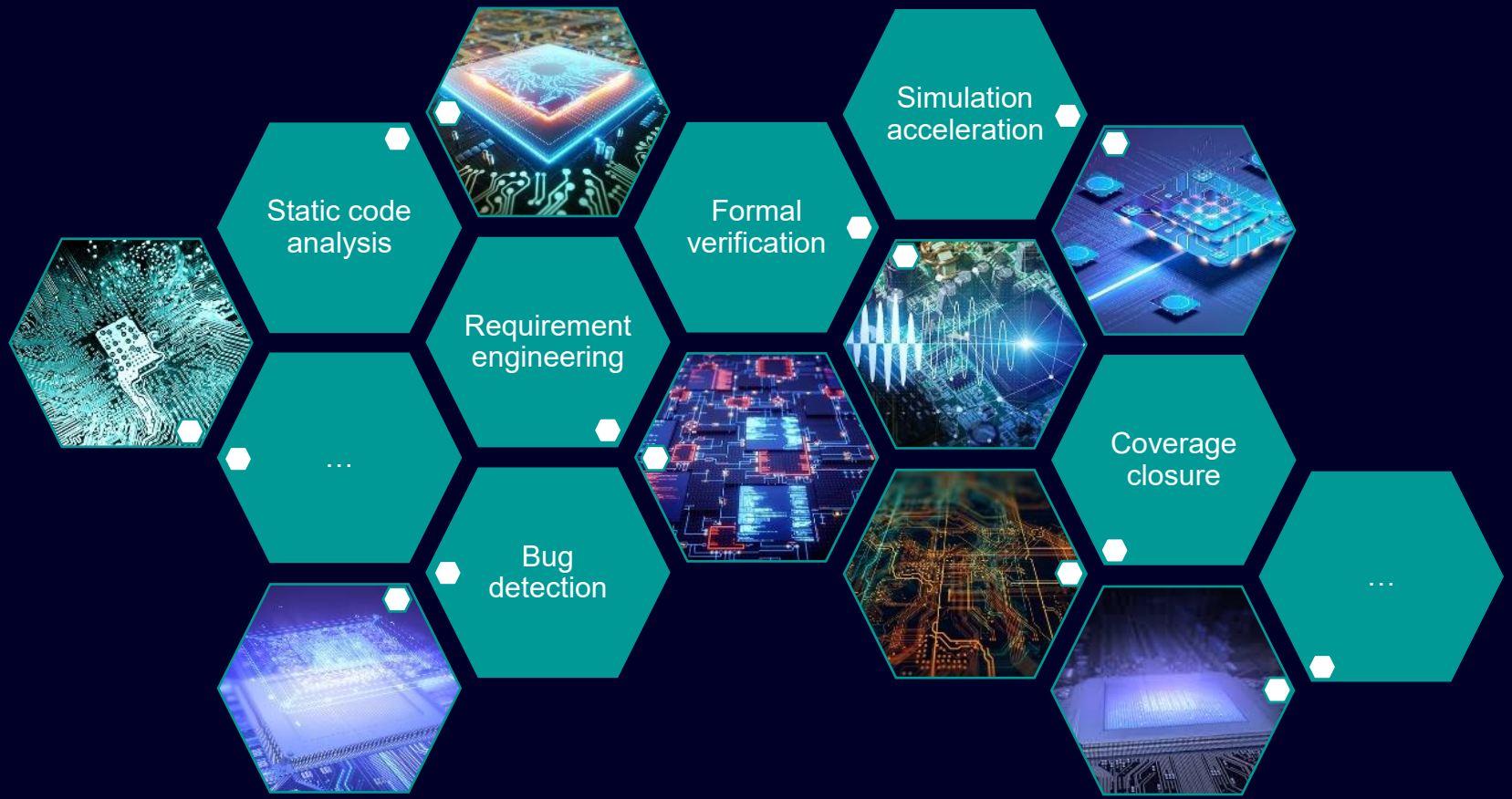
Verification is Fundamentally a Data Problem

A survey of published research



DVCon US 2023 Paper

DVCon US 2024 Paper

Source: D. Yu, H. Foster, T. Fitzpatrick, "A survey of machine learning applications in functional verification," DVCon US 2023

Source: D. Yu, et al., "Large Language Model for Verification: A Review and Its Application in Data Augmentation" DVCon US 2024

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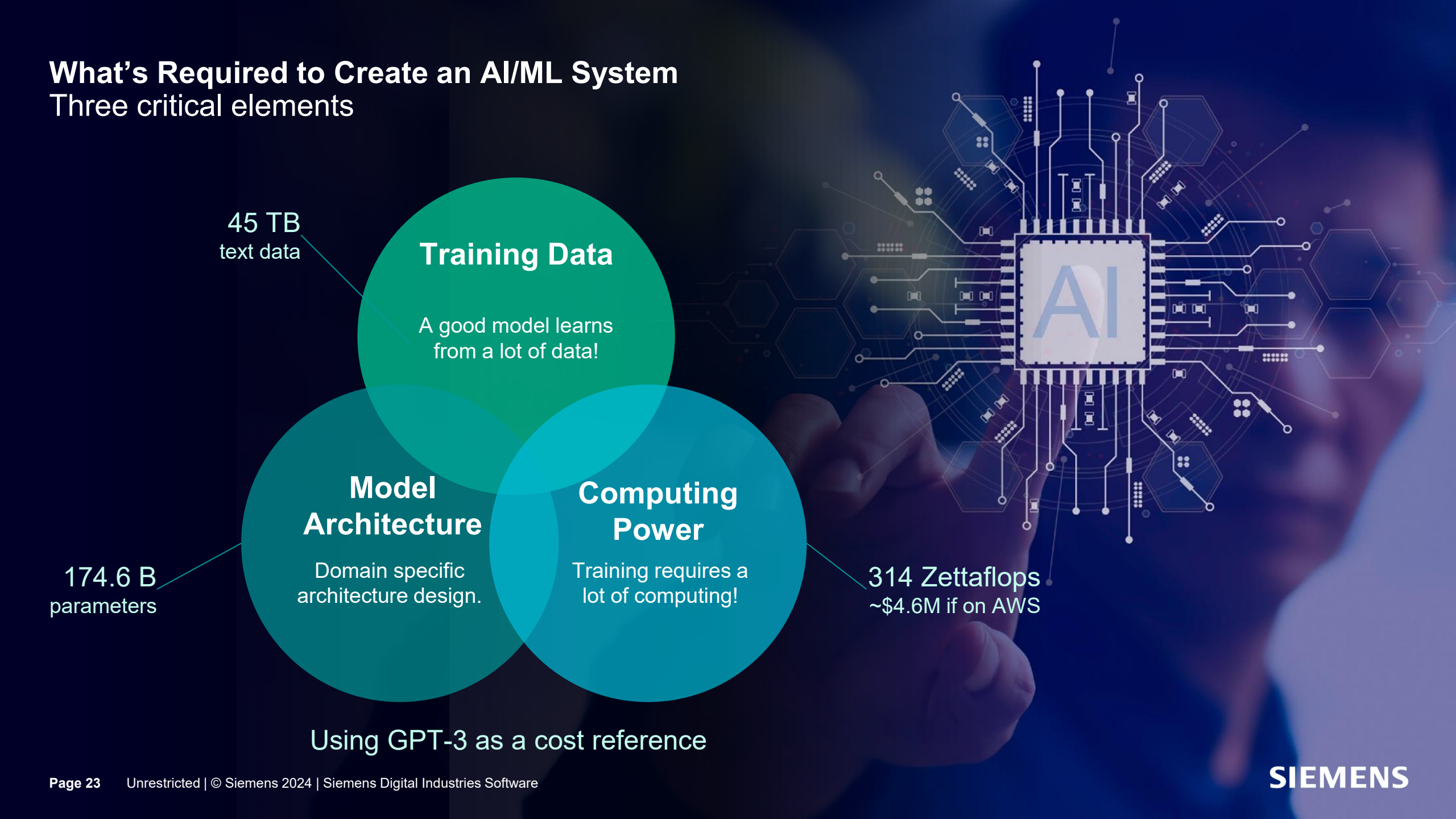
What's Required to Create an AI/ML System

Three critical elements



Using GPT-3 as a cost reference

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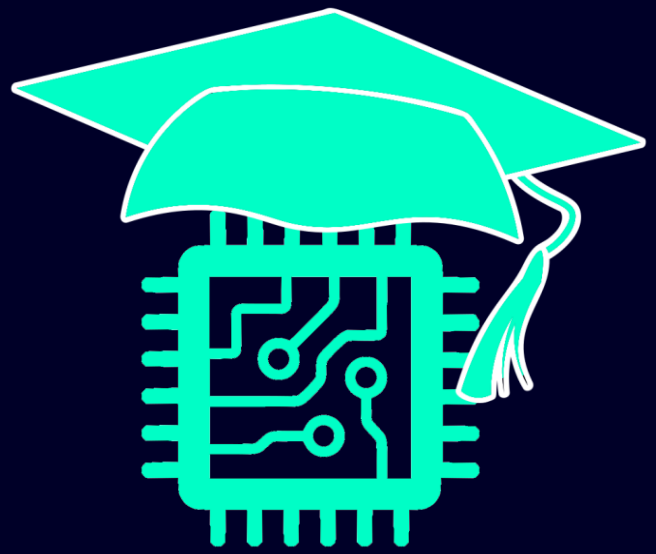
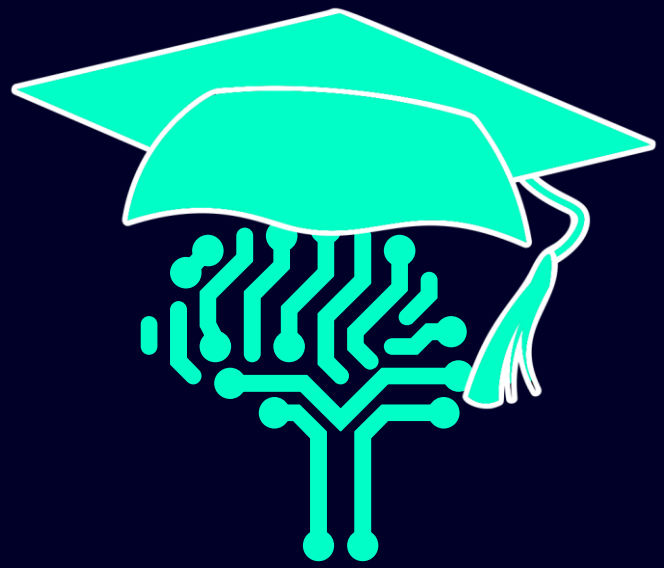
Unleashing AI for EDA
Requires Expertise and Relavent Data for Success



EDA Expertise

Data



AI Expertise

Source: DALL-E 3

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Siemens Three Track Approach to Data and ML Innovation

Building on the strength of the larger Siemens organization

Collaboration

Partners

- Earlier Adopter Customers
- Access to Real Project Datasets
- Introducing Early Requirements

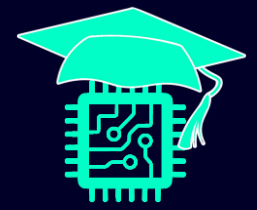
Siemens EDA

- IC and EDA Division Experts
- Open Source & Real Project Lifecycle Data
- AI and Data Science Central Group

Siemens Technology

- 1400+ AI Experts & 3700+ AI Patents
- Creating Verification Knowledge Graph
- Research on AI Approaches

Data



EDA Expertise

AI Expertise

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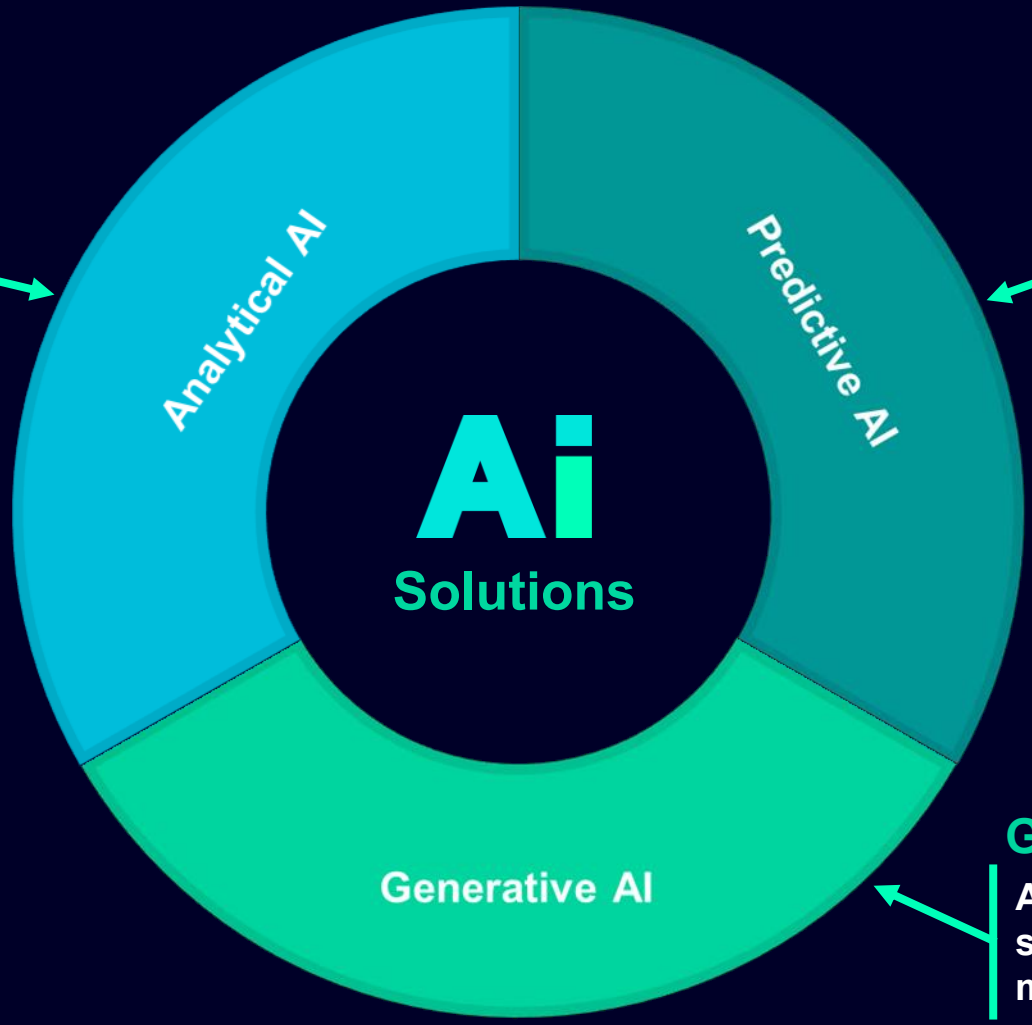
Three Primary Approaches to Using AI and Their Objectives

Analyze

Turning data into information and making rational decisions



Optimize

Identify patterns and predict future events based on historical data

Generate

Accelerate design creation, system optimization, and model abstraction

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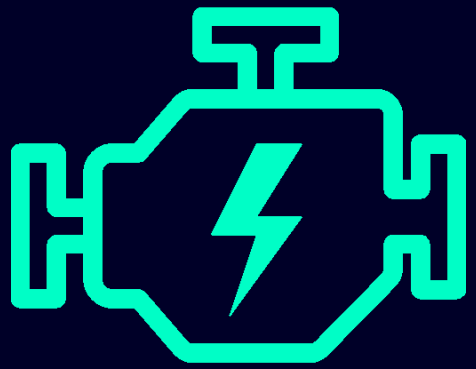
What Are the Opportunities?

A verification cycle is a non-renewable resource—make sure everyone you use is effective!

Faster Engines

Replacing heuristics and graph analytics in core engines & tools

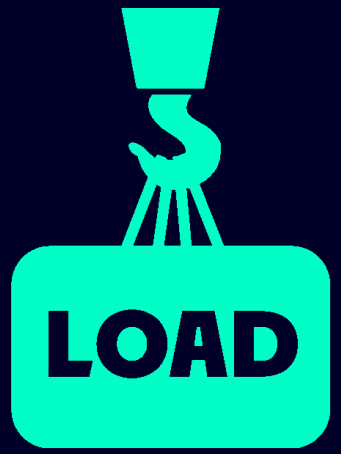


Faster Engineers

Enabling new creation, analysis and debug capabilities

Fewer Workloads

Predictive technologies to stream-line & accelerate verification



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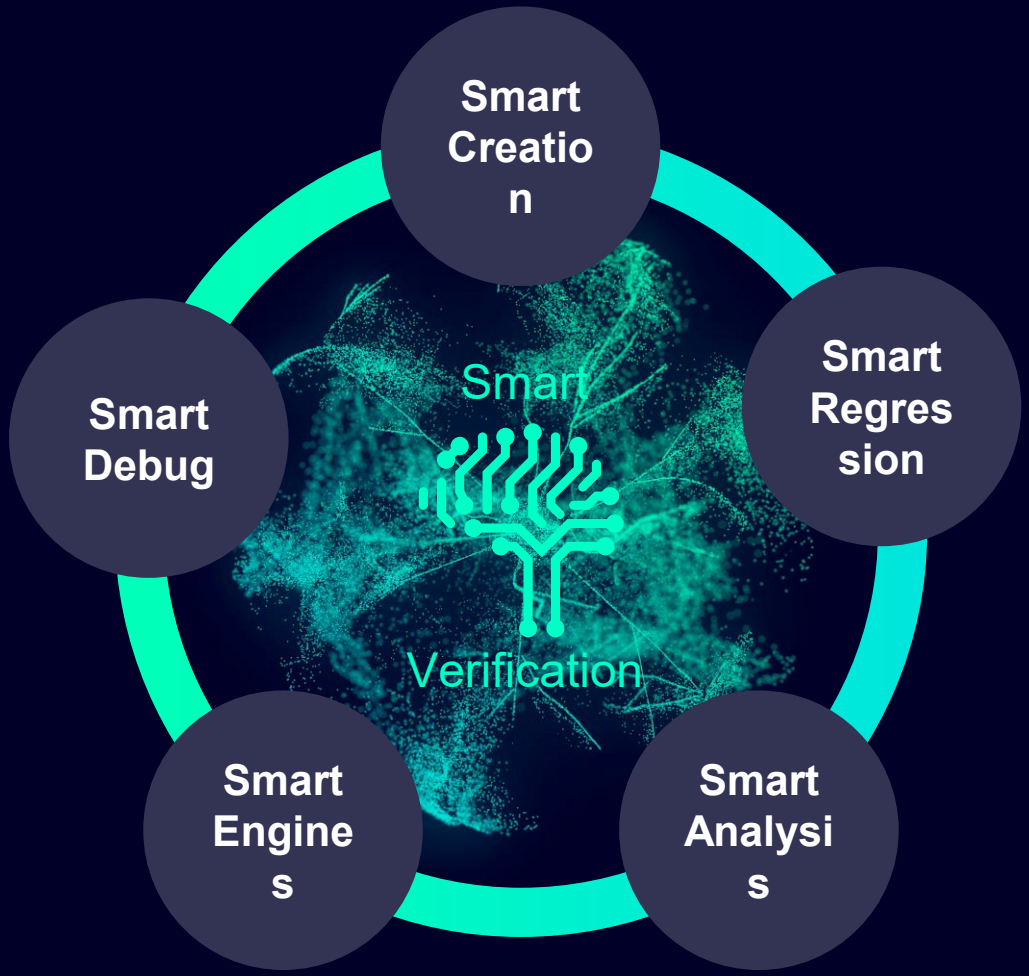
Smart Verification
Exploring potential opportunities for improving productivity



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Smart Creation
How can AI/ML assist us to ...

Faster Engineers

Code Generation

Finetuned LLM outperforms ChatGPT in niche language knowledge to generate RTL, UVM and PSS

Documentation Exploration

Natural language based service portal with detailed knowledge of all products to accelerate tool usage

Assertion Generation

Finetuned LLM enables the automatic generation of SVA to accelerate assertion based methodologies

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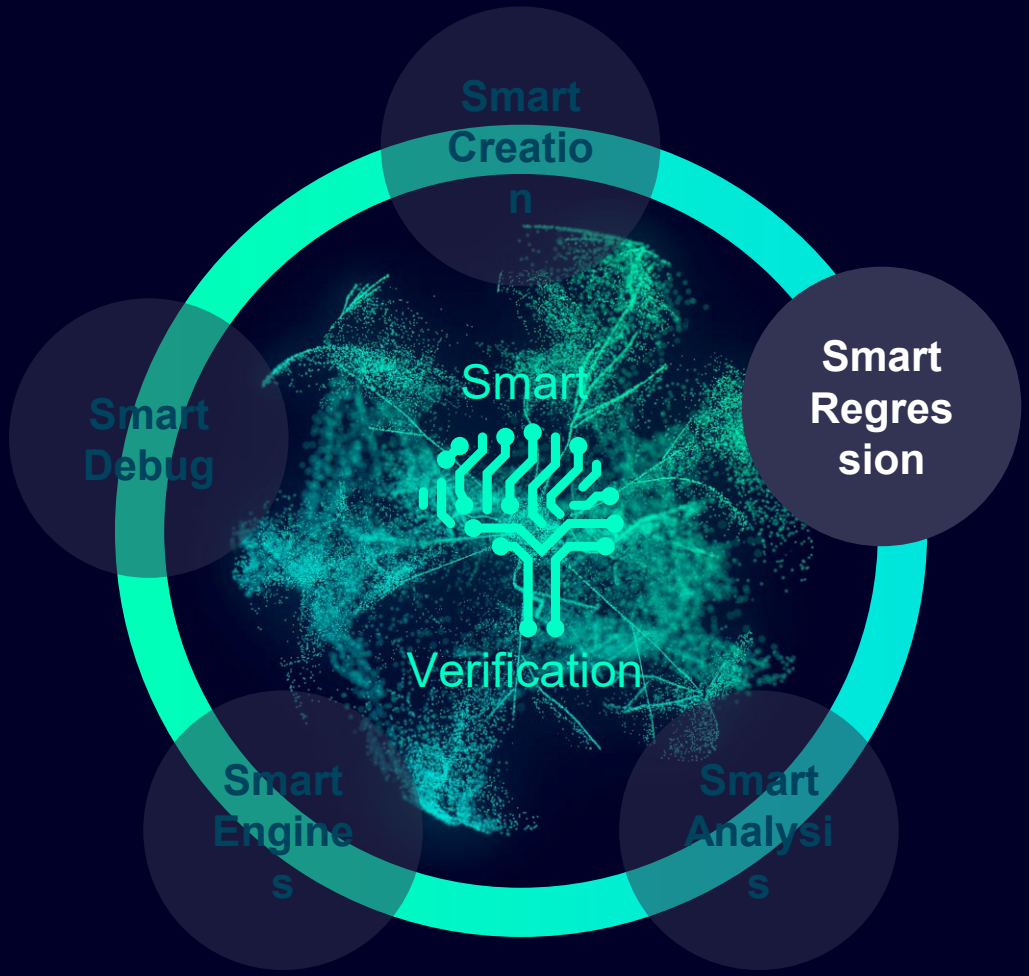
Smart Regression
Accelerating Regressions



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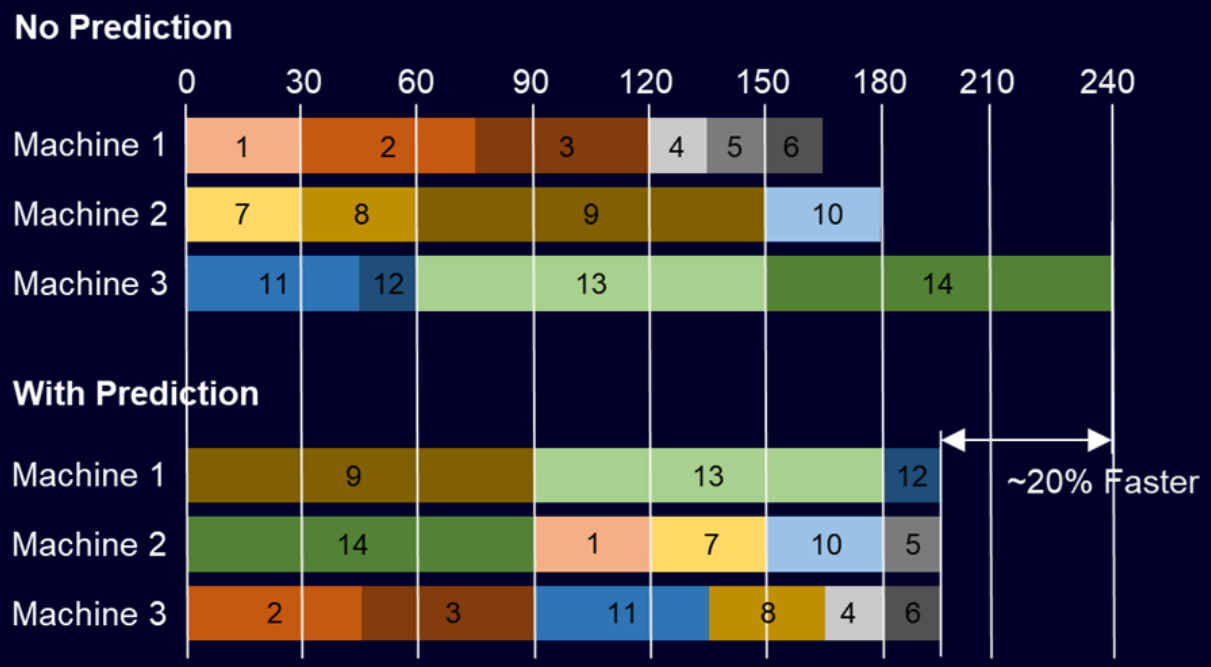
Smart Regression
How can AI/ML help ...

LOAD
Fewer
Workload



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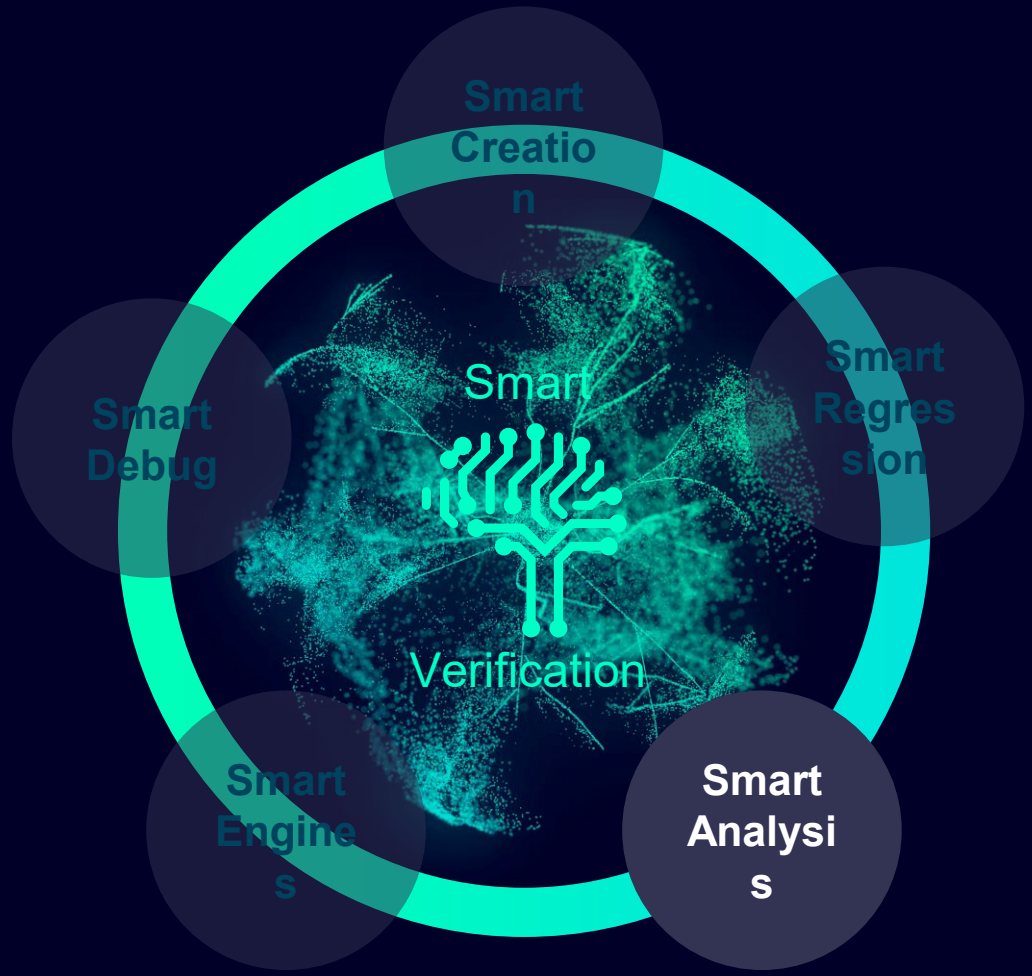
Smart Analysis
Accelerate Verification Analysis



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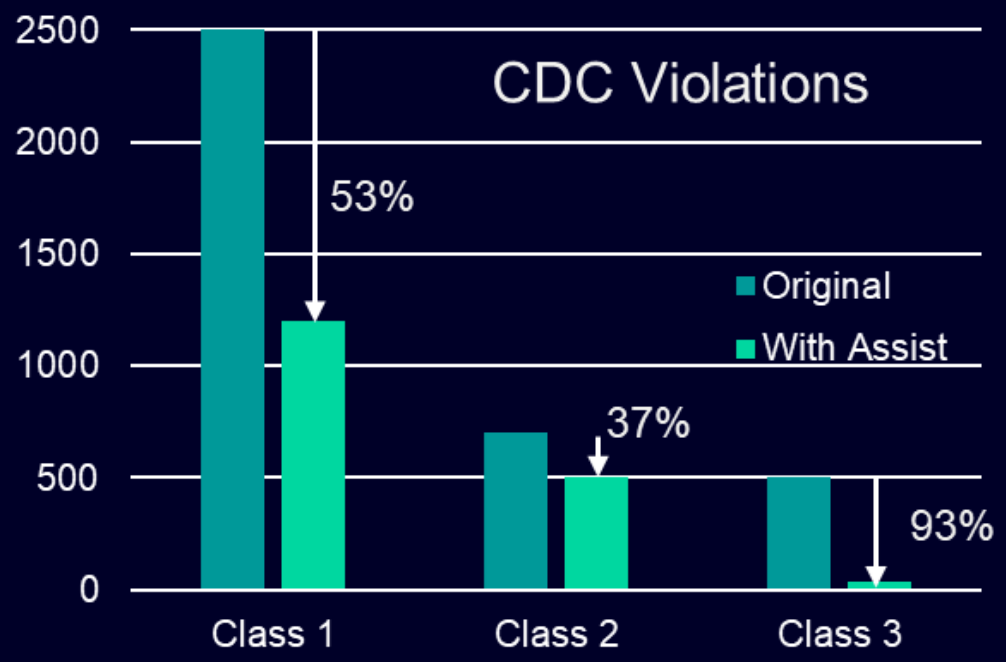
Smart Analysis
How can AI/ML help ...



Faster Engineers

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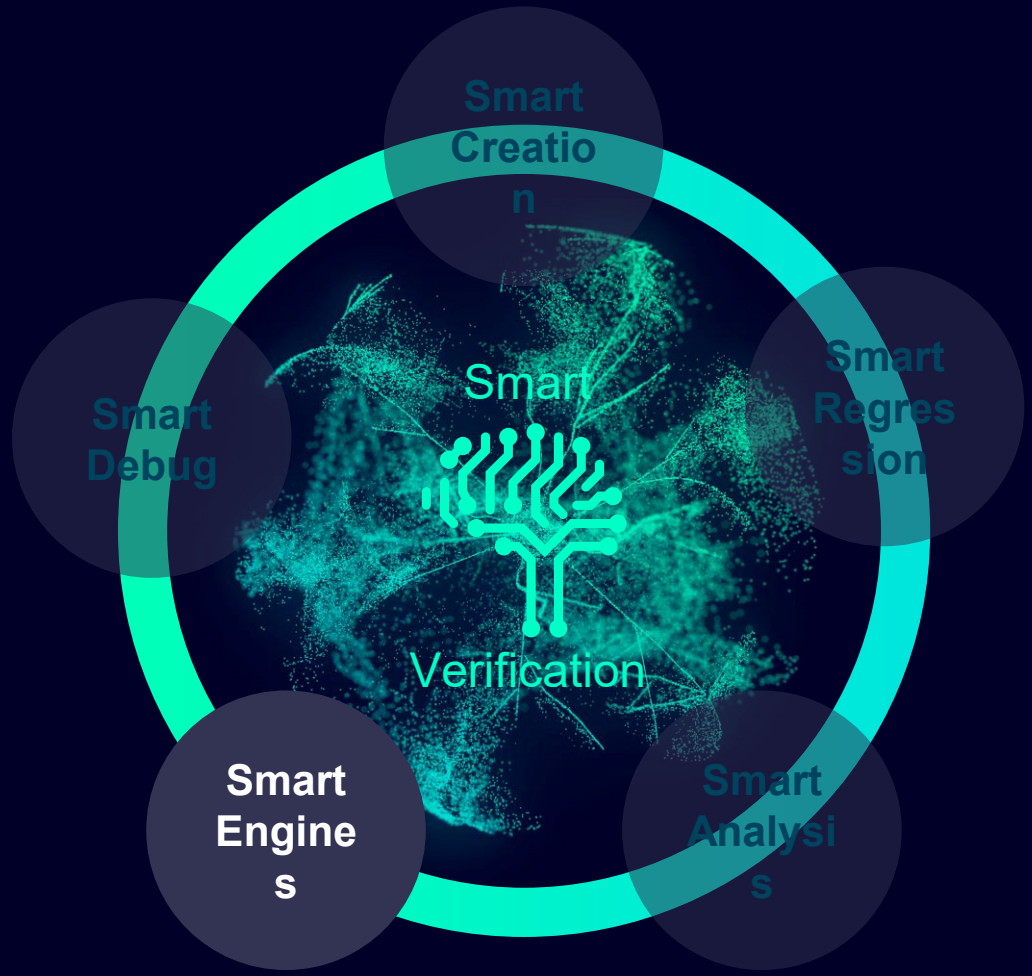
Smart Engines
Accelerate Verification Engines



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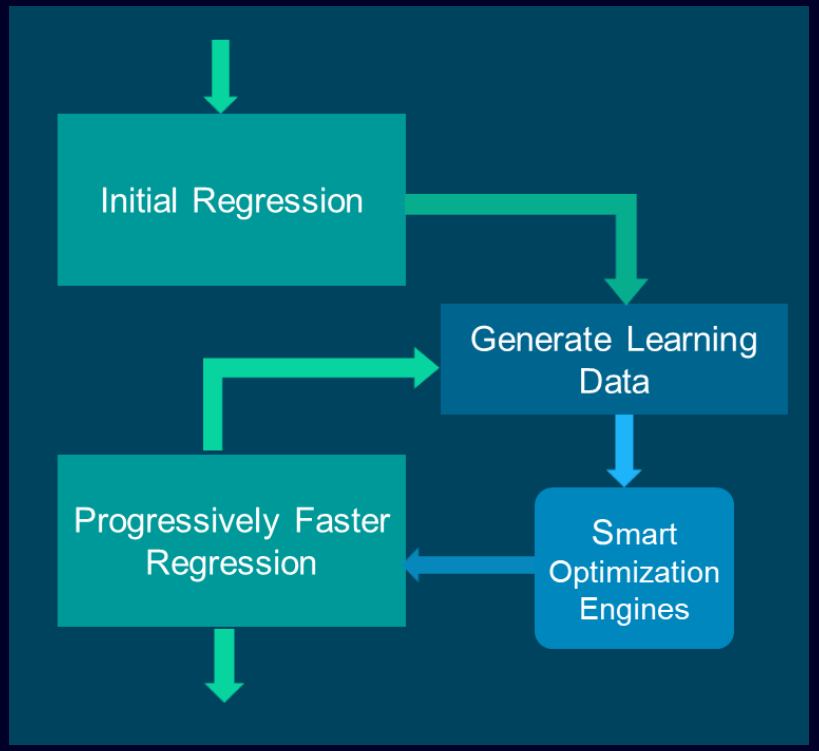
Smart Engines
How can AI/ML help ...

Faster Engineers



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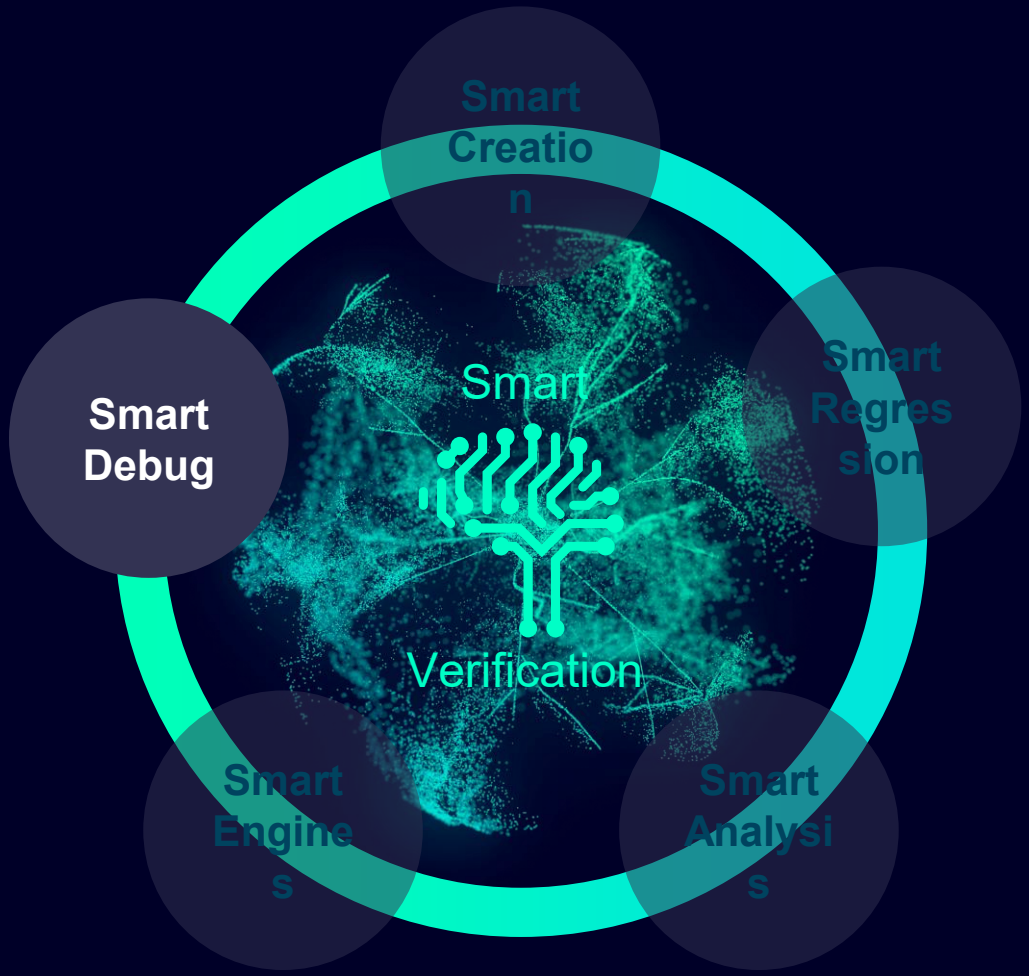
Smart Debug
Accelerate Debug Turn-around



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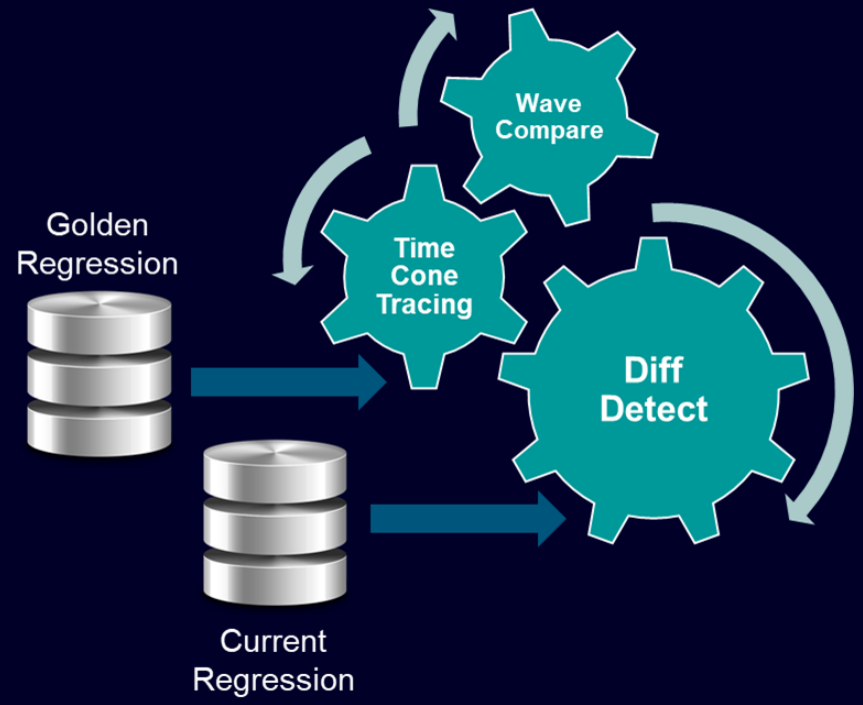
Smart Debug
How can AI/ML help ...

Faster Engineers



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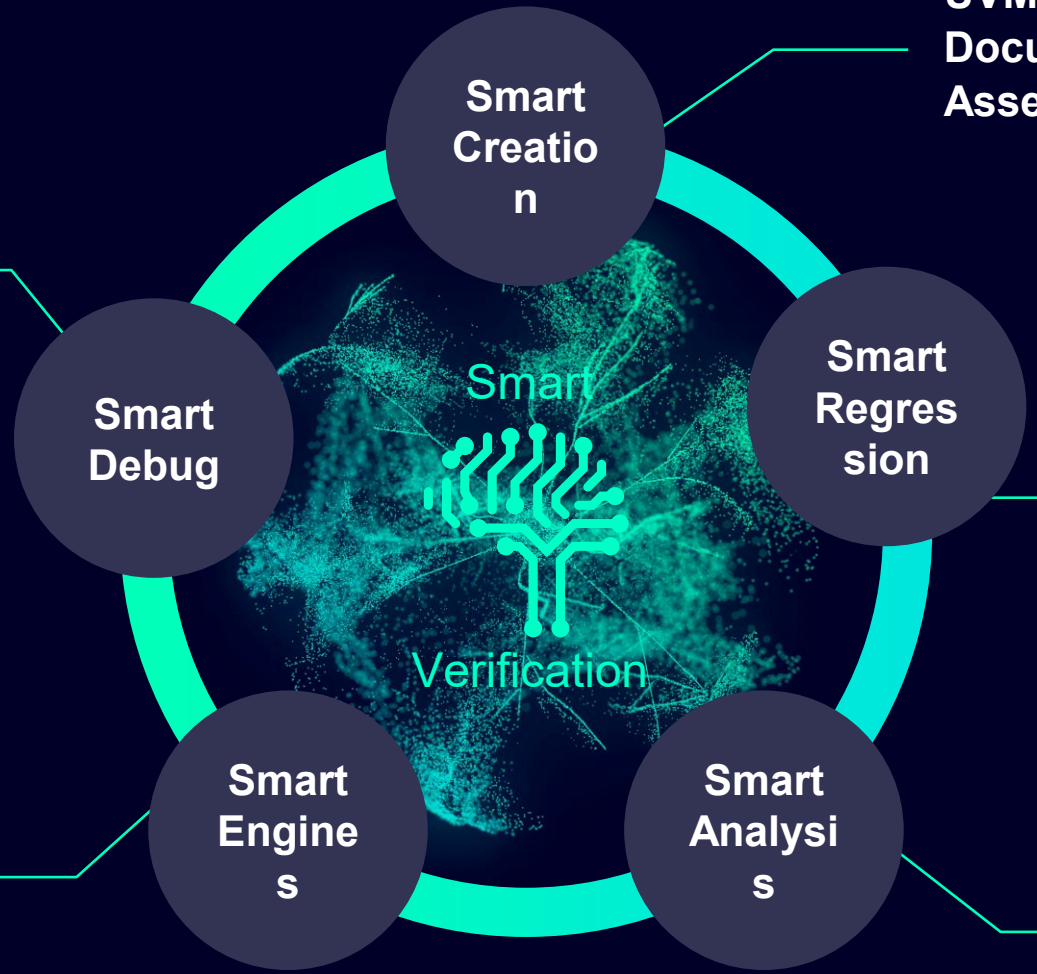
AI Opportunities Verification Productivity

Faster Engines, Faster Engineers and Fewer Workloads

Bad Commit Prediction
Failure Signature Prediction
Root Cause Prediction

UVM and PSS Generation
Documentation Exploration
Assertion Generation



Failure Prediction
Smoke-test Prediction
Schedule Prediction

Coverage Acceleration
Progressive Performance
Coverage Optimization

Pattern Analysis
Cross Hole Analysis
CDC/RDC Assist

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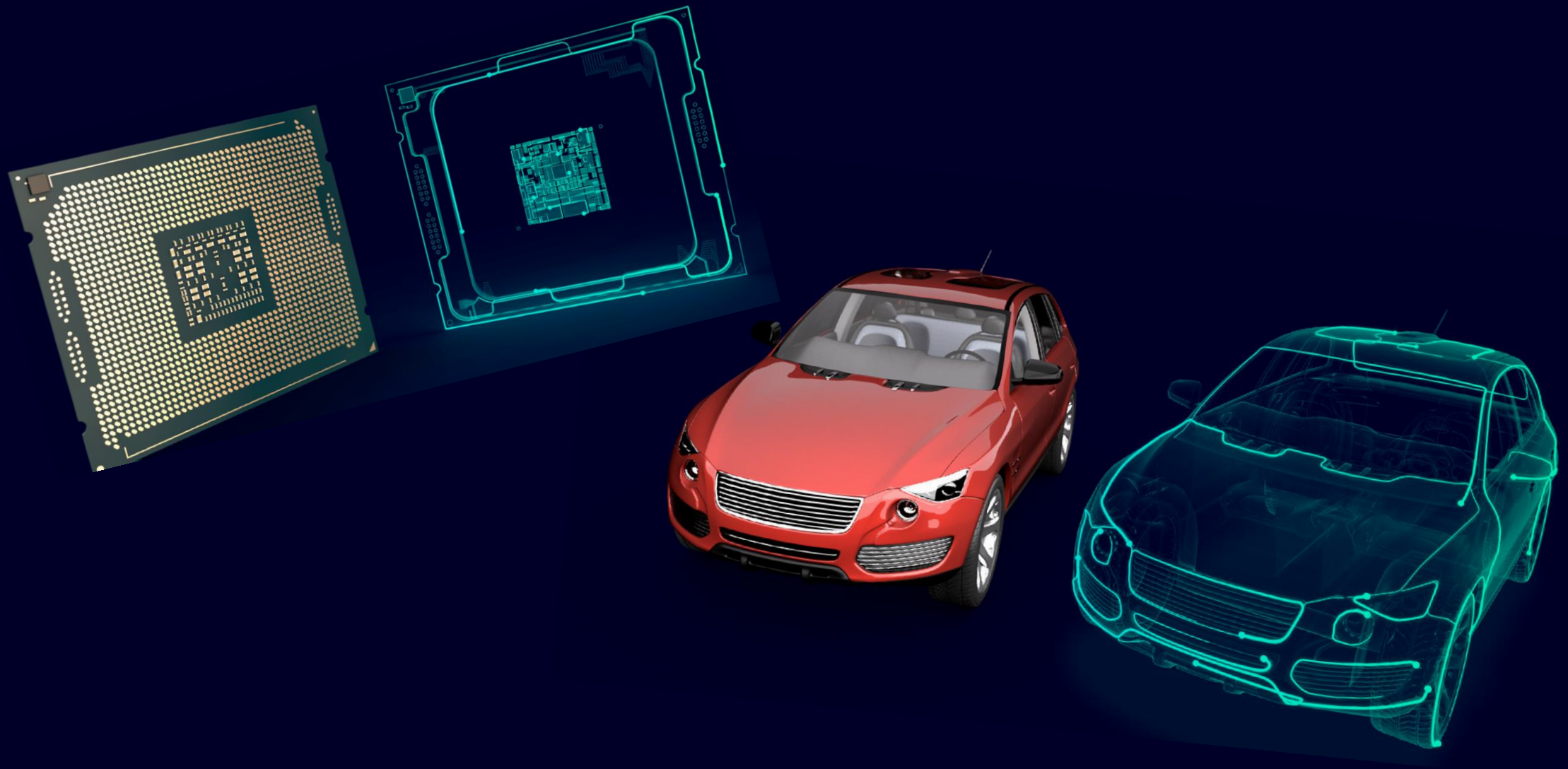
Software-Defined Products, and Design Productivity, and Digital Twins



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Digital Twins

Concept applied to the Apollo 13 Crisis, 1970

Term Digital Twin coined by Dr Michael Grieves 2002

NASA begin using Digital Twins explicitly in 2010

Siemens started focus on Digital Twins in 2012

EDA has been implementing partial Digital Twins for years

Today’s Digital Twins encompasses the entire product lifecycle

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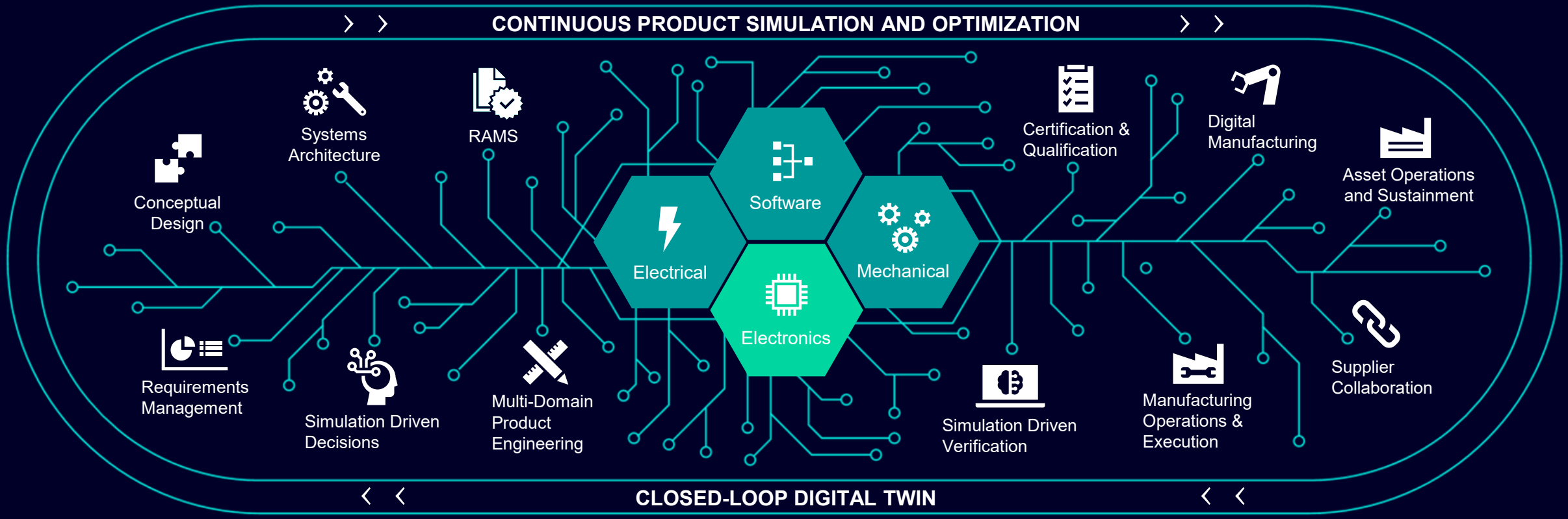
Digital Twins Bridge the Gap Between Physical and Digital Worlds

A critical component of software-defined products to meet complex demands



Real-time Monitoring, Continuous Improvement, Personalization, and Innovation

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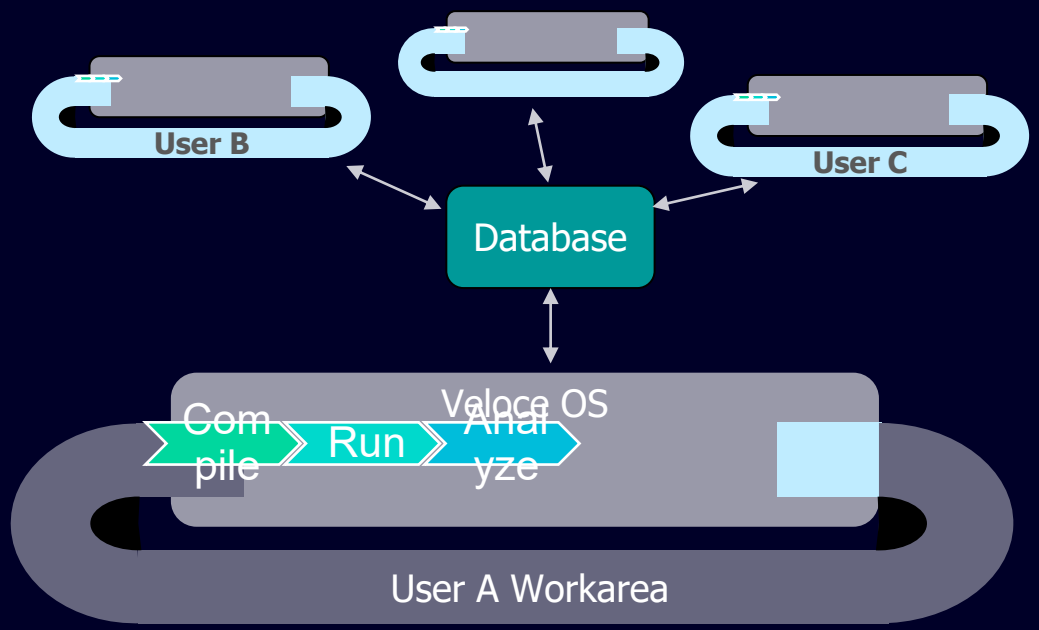
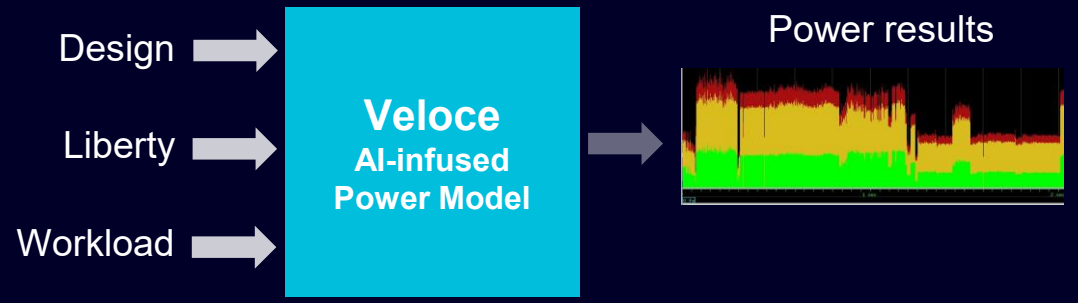
Veloce AI/ML Tools Empower Software-Defined Products & Digital Twins

Adaptive, efficient, and aligned with real-world conditions



- **AI-driven compile optimizers** streamlines the process of compiling a design for emulation
- **50% better** compile time (RTLC phase)
- **100x Increase** in runtime throughput



- **AI-enabled accurate and fast power profiles** for RTL designs, running real software workloads
- **3-5%** accuracy margin of power tools
- **200X** faster than traditional power estimation

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HLS Enables the Next Generation of Edge AI Accelerators

Unlocking design productivity with Catapult HLS

Accelerated Design Cycle Up to 4x Faster

- Transforms C++/SystemC models into optimized RTL

Higher Abstraction Level

- Simplifying complex system designs and enhancing productivity.

Automated Optimization

- Automatic pipelining, resource sharing, and power optimization.

Design Space Exploration

- Allows rapid exploration of multiple architectural options to find the optimal balance between performance, power, and area.

Improved Verification

- Enabling early validation and reducing verification bottlenecks.

Download Paper

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Bug prevention through HLL and HLS

15-50 Bugs per 1000 Lines of Code

100 lines of HLL is equivalent to 1000 lines of RTL

Expect a 10x reduction in the average number of bugs

1–5 bugs for HLL design vs. 15–50 bugs for equivalent RTL design

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Summary
Harnessing Collective Wisdom Across Tools, Processes, and People

AI is a means to achieve transformation, not an end in itself

Macro Trends

- Semiconductor transformation
- Data explosion changing everything
- Movement to Software Defined Products
- Decline in engineering talent demands smarter verification
- Sustainable solutions is no longer an option

Smart Verification

- Faster Engines, Faster Engineers, Fewer Workloads

Harnessing Collective Wisdom Across Tools, Processes, and People

The future of verification requires the key elements

Scalable Verification

Scaling verification of large, complex designs with solutions that accelerate closure and bring automation enabling teams to do more with less

- ► Acceleration
- ► Automation
- ► Cloud

Data-Driven Verification

Leveraging the power of data through analytics to bring new insights that improve productivity of debug and verification closure

- ► AI/ML
- ► Data mining
- ► Traceability

Connected Verification

Connecting users and tools to form a cohesive verification ecosystem for a comprehensive and seamless verification experience

- ► Inter-connected
- ► Collaborative
- ► Interoperable

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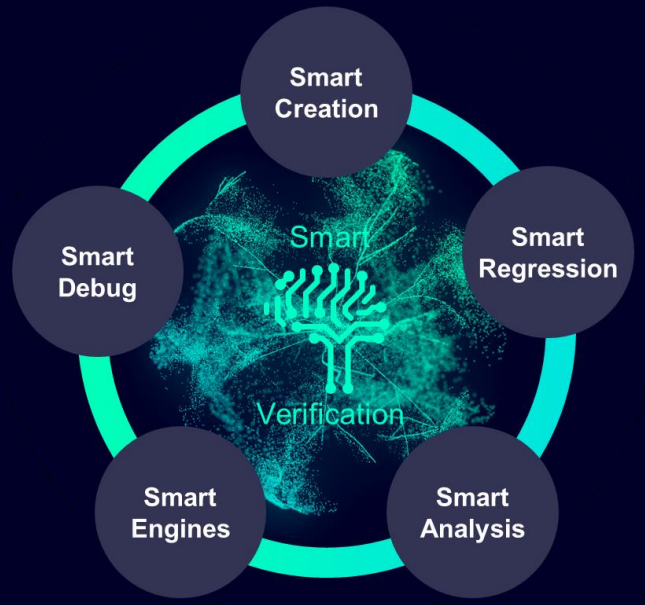
Is this stuff real?
Questa Smart Verification

Product	Technology	AI Value Observed
VIQ Coverage Analyzer	Pattern & Cross Hole Analysis	**3x** reduction in coverage closure time
CDC/RDC	CDC/RDC Assist	**90%** reduction in crossing violations
VIQ Regression IQ	Failure Prediction	**100x** faster to find first failure and **2x** faster to find last failure
	Smoke Test Prediction	**10x** reduction in smoke test regression time
VIQ Debug IQ	Bad Commit Prediction	**2x** reduction to find and confirm bad check-ins
	Signature Prediction	**30%** reduction in overall debug time
Questa Sim	Coverage Acceleration	**100x** faster time to coverage closure with **500x** fewer tests



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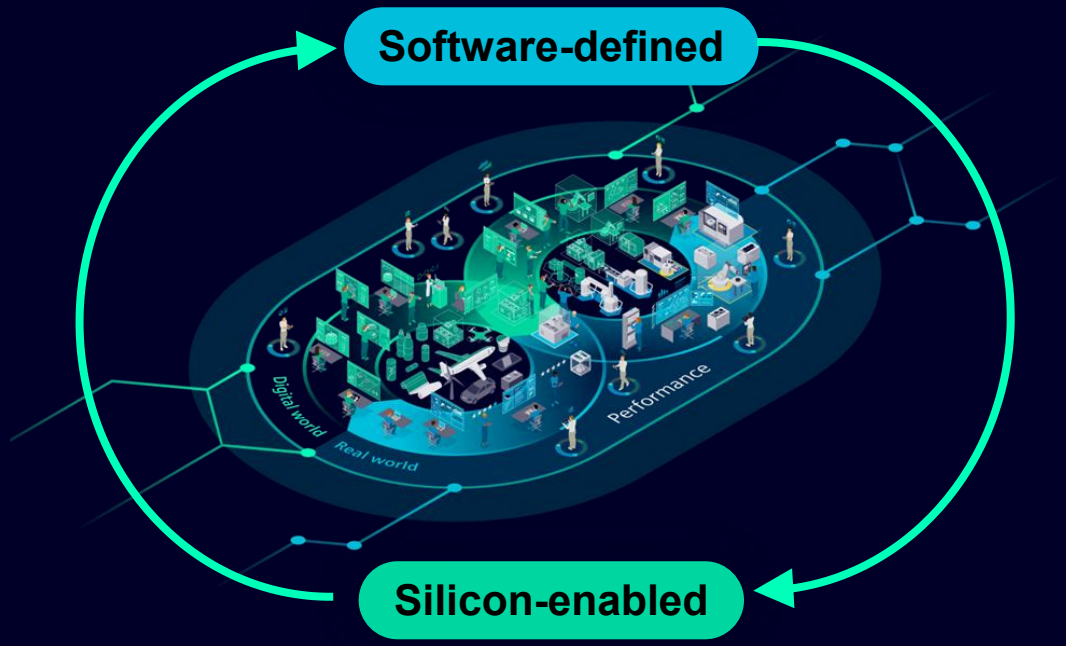
Harnessing Collective Wisdom Across Tools, Processes and People

Referenced AI/ML papers



DVCon US **2023** Paper

DVCon US **2024** Paper

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