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A Comparative Study of CHISEL and SystemVerilog, Based on Logical Equivalent SweRV-EL2 RISC-V Core

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Presentation overview

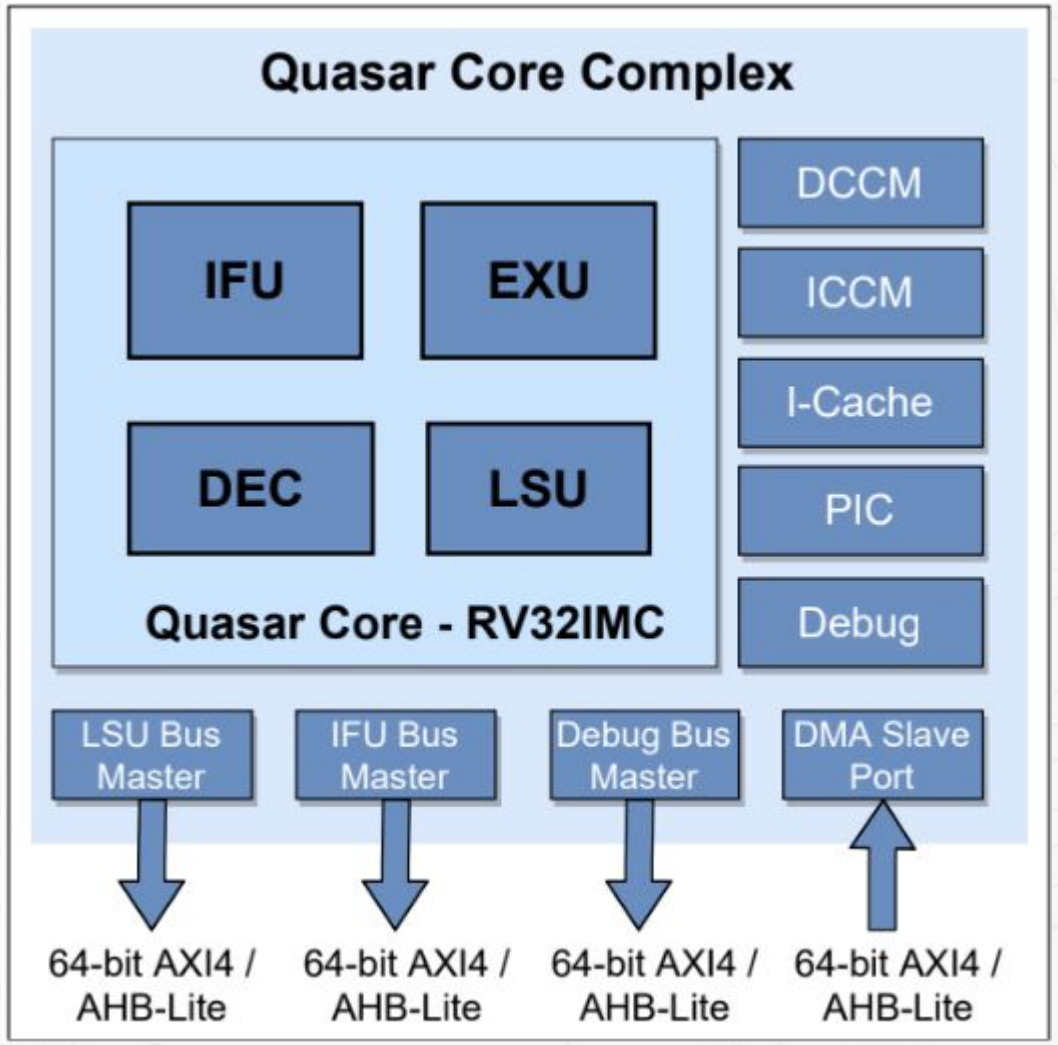
- The presenter will be covering following points:
  - Introduction to the paper
  - Micro Architecture of Quasar core
    - An open source CHISEL based SweRV-EL2 equivalent core
  - Methodology adopted for this paper
    - Verification
  - Results
  - Useful links

Introduction to Quasar project

- A comparative analysis between CHISEL & SystemVerilog is done
  - The design chosen for this comparative analysis is SweRV-EL2 (SweRV-EL2 is a 4-stage pipelined open-source RISCV based core by Western Digital Corporation)
- The logical equivalent CHISEL implementation of SweRV-EL2 is named Quasar
- After logical equivalent check between SweRV-EL2 RTL & CHISEL generated Quasar RTL, the following parameters have been compared
  - Max frequency
  - Area
  - Dynamic power
  - Code maintenance & readability

Micro Architecture of Quasar

- Quasar is a 4-stage pipelined core
- The core supports RV32IMC instruction-set
- The code is parameterized for major blocks
  - Branch-Predictor size
  - Store-buffer size
  - Bus-Buffer size
  - Configuration for AXI-4 or AHB
  - Configuration for ICCM/I-Cache/DCCM



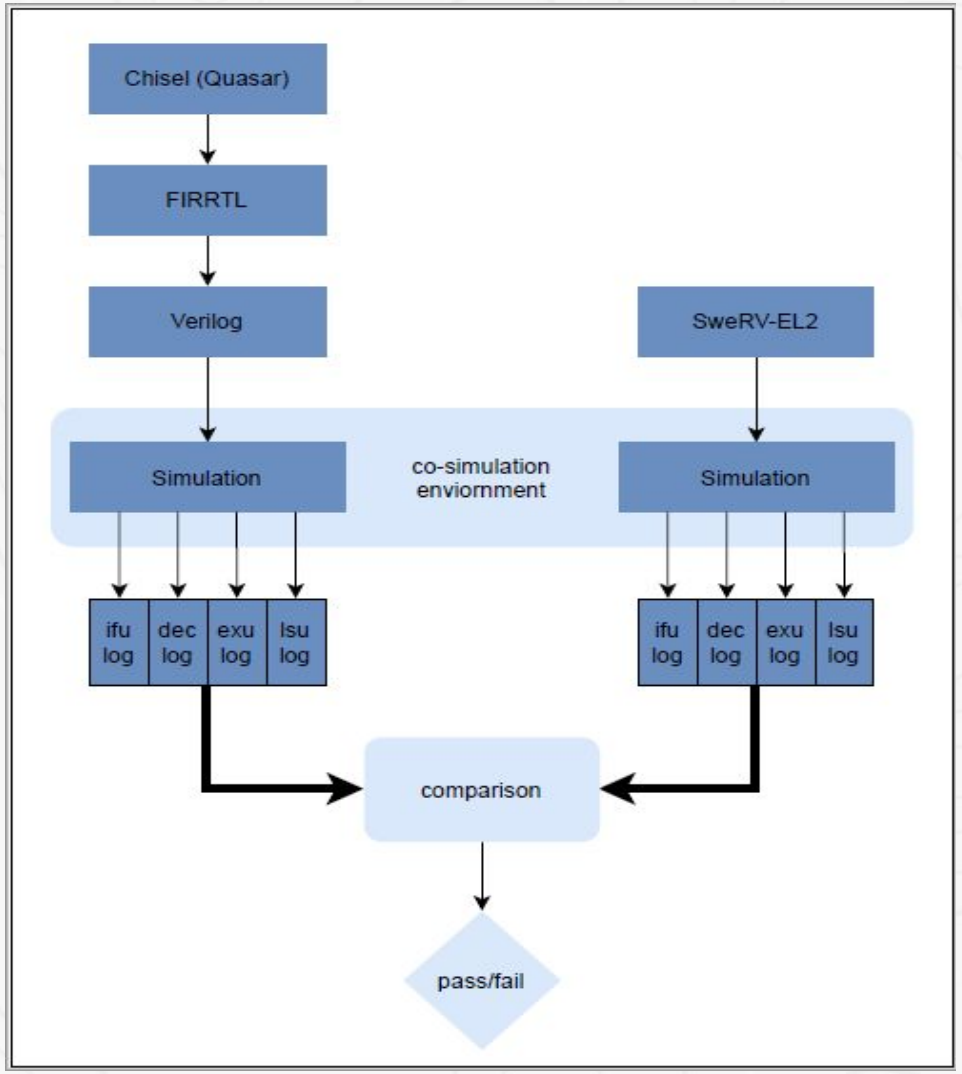
Methodology

The development of Quasar is divided into 4-major parts

1. Comprehending the Microarchitecture of SweRV-EL2
    a. This lead to compilation of MAS(Micro Architecture Specification) document
2. Implementation in CHISEL
3. Verification of CHISEL generated verilog
    a. Verification methodology consists of two phases
        i. Co-Simulation
        ii. LEC
    b. The verification using the traditional method would add much time constraint to the completion of the project
    c. It was evaluated to do a LEC RTL/RTL on both the implementations, to decease completing time
    d. For LEC, SweRV-EL2 is used as golden reference model

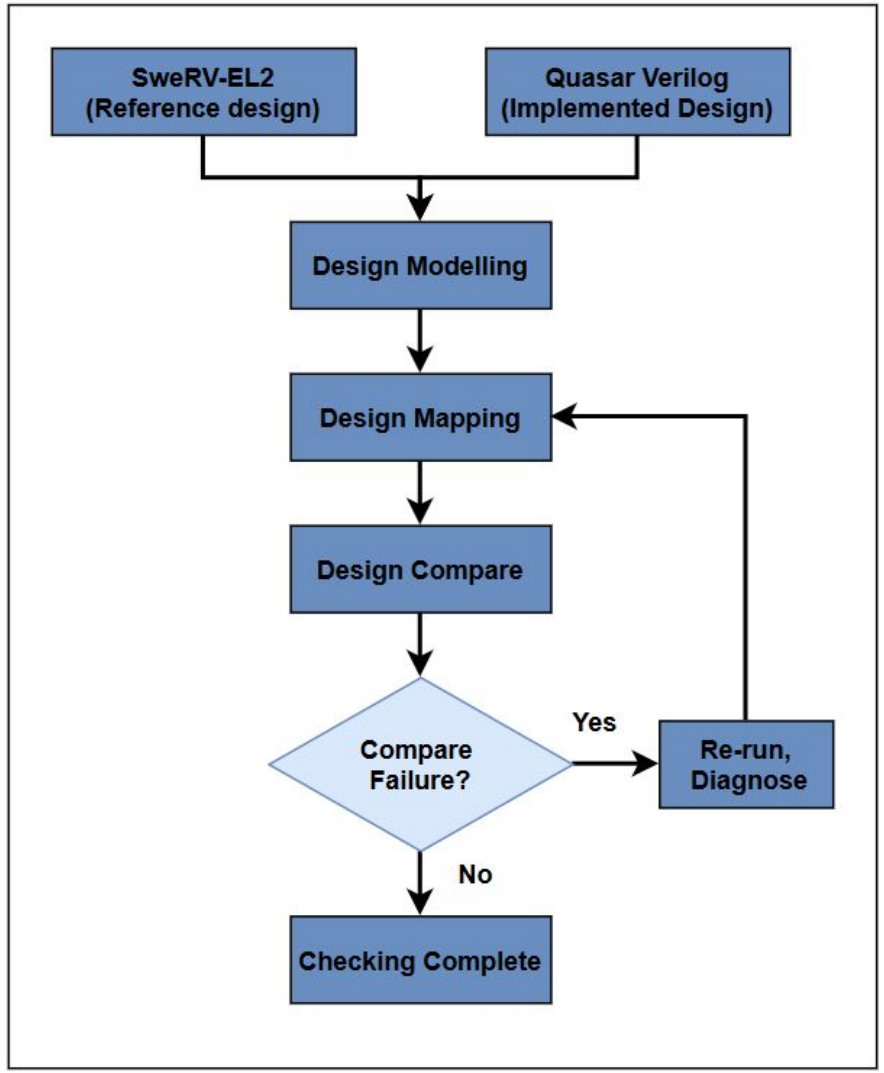
Verification (Co-Simulation)

- It was evaluated that to increase coverage beyond 90% much work is needed, so the team moved towards LEC rather than pursuing tradition verification
- For co-simulation verification, a simple test-environment was created which compared the post simulation logs of both cores



Verification (LEC)

- After Co-simulation verification both the cores were subjected to LEC using Synopsys Formality tool
- As the core can have multiple configuration, so LEC was performed on basic & high performance configurations
- As the CHISEL generated RTL had signals with name conversion, so a total of 15,000+ user matched had to be done



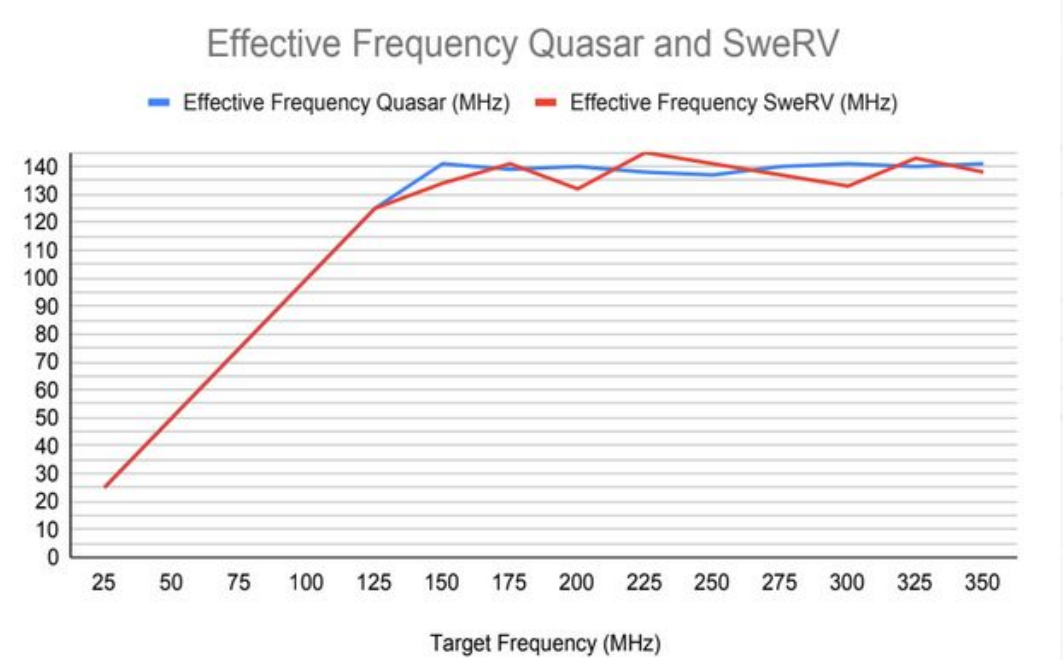
Results

- Both the implementations (SweRV-EL2 & Quasar) were subjected to frequency sweep on 130nm SkyWater-PDK
- As discussed above 4-major key matrices were analyzed
  - Maximum frequency
  - Silicon area
  - Dynamic power
  - Code maintenance & readability
    - Lines of code
    - Readability of code

Results Con’t

These results shows SweRV-EL2 is about 2.7% better in frequency with respect to Quasar

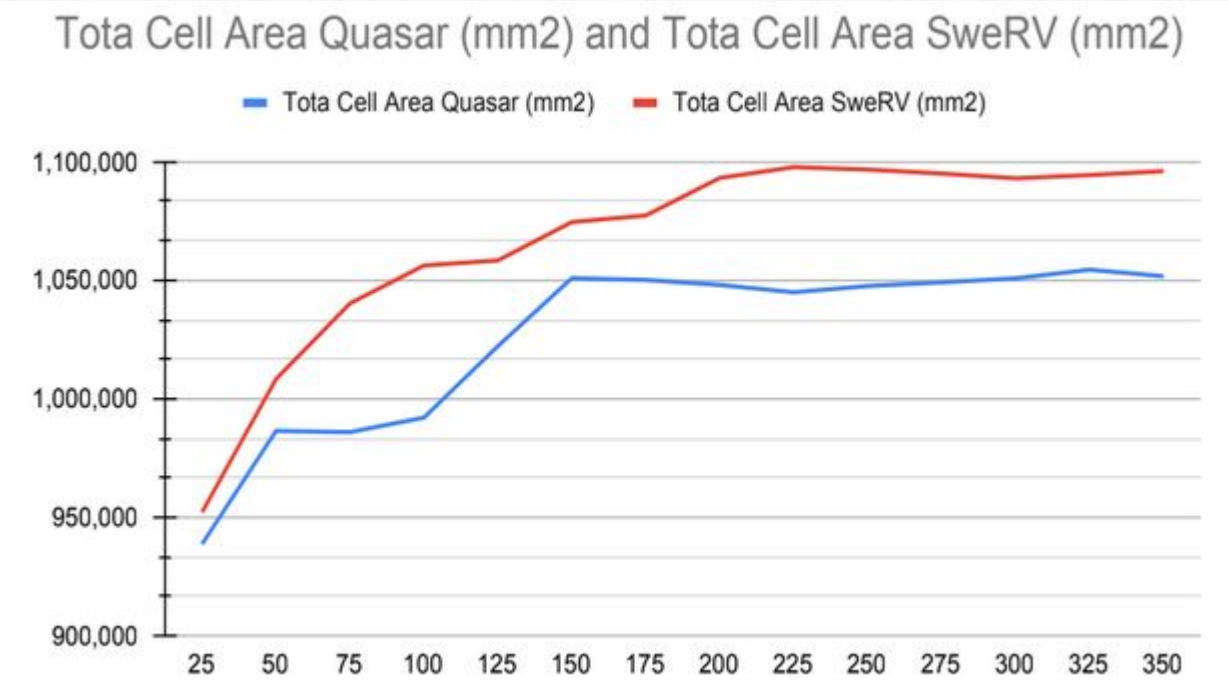
Target Frequency (MHz)	Effective Frequency	
	Quasar (MHz)	*SweRV (MHz)*
25	25	25
50	50	50
75	75	75
100	100	100
125	125	125
150	141	134
175	139	141
200	140	132
225	138	145
250	137	141
275	140	137
300	141	133
325	140	143
350	141	138



Results Con’t

Results show that Quasar is 4.2% smaller in area relative to SweRV-EL2’s area

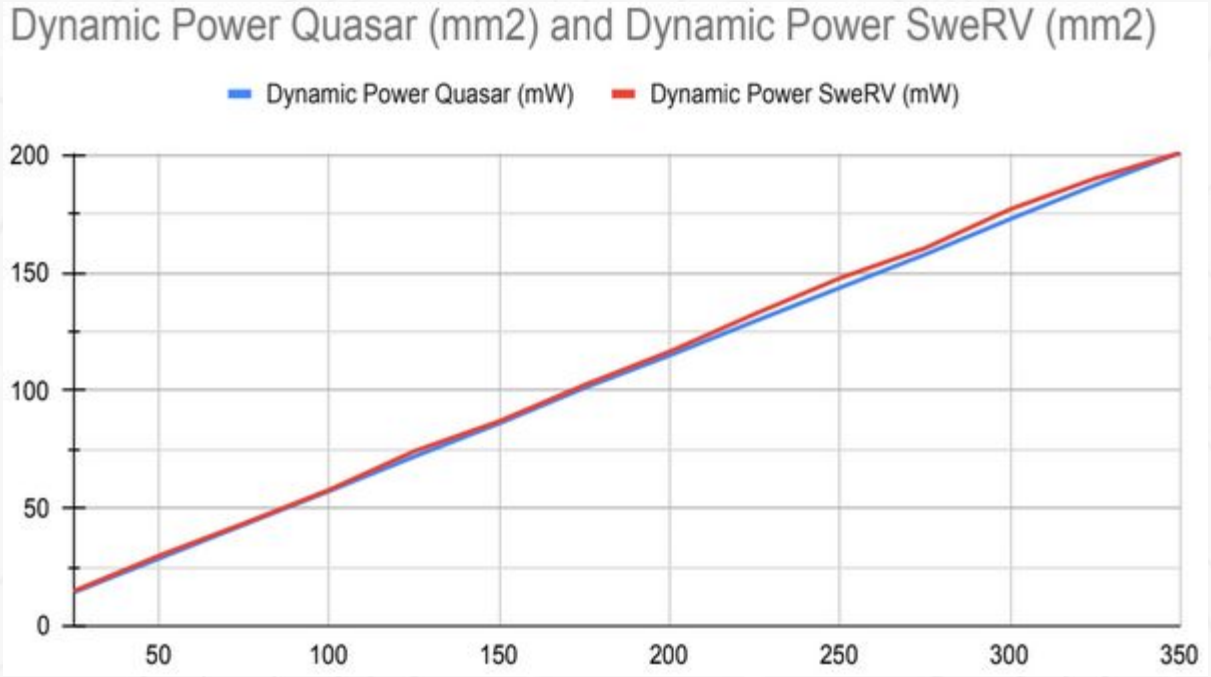
Target Frequency (MHz)	Total Cell Area	
	Quasar (um^2)	*SweRV* (um^2)
25	938,648	952,117
50	986,381	1,008,292
75	985,884	1,040,223
100	992,014	1,056,209
125	1,022,198	1,058,341
150	1,050,860	1,074,543
175	1,050,117	1,077,312
200	1,048,001	1,093,162
225	1,044,916	1,097,709
250	1,047,533	1,096,681
275	1,049,092	1,095,016
300	1,050,784	1,093,012
325	1,054,411	1,094,366
350	1,051,685	1,096,023



Results Con’t

On account of dynamic power, Quasar is 3.8% better in power at maximum operating frequency relative to SweRV-EL2

Target Frequency (MHz)	Dynamic Power	
	Quasar (mW)	*SweRV (mW)*
25	14.32	14.87
50	28.66	29.87
75	43.07	43.60
100	57.33	57.85
125	71.99	74.27
150	86.11	87.03
175	101.19	102.41
200	114.97	116.60
225	129.49	132.57
250	143.70	147.78
275	157.83	160.52
300	172.89	177.03
325	187.33	190.15
350	201.05	201.05



Results Con’t

Finally coming down to Qualitative results

- Number of lines of code
  - It is calculated that the number of lines of code written for Quasar is about 35-40% less as compared to that for SweRV-EL2
- Readability of code
  - The readability of code for Quasar is subdivided into 2-parts
    - Readability of CHISEL
      - For a person well-versed in CHISEL it is assumed that the readability of CHISEL code is much easier as the code-based is written at higher abstraction level
    - Readability of verilog generated from CHISEL

Conclusion

- From the results accumulated it is observed that CHISEL and SystemVerilog implementations are relatively equal on accounts of PPA as a whole
- The CHISEL community is not well diverse compared to SystemVerilog, so there is little support available for CHISEL on publicly accessible networks.
- The majority of the semiconductor vendors are still using SystemVerilog for developing chips and tools, So there is a need to convert the CHISEL to Verilog for verification purposes
  - This is the major bottleneck because the verification task involves more steps of conversions
  - These conversions are not needed when the code is written in SystemVerilog. The CHISEL community needs to develop its own verification tools to exploit CHISEL to its fullest potential.

Useful links

Quasar is an open-source code base and can be found at:

https://github.com/Lampro-Mellon/Quasar

A comprehensive CHISEL learning manual was also written by some members of the team, which can be found at:

https://github.com/Lampro-Mellon/Chisel-Training

Questions

Finally I welcome all to ask any questions regarding this presentation

Thanks