A Comparative Study of CHISEL and SystemVerilog, Based on Logical Equivalent SweRV-EL2 RISC-V Core

Junaid Ahmed, Waleed Bin Ehsan, Laraib Khan, Asad Aleem, Agha Ali Zeb, Sarmad Paracha, Abdul Hameed Akram, Aashir Ahsan
Presentation overview

• The presenter will be covering following points:
  • Introduction to the paper
  • Micro Architecture of Quasar core
    • An open source CHISEL based SweRV-EL2 equivalent core
  • Methodology adopted for this paper
    • Verification
  • Results
  • Useful links
Introduction to Quasar project

• A comparative analysis between CHISEL & SystemVerilog is done
  • The design chosen for this comparative analysis is SweRV-EL2 (SweRV-EL2 is a 4-stage pipelined open-source RISC-V based core by Western Digital Corporation)
  • The logical equivalent CHISEL implementation of SweRV-EL2 is named Quasar
  • After logical equivalent check between SweRV-EL2 RTL & CHISEL generated Quasar RTL, the following parameters have been compared
    • Max frequency
    • Area
    • Dynamic power
    • Code maintenance & readability
Micro Architecture of Quasar

- Quasar is a 4-stage pipelined core
- The core supports RV32IMC instruction-set
- The code is parameterized for major blocks
  - Branch-Predictor size
  - Store-buffer size
  - Bus-Buffer size
  - Configuration for AXI-4 or AHB
  - Configuration for ICCM/I-Cache/DCCM
Methodology

The development of Quasar is divided into 4-major parts
1. Comprehending the Microarchitecture of SweRV-EL2
   a. This lead to compilation of MAS(Micro Architecture Specification) document
2. Implementation in CHISEL
3. Verification of CHISEL generated verilog
   a. Verification methodology consists of two phases
      i. Co-Simulation
      ii. LEC
   b. The verification using the traditional method would add much time constraint to the completion of the project
   c. It was evaluated to do a LEC RTL/RTL on both the implementations, to decease completing time
   d. For LEC, SweRV-EL2 is used as golden reference model
Verification (Co-Simulation)

• It was evaluated that to increase coverage beyond 90% much work is needed, so the team moved towards LEC rather than pursuing tradition verification

• For co-simulation verification, a simple test-environment was created which compared the post simulation logs of both cores
Verification (LEC)

- After Co-simulation verification both the cores were subjected to LEC using Synopsys Formality tool
- As the core can have multiple configuration, so LEC was performed on basic & high performance configurations
- As the CHISEL generated RTL had signals with name conversion, so a total of 15,000+ user matched had to be done
Results

- Both the implementations (SweRV-EL2 & Quasar) were subjected to frequency sweep on 130nm SkyWater-PDK
- As discussed above 4-major key matrices were analyzed
  - Maximum frequency
  - Silicon area
  - Dynamic power
  - Code maintenance & readability
    - Lines of code
    - Readability of code
These results show SweRV-EL2 is about 2.7% better in frequency with respect to Quasar.
Results Con’t

Results show that Quasar is 4.2% smaller in area relative to SweRV-EL2’s area.

<table>
<thead>
<tr>
<th>Target Frequency (MHz)</th>
<th>Total Cell Area Quasar (um²)</th>
<th>SweRV (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>938.648</td>
<td>952.117</td>
</tr>
<tr>
<td>50</td>
<td>986.381</td>
<td>1,008.292</td>
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<tr>
<td>75</td>
<td>985.884</td>
<td>1,040.223</td>
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<tr>
<td>100</td>
<td>992.014</td>
<td>1,056.209</td>
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<tr>
<td>125</td>
<td>1,022.198</td>
<td>1,058.341</td>
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<td>150</td>
<td>1,050.860</td>
<td>1,074.543</td>
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<td>175</td>
<td>1,050.117</td>
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<td>1,047.533</td>
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<td>1,094.366</td>
</tr>
<tr>
<td>350</td>
<td>1,051.685</td>
<td>1,096.023</td>
</tr>
</tbody>
</table>

Tota Cell Area Quasar (mm2) and Tota Cell Area SweRV (mm2)
Results Con’t

On account of dynamic power, Quasar is 3.8% better in power at maximum operating frequency relative to SweRV-EL2
Finally coming down to Qualitative results

- **Number of lines of code**
  - It is calculated that the number of lines of code written for Quasar is about 35-40% less as compared to that for SweRV-EL2

- **Readability of code**
  - The readability of code for Quasar is subdivided into 2-parts
    - Readability of CHISEL
      - For a person well-versed in CHISEL it is assumed that the readability of CHISEL code is much easier as the code-based is written at higher abstraction level
    - Readability of verilog generated from CHISEL
Conclusion

- From the results accumulated it is observed that CHISEL and SystemVerilog implementations are relatively equal on accounts of PPA as a whole.
- The CHISEL community is not well diverse compared to SystemVerilog, so there is little support available for CHISEL on publicly accessible networks.
- The majority of the semiconductor vendors are still using SystemVerilog for developing chips and tools, So there is a need to convert the CHISEL to Verilog for verification purposes.
  - This is the major bottleneck because the verification task involves more steps of conversions.
  - These conversions are not needed when the code is written in SystemVerilog. The CHISEL community needs to develop its own verification tools to exploit CHISEL to its fullest potential.
Useful links

Quasar is an open-source code base and can be found at:
https://github.com/Lampro-Mellon/Quasar

A comprehensive CHISEL learning manual was also written by some members of the team, which can be found at:
https://github.com/Lampro-Mellon/Chisel-Training
Questions

Finally I welcome all to ask any questions regarding this presentation

Thanks