

# Effective Design Verification – Constrained Random with Python and Cocotb

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**Abstract** —Being the most widely used language across the world due to its simplicity and with 35 keywords (v3.7), Python attracts both hardware and software engineers. Python-based verification environment leverages open-source libraries such as *cocotb* and *cocotb-coverage* that enables interfacing the testbenches with any available simulator and facilitating constrained randomization, coverage respectively. These libraries significantly ease the development of testbenches and have the potential to reduce the setup cost. The goal of this paper is to assess the effectiveness of a Python-Cocotb verification setup with design IPs and compare its features and performance metrics with the current de-facto hardware verification language i.e., SystemVerilog [1].

**Keywords** —*cocotb; python; constrained random; functional verification; coverage; hardware verification language*

## I. INTRODUCTION

With the conclusion of Dennard scaling [2] and the deceleration of Moore's law [3], the design of System-on-Chip (SoC) has become increasingly challenging. As the transistor size is shrinking at a remarkable rate, the total count of transistors in a chip has increased exponentially over the years. This results to more functionality in the same die area, hence increased design complexity [4]. With such an increase in complexity of designs, the time required for verification experiences a significant upsurge. In comparison to directed tests, Constrained Random Verification (CRV) technique improves the productivity gain significantly [5]. This methodology is crucial because it saves time in achieving coverage closure. The traditional method of using targeted tests to verify specific design elements grows exponentially with the number of inputs, hence there is a requirement for speeding up CRV [4].

There has been growing trend in the use of Python as high-level and general-purpose programming language. Renowned for its conciseness and formidable capabilities, it has emerged as a cornerstone for pioneering technologies, prominently encompassing artificial intelligence, automation, machine learning, General Purpose Interface (GPI), and networking [6][7]. Additionally, the success of Python is due to (i) a simple and clean syntax, (ii) interpreted and dynamically typed (iii) object oriented (iv) huge ecosystem, (v) a rich standardized libraries that is conveniently available, and (vi) very good documentation and help support [8][9].

For the functional verification, Hardware Verification Language (HVL) Verilog was transitioned to SystemVerilog in order to incorporate numerous powerful programming features, particularly object-oriented programming with additional capabilities such as constrained random data generation and functional coverage [9]. SystemVerilog, which is also used as a language construct for industry-utilized verification methodologies like Metric Driven Verification (MDV) and CRV, is a complex language with a steep learning curve especially for engineers who are new to hardware verification. It requires very good understanding of digital design concepts and a thorough grasp of the language syntax and constructs. Developing an efficient and robust testbench in SystemVerilog can be time-consuming [9]. Figure 1 shows that HVL i.e., SystemVerilog, is the most complicated language in comparison with other programming languages which has 1315 specification pages and 248 keywords as per IEEE 1800-2012. On the other hand, Python (v3.7) is a high-level programming language with only 35 keywords and 600 specification pages with 1750 full standard libraries [10]. While SystemVerilog follows a set format, various Electronic Design Automation (EDA) tool vendors might incorporate the format differently within their simulation tools. Although it is widely used, there can be variations in the level of tool support across different vendors [11].

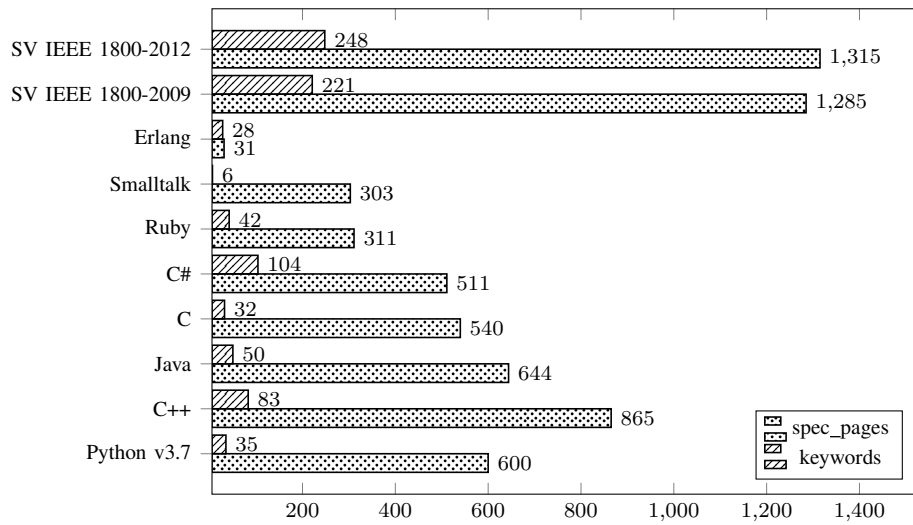


Fig. 1: Language complexity with respect to number of specification pages and keywords [10]

A recent study conducted by the Wilson research group in 2022 shows that the trend of using python as a HVL for Application-Specific Integrated Circuit (ASIC) development has been increased and can be seen in Figure 2.

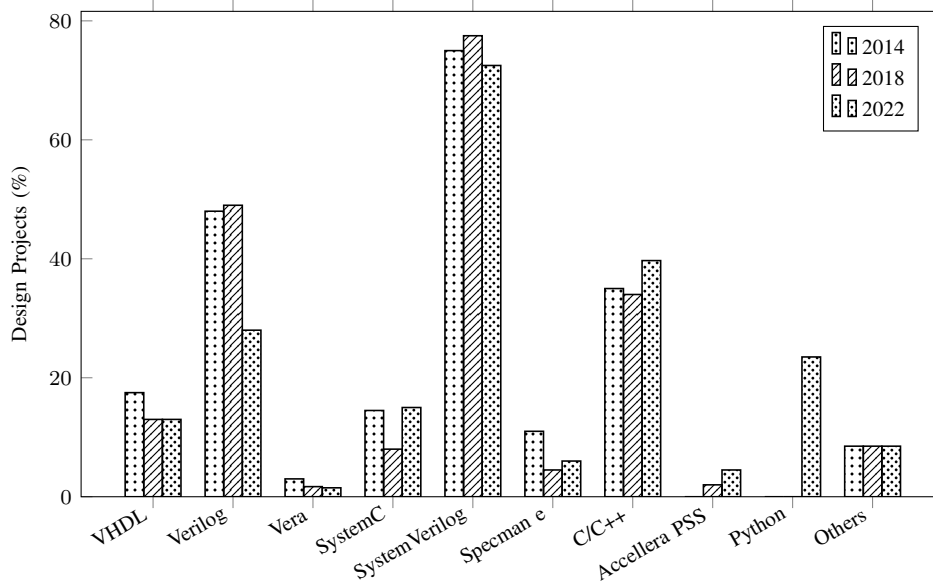


Fig. 2: ASIC verification language adoption [1]

In this paper, the main focus is to evaluate the usage of a Python-based verification setup on design IPs and compare it against the existing state-of-the-art HVL for instance SystemVerilog. The key highlights of the paper are listed below:

- Comparison of SystemVerilog and Python as HVLs
- Exploration of Python libraries i.e., cocotb (framework enabling functional verification), cocotb-coverage (library allowing CRV and functional coverage)
- Preparation of testbenches in Python and SystemVerilog for the design IPs. i.e., 32-bit Arithmetic Logic Unit (ALU), Inter-Integrated Circuit (I2C), and 16-bit Analog-to-Digital Converter (ADC)
- Analysis of results and empirical observations made during the testbench preparation for respective IPs
- Comparison of performance metrics for both verification environments, simulated with various EDA tools

The rest of the paper is organized as follows: Section II introduces functional verification along with various methodologies and presents related work. Section III explains the building blocks for the Python-Coroutine based

cosimulation testbench (Cocotb) verification implementation. Section IV discusses the results and compares for SystemVerilog and Python-Cocotb verification setups. Section V details the empirical observations made implementing the verification. Lastly, Section VI summarizes the paper and lists further scope of Python-based verification.

## II. BACKGROUND

The main goal of functional verification is to test the verification target, thereby guaranteeing accurate and comprehensive functionality [12]. The present design verification stage utilizes a well-established technique for larger designs known as simulation-based verification. Such modern methodologies involve a largely automated procedure encompassing test generation, checking, and coverage collection, combined with instances of manual involvement [13]. One of the methodology is CRV where stimulus generation, scenarios can be generated in an automated fashion under the control of a set of rules, or constraints, specified by the user [14]. Another notable approach rooted in simulation is the Universal Verification Methodology (UVM), which employs Transaction Level Modeling (TLM) for the creation of testbenches. It is a class library that makes it easy to write configurable and reusable code [5]. All the technologies discussed uses SystemVerilog as their language construct. In contrast, this paper discusses simulation-based verification for 3 designs detailed in section III, using Python as HVL and *cocotb*, *cocotb-coverage* libraries.

The authors in paper [15] presents an explanation of the Python-based verification methodology along with a discussion on code coverage data obtained from verifying a design Intellectual Property (IP) using a Python testbench. A similar work is done in paper [16], that extends Cocotb to provide constrained randomization and functional coverage constructs. The paper also motivates to enable the implemented mechanisms to be adopted by verification engineers, taking advantage of Python syntax and object-oriented approach. Nevertheless, these works did not discuss feature, performance comparison with respect to the other verification methodologies. PyVSC is a library supported by Python that has the same functionality as *cocotb-coverage* library to support randomization and functional coverage [17]. The work claims that PyVSC will make it easier for SystemVerilog practitioners to reuse their knowledge of constraints and coverage in Python. The work [18] employs Cocotb to model the Python testbench for a comparator designed in Verilog and an open-source simulator Icarus Verilog for simulating the testbench. Additionally, machine learning technique is implemented to optimize design verification. In the paper [19], the testbench is written in Python to develop a library (VeRLPy) for the verification of digital designs with reinforcement learning.

The related works elaborated above mostly discusses creating Python testbench using Cocotb, how SystemVerilog functional coverage constructs are supported by Python library like PyVSC. But none of them examines the comparison of the verification methodologies or language construct(s) used for the methodologies. In this work, we try to address the simulator compatibility, feature comparison between HVLS, its performance in terms of run-time.

## III. IMPLEMENTATION

The verification implementation with Python-Cocotb involves three key components: Design Under Test (DUT), Testbench written in Python, and a Makefile. These building blocks play crucial roles in carrying out the verification process as discussed below.

### A. Design

The DUT in the Python-Cocotb testbench can be designed in any Hardware Description Language (HDL) i.e., SystemVerilog, Verilog, or VHDL. For this paper, we carefully selected three different designs for thorough verification. These choices were made based on important factors that enhance the significance of their verification. A short explanation to the design IPs used in this work is as follows:

#### 1) ALU

The 32-bit ALU, a combinational design written in Verilog, carries out a range of operations on the input signals and generates 32-bit output. It supports two arithmetic operations, namely addition and subtraction, and also provides functionality for six logical operations: NOT, AND, OR, XOR, NAND, and NOR. In Figure 3, (a) depicts the block diagram of 32-bit ALU where input buses  $a$  and  $b$ , control bus  $op$ , and output bus  $r$  are responsible for transmitting their corresponding signal data. Its computational capabilities finds applications in modern processors.

## 2) I2C

In general, reactive testbenches are particularly useful for protocol like I2C, where the communication is event-driven and depends on the actions of both the master and the slave devices. For the verification process, the testbench created in Python-Cocotb acts as Master for the design IP coded in Verilog. In Figure 3, (b) shows the block diagram of I2C master-slave configuration.  $A_0$ ,  $A_1$ ,  $A_2$ , and  $W_p$  are unidirectional input signals whereas  $SDA$  and  $SCL$  are bidirectional in/out pins.  $SDA$  transfers addresses and data during input and output operations; while  $SCL$  synchronizes the data exchange to and from the DUT.

## 3) ADC

It is an analog mixed signal design, implemented in SystemVerilog. Python-Cocotb testbench is set up to evaluate Cocotb with the design IP performance. In Figure 3, (c) shows that *adc* is the top level, where real valued from -10V to 10V are given. *\$realtobits* function has been used to convert *analog\_in* to 64-bit analog input, which is then fed as input to *adc\_core* and it produces the 16-bit digital output *digital\_out*.

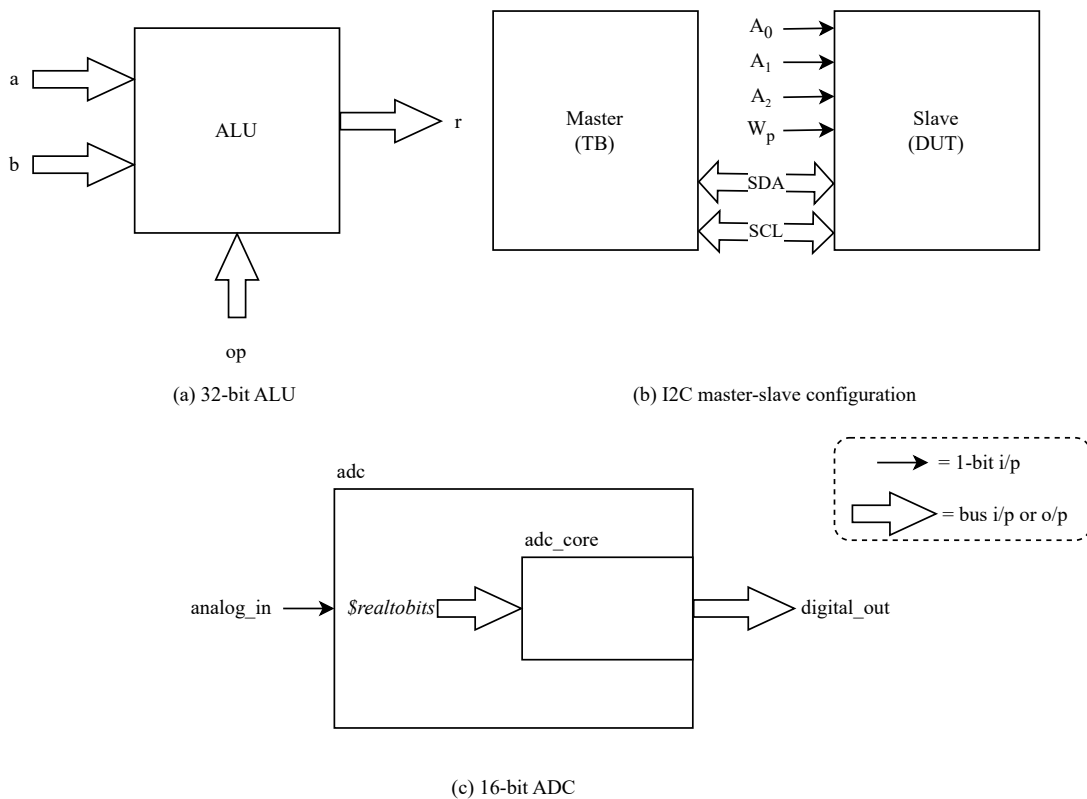


Fig. 3: Design(s) under test

## B. Python Testbench

The verification setup consists of a top testbench, where Cocotb connects the Python testbench with the simulator. It also provides the Python library for creating synchronous logic. In this setup, the testbench uses constrained randomization of signals and bin definitions for analyzing functional coverage. These capabilities are supported by the *cocotb-coverage* library.

The basic structure of general Python-Cocotb testbench is explained using ALU testbench in Listing 1. Firstly, the important required modules are imported, for instance, *cocotb*, and all the objects from *cocotb-coverage* module. Then the tests specified in the testbench is automatically discovered by Cocotb using *cocotb.test()* decorator<sup>1</sup> during simulation run. The clock is generated succeeded by signals being constrained and randomized. These signals are sent to DUT and reference model. The coverage sample function is called and finally the outputs from DUT and reference model are asserted.

<sup>1</sup>Decorators use @ followed by the decorator name before a function or class declaration. When invoking the decorated function or class, the decorator runs first, and its output substitutes the original.

A single test specified in the ALU testbench is simulated with various number of transactions i.e., 20000, 40000, and 60000. Similarly, a single test is present in the ADC testbench which is run with 210, 410, and 610 number of transactions.

A Bus Functional Model (BFM) is a class that sends data using coroutine tasks. It contains coroutines<sup>2</sup> that manipulate signals to communicate to the DUT. Hence, a class-based BFM testbench is created for I2C enhancing modularity. Figure 4 shows the BFMs (coroutine tasks) included in the I2C testbench (Master) and I2C bus communicates between testbench and the DUT. The testbench includes 3 tests, namely, byte write followed by random read, page write succeeded by random read, and page write read sequentially.

```

1  ## Import required modules ##
2  import cocotb
3  ..
4  @cocotb.test() # Automatic test discovery
5  async def alu_test(dut):
6  """ Test coroutine starts with a handle to the the top level (dut)"""
7  cocotb.start_soon(Clock(dut.clk,20,units="ns").start()) # Generate clock
8  a = 0 # Initialize the signals
9  ..
10 for i in range(1000): # No. of transactions specified in loop count
11     ref_out = alu_ref(a,b,op) # Send the i/p signals to reference model
12     and get o/p
13     a = random.randint(-100, 100) # Randomize the signals
14     ..
15     dut.a.value = a # Send the input signals to the DUT
16     ..
17     sampling_function(a, b, op) # Sample coverage
18     assert ref_out == dut.r.value.integer # Assert outputs from reference
19     model and DUT

```

Listing 1: Python-Cocotb testbench e.g. ALU

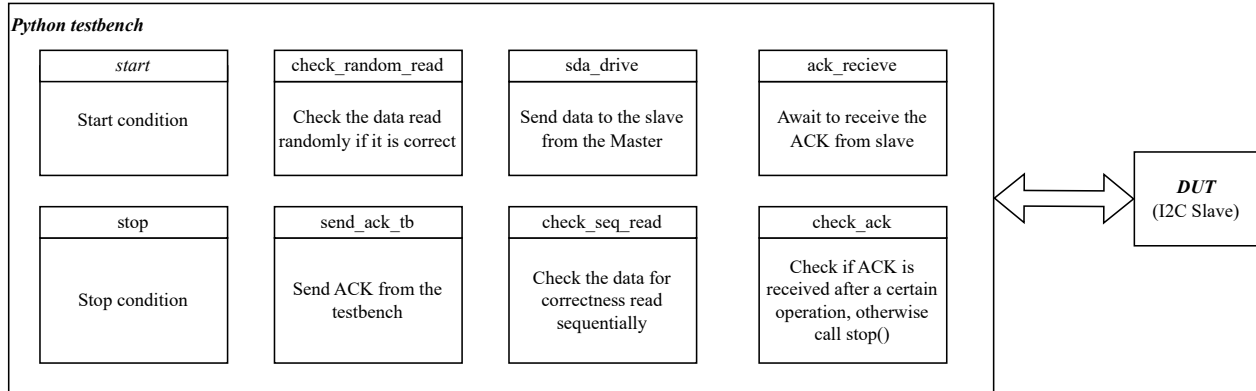


Fig. 4: BFM class based Python-Cocotb testbench e.g. I2C

### C. Makefile

A verification environment set-up needs a build option *Makefile*. It contains information about the project, starting from EDA tool to top level instantiation. Listing 2 shows the Makefile for setting up the testbench environment for ALU. After the execution of command in line 8, the libraries gets compiled and simulator starts.

```

1  SIM ?= xcelium
2  GUI ?= 1
3  TOPLEVEL_LANG ?= verilog
4  MODULE = alu_test
5  TOPLEVEL = alu
6  VERILOG_SOURCES = ../rtl/alu.v
7
8  include $(cocotb)/makefiles/Makefile.sim

```

Listing 2: Makefile e.g. ALU

<sup>2</sup>Coroutine is a decorated function that facilitates asynchronous execution and cooperative multitasking.

#### IV. RESULTS

The three design IPs i.e., ALU, I2C slave, and ADC are verified in SystemVerilog-UVM and Python-Cocotb testbenches and investigated compatibility of Cocotb with commercial simulators like Cadence Xcelium [20] and Siemens Questa [21]. Additionally, an open-source simulator Verilator [22] is explored.

##### A. Features Comparison

While implementing the verification environments with SystemVerilog and Python as HVLS, they are found to have setup advantages with Python over SystemVerilog like, setting up test environment with any simulator only requires to modify makefile variable *SIM*. Table I shows other features compared for both verification implementations.

TABLE I: Features comparison for SystemVerilog and Python-Cocotb

Feature	SystemVerilog	Python	Remarks
Declaration of data types	Static	Dynamic	Python allows undeclared variables and perform any operation on them. Additionally, it has advanced data structures e.g., tuple and dictionary, unlike SystemVerilog.
Supported types of logic	0, 1, X, Z	X, Z, U, W	Python-Cocotb needs BinaryValue object for these logics
Parameterization and size of the variable	Required	Not required	If size is not declared in SystemVerilog, data may be lost after an assignment to a different size than specified
Styles of control flow	<i>begin, end</i>	Proper indentation	<i>elif</i> in Python replaces case in SystemVerilog/Verilog
Functions	Not objects	Callable objects	Function in SystemVerilog are not objects and cannot be stored or passed directly as arguments
Exceptions	Not supported	Supported	In Python, exceptions are caught with <i>try/except/finally</i> blocks
Libraries	-	Large	Create reference model for any complex design easily
Interpreted	No	Yes	It allows to restart the simulator without recompiling and edit tests while it is running
Design Hierarchy	Includes top testbench	Does not include top testbench	It limits debugging capabilities, since tracing back signals in the testbench is not possible

##### B. Performance Metrics

Based on simulation results, certain performance metrics are defined. These metrics are analyzed and compared for both verification environments i.e., Python-Cocotb and SystemVerilog-UVM in this subsection.

###### 1) Design Hierarchy

The hierarchy in the simulators design browser is different in SystemVerilog-UVM and Python-Cocotb testbenches. The SystemVerilog-UVM testbench includes the top testbench whereas Python-Cocotb starts with the DUT or *TOPLEVEL* defined in the build option, as explained in Figure 5. This results in the limitation of Python-Cocotb since it hinders the debugging capabilities of the testbench signals.

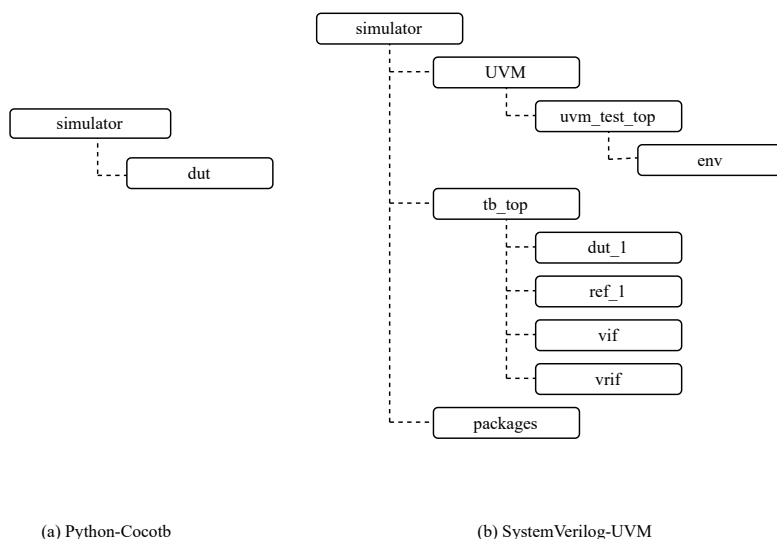


Fig. 5: Design Hierarchy

## 2) Simulation run-time

The Python-Cocotb and SystemVerilog testbenches are compared in terms of simulation run-time. They are simulated using various simulators such as Xcelium, Questa, and Verilator, with detailed testbench specifications provided in subsection III-B. During the simulation, it became evident that Verilator cannot simulate I2C and ADC designs due to non-synthesizable nature of I2C design used for this work whereas ADC design required substantial modifications to verilate it. But ALU design got simulated with Verilator, showing similar run-time performance as Xcelium.

Additionally, it is observed that the simulation run-time of Python-Cocotb testbenches is slower compared to that of SystemVerilog or SV-UVM testbenches, as demonstrated in Figure 6a, Figure 6b, and Figure 6c. This difference is attributed to the reasons discussed. Generally, SystemVerilog employs simulation directives and commands to establish communication with the simulator. The close integration between SystemVerilog-UVM and the simulator enhances simulation execution, resulting in relatively shorter run-time. Conversely, the interaction between Python testbenches and the simulator via VPI/VHPI is typically slower and less tightly integrated than the direct interaction between SystemVerilog-UVM and the simulator. This overhead becomes more significant as the number of transactions increases, leading to longer simulation run-time for Python-Cocotb testbenches.

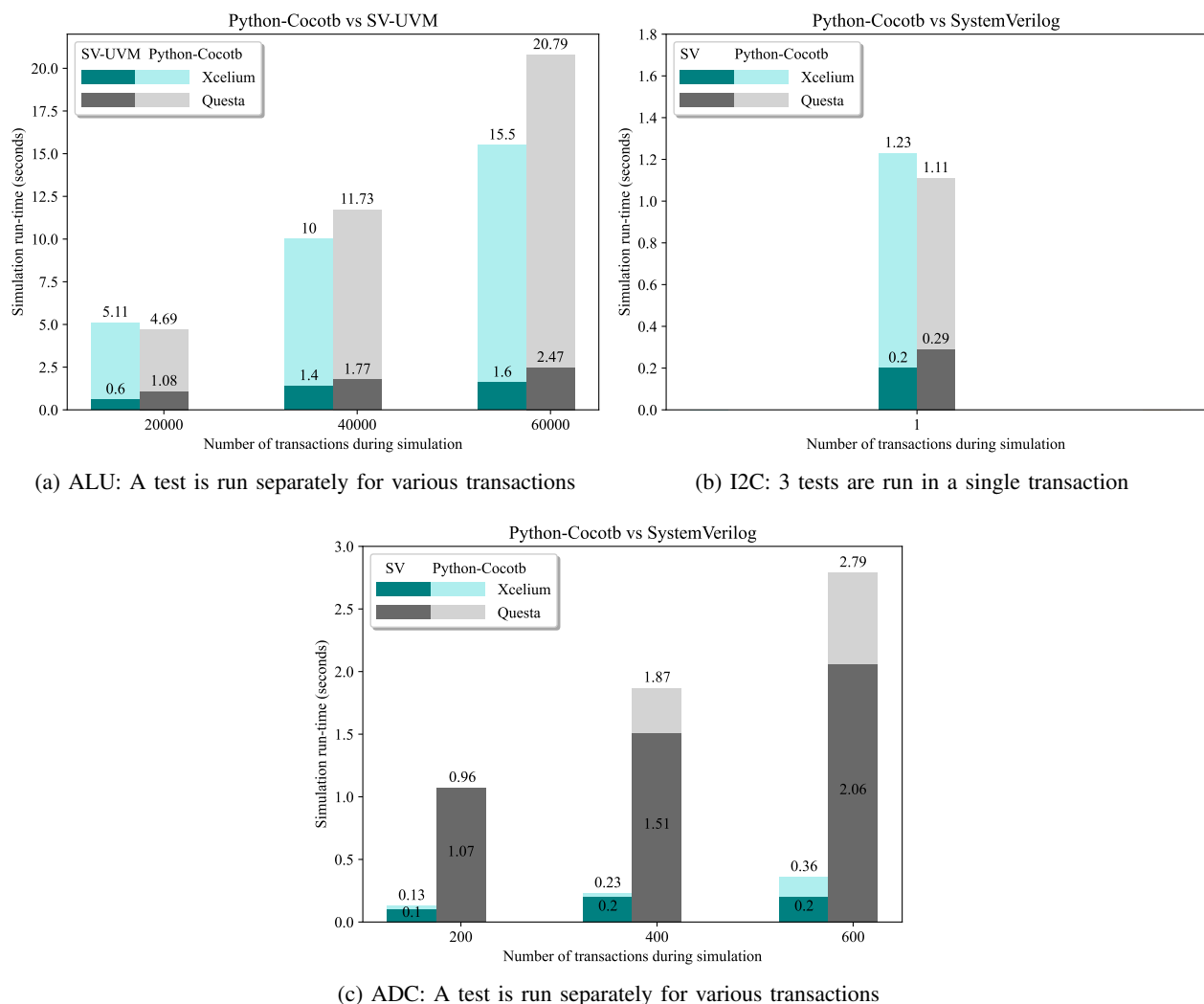


Fig. 6: Simulation run-time comparison with different simulators

## 3) Coverage Analysis

Table II details the bins definition for all the cover items for design IP, i.e., ALU, I2C, and ADC along with the results. The coverage model defined was same in both SystemVerilog and Python testbenches and the results obtained were also similar in both cases. For ALU and ADC, the total coverage obtained in 100% for the bins

TABLE II: Coverage results for SystemVerilog-UVM and Python-Cocotb testbenches

Design	Cover items	Bins definition	Coverage (%)	Description
ALU	a	3 bins	100	Cover the range $-2^{31}$ to $2^{31}-1$
	b			
	op	1 bin		Cover all operations ranging 0 to 7
	aXb	-		
	aXop			
	bXop			
aXbXop				
I2C	c_start	2 bins; <i>True</i> , <i>False</i>	50	Cover start condition
	c_stop			Cover stop condition
	c_write			Cover write operation
	c_read			Cover read operation
	c_ack			Cover ACK recieved
	c_nack			Cover NACK condition
	c_repeated_start	100	Cover repeated start, i.e., if write and read is done in the same test.	
	c_mem_data	16 bins	90.62	Cover for data write and read in memory are same
c_mem_addr	32 bins	100	Cover for write and read are same for memory address access	
ADC	analog_in_tb	3 bins	100	Cover the range -10V to 10V

defined whereas I2C reached 85.48 %. It was also verified that all the functional coverage features in SystemVerilog is available in *cocotb-coverage* library, although they are syntactically different.

## V. EMPIRICAL OBSERVATIONS

While implementing the verification environments for the design IPs i.e., ALU, I2C, and ADC with Python-Cocotb and *cocotb-coverage*, there are some observations made as listed below.

- 1) ALU: While utilizing the Python-Cocotb testbench (i) If the input signals *a*, *b*, and *op* are not initialized, it gives *Assertion Error* in the first clock cycle and simulation stops. Therefore, it is crucial to initialize the input signals before performing any operation. (ii) The bins definition for covering ALU signals has to be specified explicitly. If auto bins are attempted to be created for this design IP, it requires a significant amount of space for the number of bins to be generated and results in a memory error.
- 2) I2C: SDA is open-drain terminal, so it has to be pulled up through a resistor. Python-Cocotb lacks native support for pull-up/pull-down signals and tristate logic, a workaround is achieved by introducing an HDL wrapper. In contrast, SystemVerilog, being a HDL, provides built-in support for pulling up any signal, and does not need an additional wrapper. Figure 7 details the workaround to include tristate logic in Python testbench.

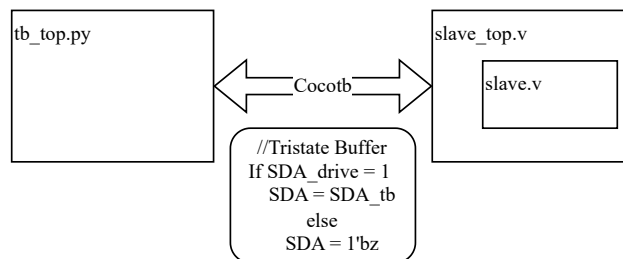


Fig. 7: HDL Wrapper to include tristate logic in I2C Python-Cocotb testbench

- 3) ADC: Analog simulation package that lets real number modelling in SystemVerilog, are not supported in the Python-Cocotb. It gives VPI error (Communication error). To convert the real input *analog\_in* to 64-bit digital input, the datatype is defined as *real* type. This 16-bit signal is then sent to the design. Listing 3 and 4 show that *analog\_pack\_sv* module is imported in the *adc* wrapper for SystemVerilog testbench whereas the input *analog\_in* is declared as *real* datatype for Python testbench respectively.



```

1 import analog_pack_sv : : * ;
2 input analog_t analog_in ;
3 assign analog_input = $realtobits(analog_in) ;

```

Listing 3: adc wrapper in SystemVerilog testbench

```

1 input real analog_in ;
2 assign analog_input = $realtobits(analog_in) ;

```

Listing 4: adc wrapper in Python-Cocotb testbench

## VI. CONCLUSION

In this paper, We analyzed the verification of three designs using Python-Cocotb and SV-UVM in three simulators. When running Python-Cocotb testbenches, it is found that the simulation run-time increases with increase in transaction count for the multiple simulation run. This behavior is attributed to the communication between the testbench and simulators through VPI/VHPI, which involves longer interaction times with the simulators. Consequently, the overall simulation run-time is extended. Nevertheless, this interaction via GPI provides necessary hooks to access and control the simulator’s internal data structures, signals, and events.

Concerning the CRV and functional coverage in Cocotb, the constrained randomization of the input signals and coverage constructs are derived from *cocotb-coverage* library. The coverage analysis yields results similar to those obtained in SystemVerilog.

Despite Python’s interactive and user-friendly coding nature, the testbench is not included in the design hierarchy due to Cocotb’s co-simulation approach. If the testbench can be integrated into the top of the hierarchy, it would greatly improve debugging capabilities by facilitating the tracing back of signals. Combining Cocotb and Python libraries, and machine learning techniques holds promise for enhancing the verification process.

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