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Self-Triggering Mechanism for Modeling a Low-Dropout Regulator with Load Capacitor

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***Abstract*— This paper present a Self-triggering Mechanism for modeling a Low-Dropout Regulator (LDO) with current limiting and load capacitance by SystemVerilog User-Defined-Nettype (SV UDN), which mimics the transient behavior of the circuit. The self-triggering mechanism adjusts the time step based on any disturbance to the output, such as load current, reference voltage, etc. This method is compared to the same LDO using a discrete capacitor model with internal clock, the outcome shows up to 778x events saving with the proposed method.**

Keywords—Low-Dropout Regulator; Current Limiting; Low Events Count

I. INTRODUCTION

The SystemVerilog User-Defined Nettype (SV UDN) in Voltage-Current-Resistance format (VIR) is preferred above the scalar Real Number for modeling because the latter net type can only be modeled either voltage or current. To model the loading effects and driving capabilities, voltage, current and impedance of the same net are needed. This is enabled by using the SV VIR UDN and is already done for a power regulation block[1]. In addition, the SV VIR UDN is also capable of modeling capacitor as explained in the Rapid Adoption Kit (RAK) EEnet[2], this approach is used for modeling a charge-pump[3], and it can introduce transient response for an LDO model with a load capacitor.

The modeling of a capacitor with SV VIR UDN is implemented with discrete domain differentiation, which relies on an internal clock inside the capacitor module. To get a precise voltage behavior over time, the internal clock should be in nano or even pico-second range. If the sampling rate is constant, then it generates unnecessary events when voltage over capacitor is stable. Thus, it slows down the overall simulation speed, especially at the chip-level verification.

To avoid the fixed frequency of the internal clock, the behavior of the capacitor is modeled by a self-triggering mechanism with variable step size and a defined voltage step size by using the SV VIR UDN. This approach can be used for various switch-capacitor based circuit, such as charge-pump, DCDC converter, crystal device, etc. And it can also be used for a low drop-out regulator (LDO) with a load capacitor, such model is presented by this paper. Besides the transient response feature enabled by the load capacitor, the current-limiting feature is also modeled for the LDO.

In Chapter II, the LDO model including current limiting by using SV VIR UDN is explained. In Chapter III, the self-triggering mechanism is explained and shows the simulations results. Finally, conclusions are drawn in Chapter IV.

II. LDO MODEL INCLUDING CURRENT LIMITING

The LDO model described in this paper is implemented by using SV VIR UDN, this means every net is resolved to a {Voltage, Current, Resistance} structure. The final resolved value of a net can be read by referencing to its fields(s) by using the period (".") delimiter[2]. For example, the output net *vout_a* can be read as *{vout_a.V, vout_a.I, vout_a.R}*. The LDO has 2 modes, the voltage mode and the current limiting mode.

When the load current is lower than the maximum output current, the LDO is in the voltage mode, which can be seen as a voltage source in series with a resistor, with value of *vout_a_R* as shown in *Figure 1*. Such voltage source drives the output, *vout_a*, by *{vout_a_V, realZ, vout_a_R}*. Where *vout_a_V* is the variable to control the output voltage of such voltage source, *vout_a_R* is the output impedance and *realZ* is a constant represent the high-

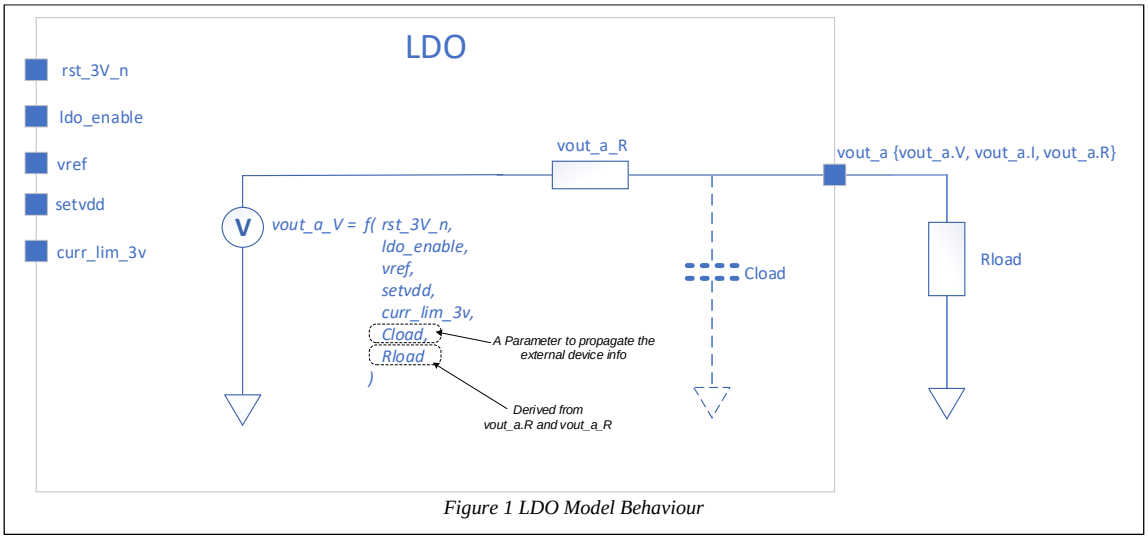

Figure 1 LDO Model Behaviour

Z state for real number. The variable *vout_a_V* depends on the reference value and the settings of the LDO. In the proposed self-triggered mechanism, the load capacitance is also included to calculate the time-step for updating the variable value. When the load resistor is connected to the output, it drives the *vout_a* net by *{0, 0, Rload}*. The net resolution function takes care of multiple drivers and eventually adjusts the resolved net voltage *vout_a.V* and *vout_a.R*. According to the equivalent circuit shown in *Figure 1*, it is possible to use the resolved resistance, *vout_a.R* to calculate the load resistance by

$$R_{load} = \frac{1}{1/vout\_a.R - 1/vout\_a\_R}. \quad (1)$$

By using this information, it is also possible to calculate the minimum load resistance of the LDO to determine whether the LDO should be in current limiting mode or in voltage mode by

$$R_{load\_min} = \frac{V_{target\_nolim}}{max\_curr\_lim} - vout\_a\_R, \quad (2)$$

where V_{target_nolim} is the target voltage in *Volt [V]* and *max_curr_lim* is the maximum allowed output current in *Ampère [A]*. When the load resistance becomes smaller than the calculated minimum resistance, as shown in (2), the LDO will enter the current limiting mode and the output target voltage during current limiting mode is calculated as

$$V_{target\_lim} = max\_curr\_lim * (R_{load} + vout\_a\_R). \quad (3)$$

This new target voltage will only be used when the LDO is in current limiting mode. The implementation of the LDO model is shown in *Figure 2* and includes both the current limiting behavior and the self-triggering mechanism.

Figure 3~~*Figure 3*~~ shows the behavior of the current limiting in the LDO model. The maximum allowed output current (max_curr_lim) is set to 30µA and the load resistance is decreasing. When the load resistance becomes lower than the minimum allowed current, the V_{target} starts using the V_{target_lim} instead of V_{target_nolim}. When the load resistance decreases further, the output voltage is decreasing as well. This is a wanted behavior, because the output current is limited and constant, the resistance decreases more, so by Ohms law, the output voltage should decrease as well. When the load resistance is increasing, it shows the opposite behavior. If the load resistance is higher than the minimum load resistance, the LDO switches back to voltage mode and the V_{target_nolim} is used again to define the output voltage.

```
always @(ldo_enable or rst_3V_n or setvdd or vout_a.V or vout_a.R or max_curr_lim or vout_a_R) begin
  Vtarget_nolim = (ldo_enable == 0 || rst_3V_n == 0) ? 0.0 : vref0v8_a.V + 0.1 + 0.05 * setvdd;   //Calculate Vtarget when current limiting is not enabled
  Rload = 1/(max(1e-12,1/vout_a.R - 1/vout_a_R));                                                  //Calculate load resistance
  Rload_min = Vtarget_nolim/max_curr_lim - vout_a.R;                                               //Calculate minimum load resistance before going to current limiting mode
  Vtarget_lim = max_curr_lim * (Rload+vout_a.R);                                                   //Calculate target voltage when LDO is in current limiting mode
  Vtarget = ((Rload < Rload_min) && (curr_lim_3v >= 1)) ? Vtarget_lim : Vtarget_nolim;              //Check whether LDO is in current limiting mode and decide with target voltage should be used
end


always @(Vtarget) begin: kickstart
  disable self_trigger;                                  //Remove future events in the self-trigger block
  if(vout_a.V <= (Vtarget-0.5*stepsize) || vout_a.V >= (Vtarget+0.5*stepsize) ) begin
    timestep <= !timestep;                               //Trigger self-trigger block if output voltage and the target voltage have a big difference
  end
end

always @(timestep) begin: self_trigger
  counter = counter + 1;
  current = abs((Vtarget - vout_a.V)/vout_a.R);                    //Calculate current
  out_current = max_curr_lim < current ? max_curr_lim : current ;  //Choose lowest value for current limiting
  cap_current = abs(out_current - vout_a.V/Rload);
  time_period = C * stepsize/cap_current;                          //Calculate new time period
  if(vout_a.V < Vtarget) begin                                     //Output voltage should increase to target value
      if((vout_a.V + stepsize) > Vtarget) begin
        vout_a.V = Vtarget;                                        //No new cycle needed, the target value and output value are the same
      end else begin
        vout_a.V = vout_a.V + stepsize;
        #time_period timestep <= !timestep;                        //Self-trigger the block for a new cycle
      end
  end else begin
    if(vout_a.V > Vtarget) begin                                   //Output voltage should decrease to target value
      if((vout_a.V - stepsize) < Vtarget) begin
        vout_a.V = Vtarget;                                        //No new cycle needed, the target value and output value are the same
      end else begin
        vout_a.V = vout_a.V - stepsize;
        #time_period timestep <= !timestep;                        //Self-trigger the block for a new cycle
      end
    end
  end
end

always @(curr_lim_3v) begin         //change in maximum allowed output current
  case(curr_lim_3v)
    0 : max_curr_lim = 5;           //Maximum output set to a high value such that it will not limit the output current
    1 : max_curr_lim = 7e-3;
    2 : max_curr_lim = 30e-3;
    3 : max_curr_lim = 75e-3;
  endcase
end
```

Figure 2 LDO Model Implementation Including Current Limiting and Self-Triggering Mechanism

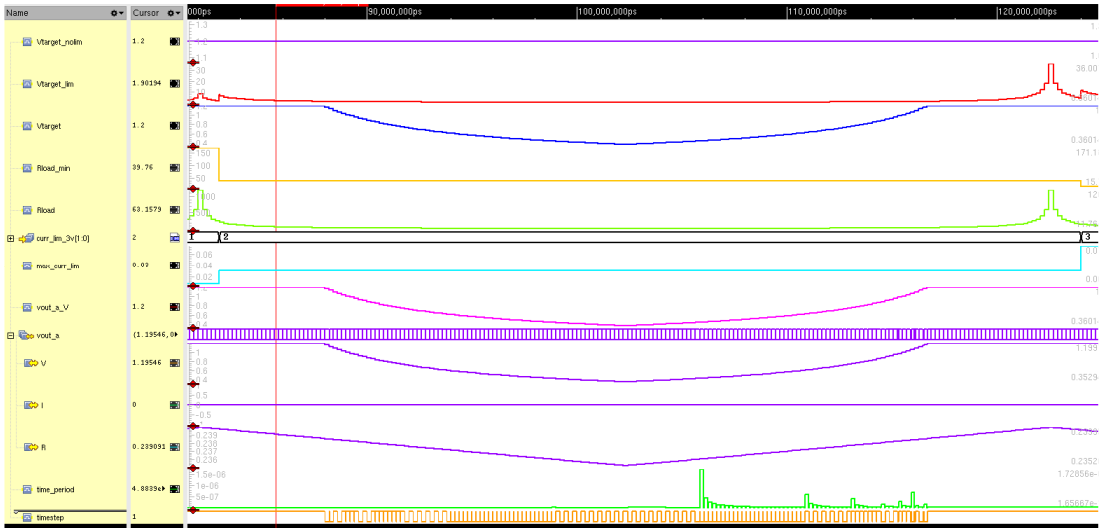

Figure 3 Simulation Result Current Limiting

III. SELF-TRIGGERING MECHANISM

To model the load capacitor, there are two possibilities, connect a capacitor model to the output of the LDO model or implement the capacitive behavior of the load already in the LDO model by using the self-triggering mechanism. The possibility using the self-triggering approach is shown in *Figure 1*, the possibility which uses the externa capacitor is shown in *Figure 4.* The modelling of a capacitor in both cases is based on the following well-known formula:

$$I = C * \frac{dV}{dt}, \tag{4}$$

where I is the current in *Ampère [A]*, V the voltage in *Volt [V]*, C the capacitance in *Farad [F]* and t time in *seconds [s]*. When the external capacitor approach is used, as shown in *Figure 4,* the timestep, *dt*, is fixed and the voltage

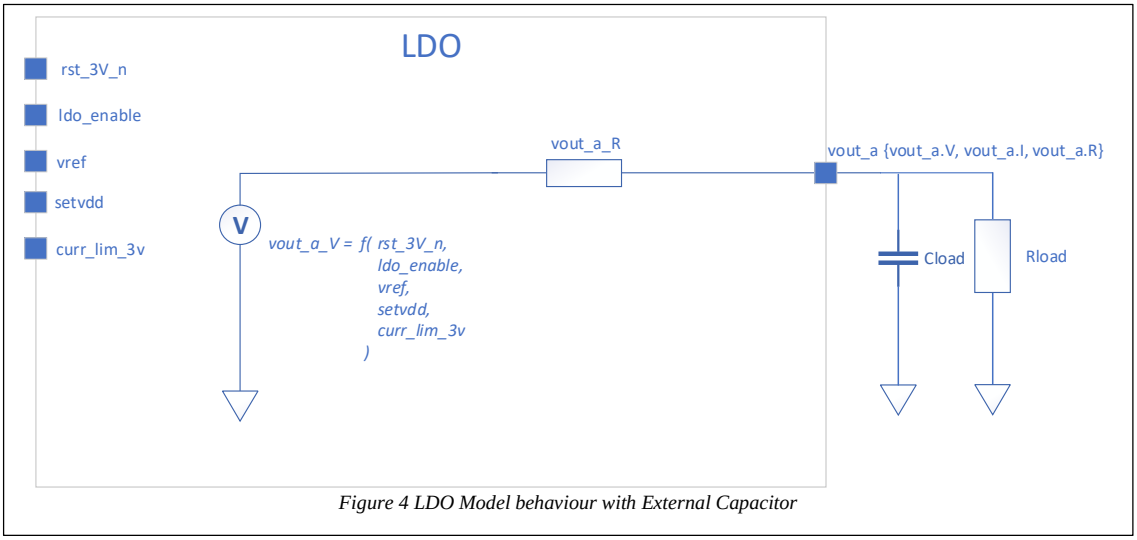

Figure 4 LDO Model behaviour with External Capacitor

step, *dV*, is calculated at every timestep. This approach is shown in [2] and requires a high frequency internal clock to get an accurate result.

Another option is to model the capacitor inside the LDO model as shown in *Figure 1*, the self-triggering approach. This approach uses a fixed voltage step and a variable time step, the time step is recalculated every cycle and the fixed voltage step will be added to the output voltage (in case the voltage over the capacitor is increasing). The implementation of this approach is shown in *Figure 2*. The self-triggering is implemented with a clock signal generated by a non-blocking assignment with a left-hand-side (LHS) delay, and the corresponding always block is sensitive to the clock itself. And such block is named as **self_trigger**. To determine the variable time step, the following formula is used

$$dt = \frac{RC\Delta V}{V_{target} - V_0} \tag{5}$$

where $V_{target} - V_0$ the difference between the target voltage and the current voltage. When the **self_trigger** block is triggered, it first recalculates the time period as shown by the formula above. After that, the fixed voltage step size is added to the current output voltage. Finally, the **self_trigger** block is triggered again by itself and this cycle repeats itself until the output voltage is in a certain range of the target value.

Figure 5 shows how the events are generated using the self-triggering. The first timestep event is generated by the **kickstart** block when the target voltage (V_{target}) changes. This timestep event triggers the **self_trigger** block and a new timestep event is triggered by the **self_trigger** block itself. The time it takes for the **self_trigger** block to trigger itself increases by every new cycle to mimic the capacitive behavior as close as possible since the voltage over the capacitor changes slower when reaching the target value.

However, it could be possible that a new event is already scheduled in the future, but a change in V_{target} happens before the **self_trigger** block is triggered again. At this moment, the model should react immediately and not wait until the **self_trigger** block is triggered again. Therefore, the **kickstart** block is triggered by a change in V_{target}, the **self_trigger** block is disabled so the future event is cancelled and a new timestep event is generated. The self-triggering block is implemented using a nonblocking LHS delay to avoid the self-triggering block can only be triggered again when the previous assignment is finished. In this way, the **kickstart** block can trigger the self-triggering block at any moment when V_{target} changes.

Figure 6 shows the simulation result of the presented LDO model including the self-triggering approach. It is clearly visible that the self-triggering approach starts when there is a change in V_{target} due to a change in setting or

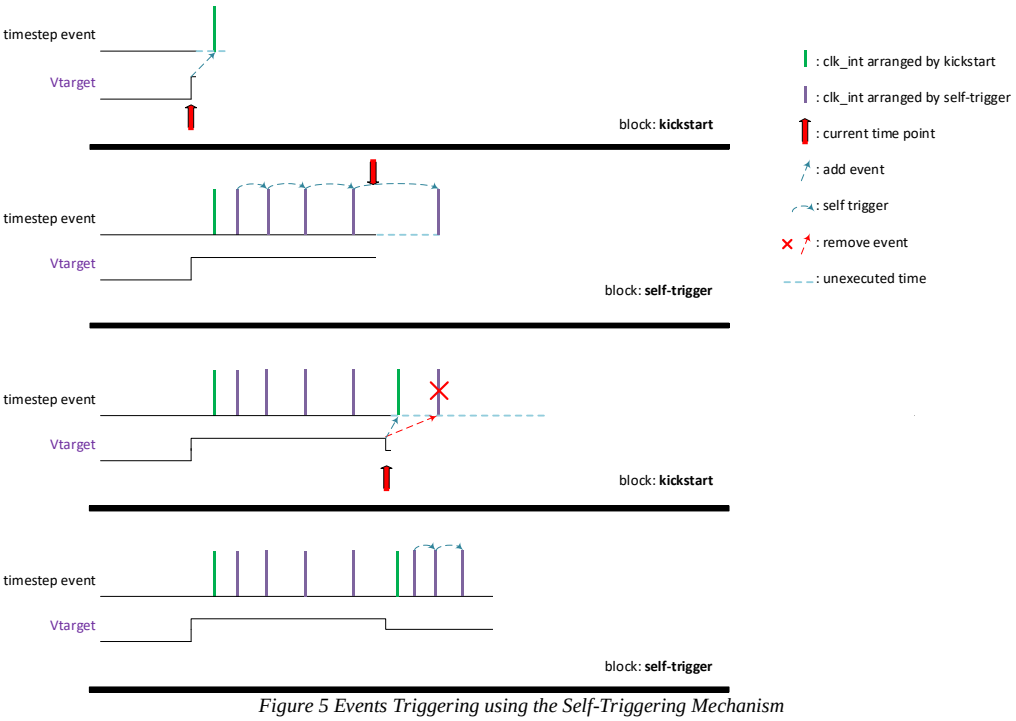

Figure 5 Events Triggering using the Self-Triggering Mechanism

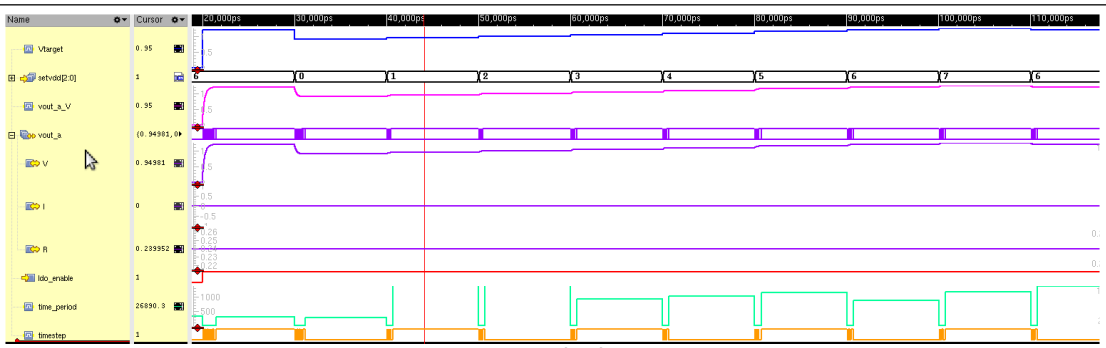

Figure 6 Simulation Result of Self-Triggering Approach

an enable of the LDO. The toggling from the timestep is also clearly visible and the delay is also visible as well as the increase in the calculated time period.

The presented the self-triggering LDO model with build-in load capacitor is compared against a simple LDO model plus a discrete capacitor model (including internal clock)[2], the simulation results are shown in *Figure 7*. It clearly shows the fixed time period, tinc, and thus the internal clock, ck. In these Figures, we clearly see that the time period is fixed (tinc) and it also shows the clock.

To compare the self-triggering approach with the approach which uses an external capacitor, the same load capacitor of 1nF for both simulations is used. In addition, the same test scenario of load regulation and output voltage trimming are applied to both simulations, which last 150µs.

For the simulation with the discrete capacitor model, in total 1,500,000 events have been generated due to the 0.1ns internal clock. On the other hand, when using the self-triggering mechanism, where the fixed voltage step size is set to 0.5mV, there are only 17,832 events, while the output voltage of these two simulations have a similar behavior. This difference can be explained by the decrease of events when the output voltage approaches the target output voltage and when the target output voltage is reached, no new events will be triggered until a change in the target voltage.

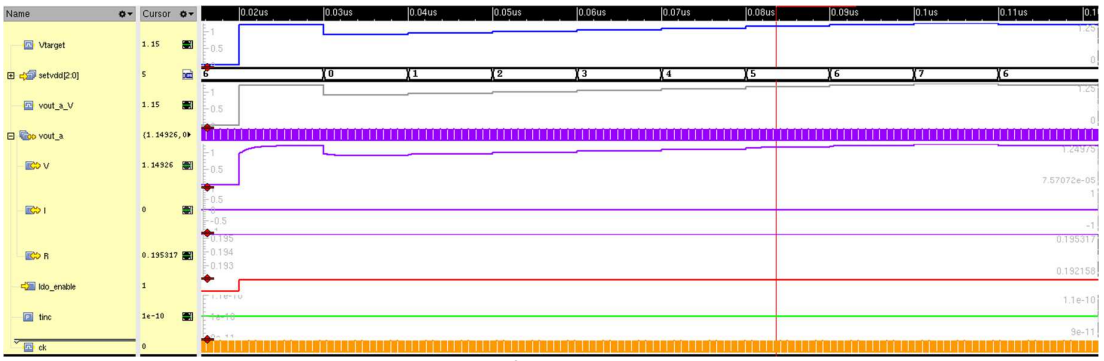

Figure 7 Simulation Result of LDO Model using External Capacitor

When comparing the number of events, the self-triggering mechanism needs 84 times less events to generate a similar result. It should be noted that when a less accurate result is needed the fixed voltage step size can be increased and the difference in number of events will even be bigger. For example, when a fixed voltage step of 5mV is used, the self-triggering mechanism only needs 1,926 events. In this case, the self-triggering mechanism needs 778 times less events. These results are summarized in Table 1. It should be noted that these numbers depend on the stimuli provided in the testbench. When the LDO is in current limiting mode during a longer time or the settings change faster, more events will be triggered by the self-triggering mechanism and the benefits of using the self-triggering mechanism in comparison to an external capacitor will become smaller.

Table 1 Comparison between Self-Triggering Mechanism and External Capacitor Model

	Stepsize	Number of Events	Ratio to Ext Cap
Self-triggering Mechanism	5mV	1,926	1/778.84
	0.5mV	17,832	1/84.11
External Capacitor Model	0.1ns	1,500,000	N.A.

IV. CONCLUSIONS

An LDO model with current limiting feature is presented by this paper. Thanks to the SV VIR UDN, the external load resistance can be extracted from the resolved output impedance, which determines the work mode of the LDO. The transient response of the LDO with load capacitor is modeled through a self-triggering mechanism, which variates the time steps instead of the voltage step, thus a fixed internal clock is no longer needed. The proposed LDO model is compared against a similar LDO model with the discrete external capacitor model. The comparison outcome shows for both models similar behavior. However, the number of events generated while using the self-triggering mechanism is 84 times lower, or even 779 times when less accuracy is needed. Since less events are generated while using the self-triggering mechanism, the simulation time will also decrease.

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