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The Road to Robustness: Addressing LPDDR5X PHY Verification Challenges with DFE

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Abstract— **We are now living in an era of digital transformation which has brought enormous amounts of data at our disposal. With the emergence of digital transformation along with future-facing technologies like 5G, AI, AR, VR applications, autonomous driving, and the metaverse require high-performance memory data transfer and make that data useful in processing, LPDDR5X Memory is an answer for better, faster, low power, ultra-high 8.5 Gbps data processing speeds, it's the memory solution built to prepare for the next generation of computing demands. As an enhancement JEDEC has proposed updated LPDDR5x spec where it can achieve a maximum data rate of 9600 mbps which can be coined as LPDDR5T(Turbo). Through various calibration algorithm, dynamic voltage and frequency scaling (DVFS), performance in the LPDDR5X has leaped forward massively. Due to this extreme high speeds at low power that data is prone to many signal integrity issues like Inter Symbol Interference (ISI), Silicon artefacts which may result in random data corruption. This necessitates of adding new techniques like Decision feedback equalizer(DFE) which will be used at receiver side to enhance the Data eye window. It throws a challenge towards verification engineer to mimic real time scenario in simulation to make sure that the calibration and algorithms like DFE are performed as intended in short time, this also adds lot of complexity in the verification environment as DFE is a mix of both Analog and Digital Solution. In this Paper we explore and propose a verification methodology which will address the challenges and solution for verification of LPDDR5X PHY with DFE. This solution can be scaled to other high speed interfaces where DFE scheme is used.**

Keywords—DFE;LPDDR5X;ISI

I. INTRODUCTION

As the world evolves with emerging technologies for applications like Artificial Intelligence (AI), Adaptive/**Generative AI**, Self-driven automobiles, High Performance computing(HPC), **Quantum Computing**, Ultra-high speed video/audio recording, etc., the requirement of data computation with high speed memories increases. These memories should have High performance, low latencies, low power & with low cost. With memories operating at low-power and ultra-high speed like LPDDR5X, the impact of Inter Symbol Interference (ISI) along with other real silicon factors effects like skew, distortion, jitter etc. will be more. This reduces the data eye width which may lead to corruption of data capture & data loss. To handle this situation, memory system uses decision feedback equalizer (DFE) as one of the solutions to compensate ISI effect and increase the data eye width for an optimal voltage. In this paper, we present a generic simulation-based verification method which will imitate real time scenarios and effectively find the issues of various calibration and DFE algorithms by modelling the channel & silicon factors effects for creating big data eye in LPDDR5T memory PHY.

II. OVERVIEW OF DDR SDRAM

Double Data Rate Synchronous Dynamic Random-Access Memory (DDR SDRAM) is a double data rate (DDR) synchronous dynamic random-access memory (SDRAM) class of memory integrated circuits used in computers. Compared to single data rate (SDR) SDRAM, the DDR SDRAM interface makes higher transfer rates possible by stricter control of the timing of the electrical data and clock signals. The name "double data rate" refers

to the fact that a DDR SDRAM with a certain clock frequency achieves nearly twice the bandwidth of a SDR SDRAM running at the same clock frequency by transferring data on both the rising and falling edges of the clock signal. SDR and DDR comparison is shown in below image.

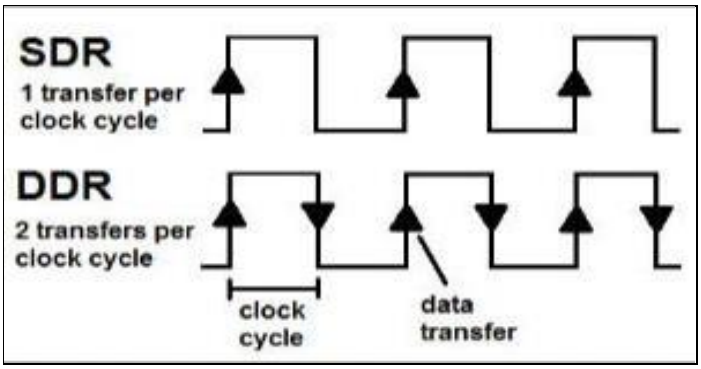

Figure 1. SDR and DDR Comparison

III. OVERVIEW OF LPDDR5X

Low Power Dual Data Rate (LPDDR) is a type of synchronous dynamic random-access memory which consumes less power and it is targeted to portable devices such as mobile phones. As naming says, it is a slightly modified version of DDR SDRAM with several changes to reduce overall power consumption.

Fifth generation of LPDDR (LPDDR5x) provides very high speed (8533mbps) for targeted devices. Below image gives different versions of Samsung LPDDR memory family which are already release to market.

Figure 2. Samsung memory speeds evolution

Advanced version of LPDDR5x (LPDDR5x 9600) is a new proposed variant of LPDDR5 which brings new height of ultra-high speed to mobile and automotive devices. This version of LPDDR5x offers a data rate of 9600 mbps(LPDDR5T).

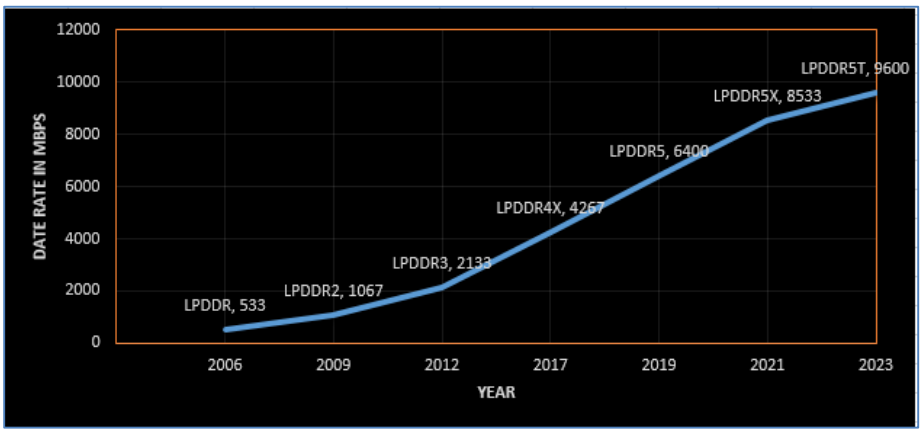

Figure 3. LPDDR Generations

IV. PRE-SILICON VERIFICATION CHALLENGES WITH HIGH SPEED DATA RATE

DDR memory connects to DDR memory system which contains two major components, DDR memory controller (MC) and DDR PHY to access DDR memory. Our scope of verification comes between DDR PHY and DRAM memory device since DRAM interface is very prone to data corruption.

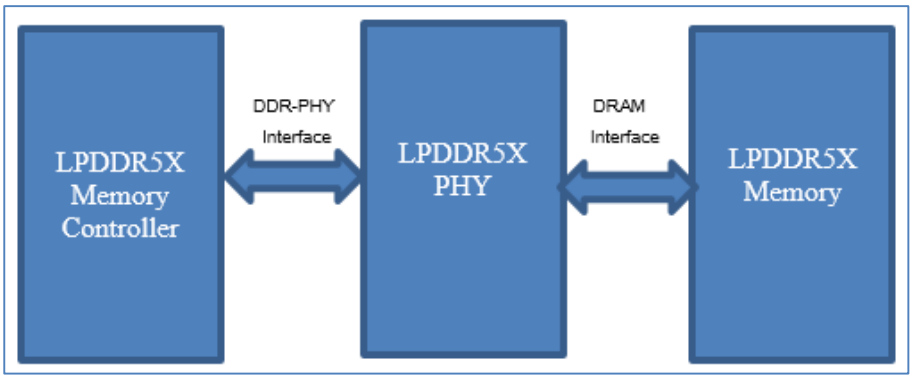

Figure 4. LPDDR5X Memory System

Due to tight packaging and high-speed, inter symbol interference can happen and distortion may be added to data signals. These added distortion during signal transition will reduce the width of data eye. With this reduced data eye width, there is big chance for wrong data sampling (Data corruption).

To get the more read data eye width, Decision Feedback Equalizer (DFE) is being used in LPDDR5X PHY.

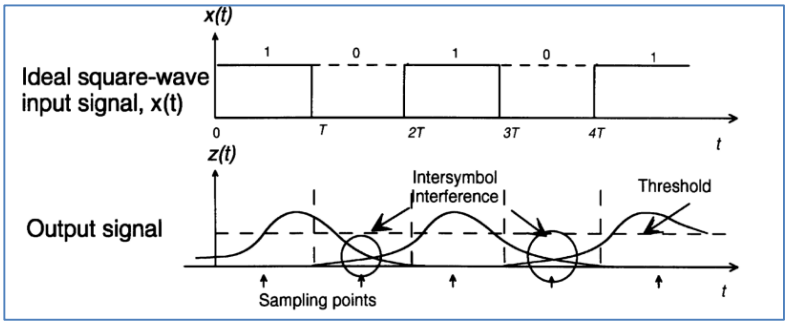

Figure 5. Inter Symbol Interference model

V. DECISION FEEDBACK EQUALIZER (DFE)

As real world communication channels are stressed with higher data rates, inter symbol interference (ISI) becomes a dominant limiting factor. One way to combat this effect that has recently received considerable attention is the use of a decision feedback equalizer (DFE) in the receiver. The action of the DFE is to feed back a weighted sum of past decision to cancel the ISI they cause in the present signaling interval.

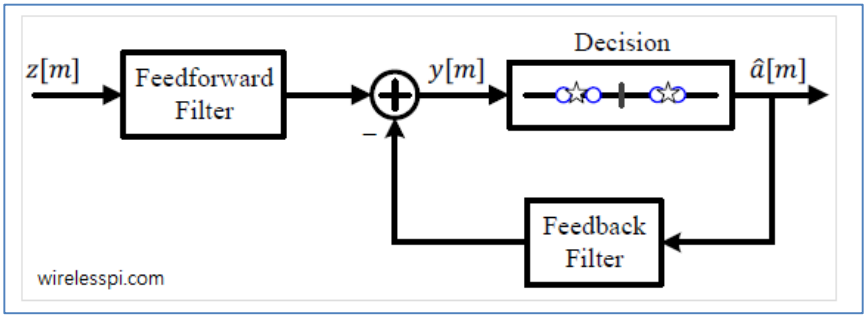

Figure 6. DFE Model

As shown in Figure 7, based on the VREF values provided, the design generates different digital output signals. DFE logic which is implemented in design chooses required signal based on previous signals values.

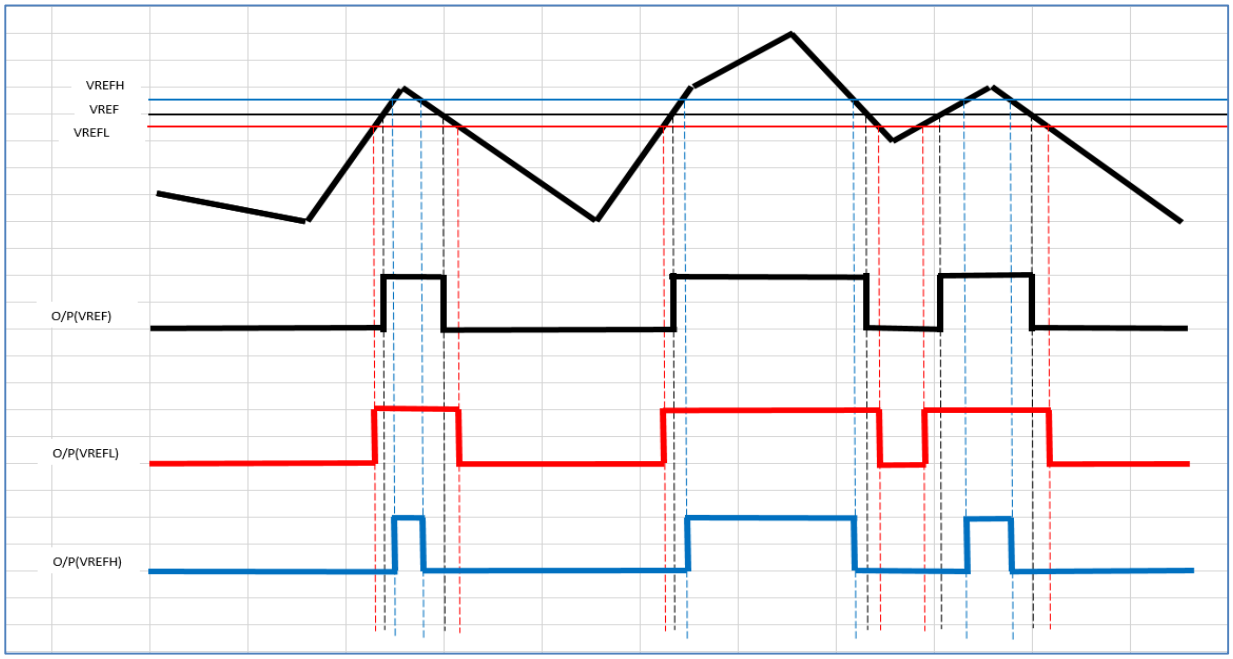

Figure 7. DFE outputs for different VREF

VI. PRE-SILICON VERIFICATION CHALLENGES FOR LPDDR5X 9600 (OR LPDDR5T) DDRPHY AND SOLUTIONS

For LPDDR5X memory and PHY, there can be different skews in each data pins compared to data strobes. These skews can be memory offset delays, board delays etc. LPDDR5X PHY performs different calibrations to make each data center-aligned to data strobes. As we discussed above, there will be ISI effect for each data bits and its impact is more with higher data rate like 9600mbps. DFE will be used at receiver side to reduce the impact of ISI. As simulation behaves as an ideal environment for the design under test (DUT), it is a challenge for verification engineers to mimic real world behavior. Skews/delay and noise/distortion should be added to data before reaching at receiver side to ensure the functionality of the algorithms. In below waveform snap shot, it shows the data and

data strobe for the LPDDR5x 9600mbps. It is clear that the Data and Data strobe are edge aligned as expected at source (LPDDR5x memory).

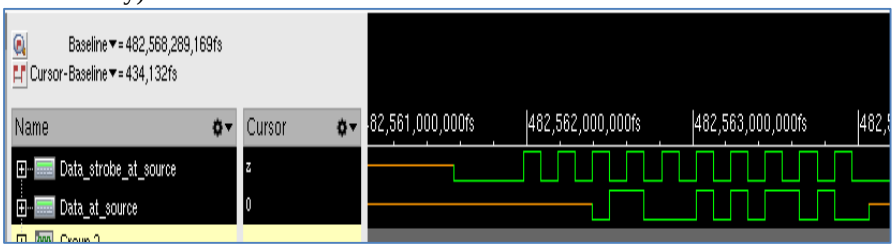

Figure 8. Ideal Signal behavior

Ideally, the receiver (LPDDR5x DDRPHY), makes 90-degree phase shift to data and makes data and data strobe center aligned.

In real case, there will be delays and distortion in data that causes misalignment and small valid data window (data eye). In simulation environment, on DRAM interface, we introduced a skew and noise injection (SNI) block as shown below.

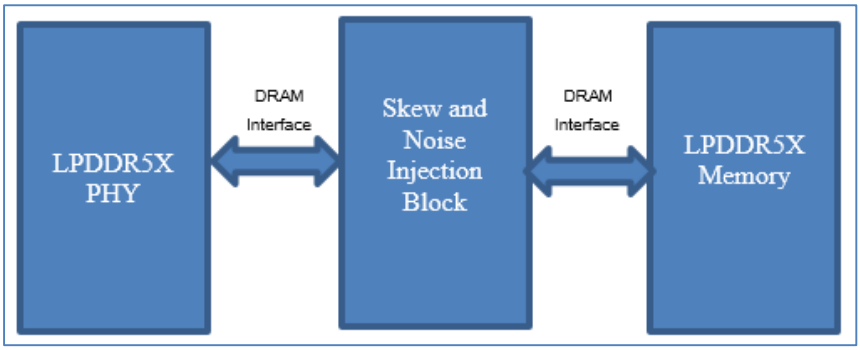

Figure 9. Skew and Noise injection (SNI) model in memory system

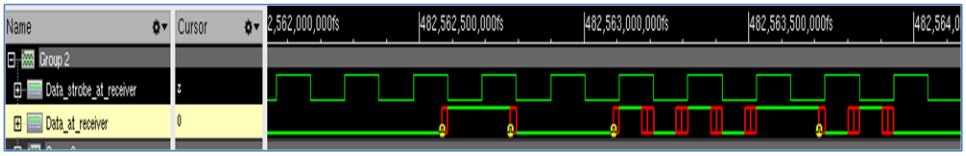

Figure 10. skew and noise/distortion induced data received at LPDDR5X DDRPHY

VII. DV MODELLING

DV modelling for ISI effects & DFE signal modulation is done by using Skew & Noise Injection(SNI) block which is implemented by using System Verilog as language & in UVM methodology. SNI block is an abstract model which represents the physical world and enables us to do IO characterization and Validation of LPDDR5x PHY by providing different features like skew, distortion, cross-talk effects, glitch etc. on Data signals. SNI block is configurable & facilitate the application of same skew/distortion to all bits of Data signal or different skew/distortion on each data bit signal. One can also specify same or different skew/distortion values for multiple ranks present in the memory. In order to make ensure the functionality & data eye valid window is not corrupted we have added functional assertions on data signals. For DV re-usability we have developed SNI block in Plug-N-play model with coverage enabled for all features.

Figure 11 shows the high level testbench architecture which is used for the verification. SNI block is connected between PHY RTL and memory models.

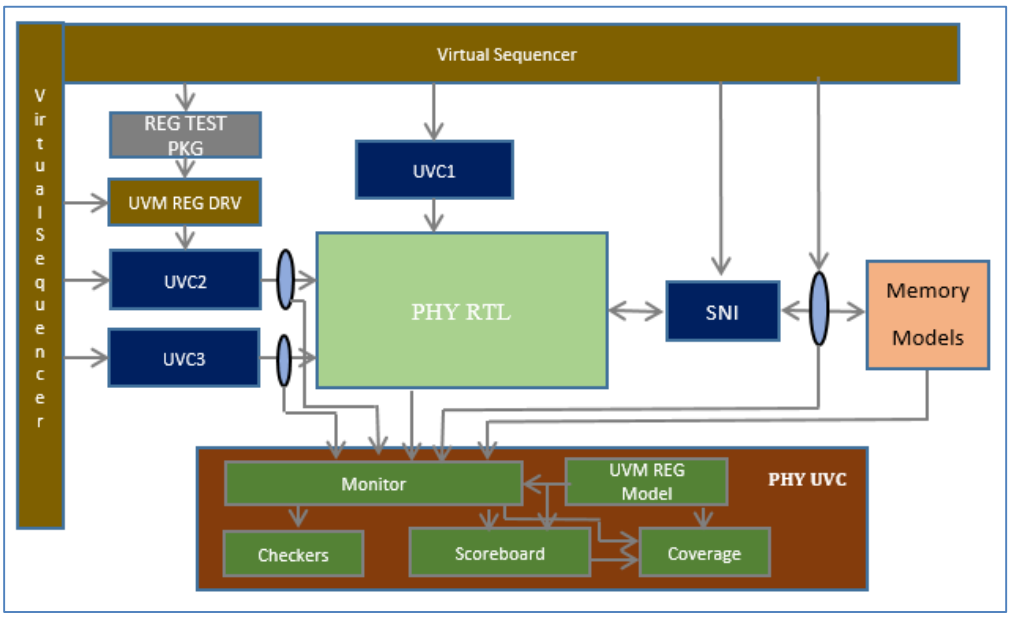

Figure 11. Testbench Architecture

SNI blocks can induce skews, distortion, cross-talk effects, glitch etc. for each bit independently. These features can be configured separately for drive and receive path of bidirectional signals. We have also enabled assertions in DV ENV for checking glitches, status check, data integrity. Functional Coverage is also enabled for all features of Design with DFE. Using mentioned DV modelling DV engineers will have more confidence to verify the DFE design part for high-speed LPDDR5x PHY and make ensure to find the issues at very early stage of verification and also improve the design quality

VIII. RESULT AND CONCLUSION

With increased demand of memory operations for high performance and low power consumption, it is very crucial for memories like LPDDR5X and memory system manufactures to bring the latest upgrades early in market without any compromise. Design verification engineers plays vital role in this aspects.

In this paper, we have discussed about challenges and solutions for verification of LPDDR5x 9600 mbps with DFE feature. By injecting skews and noise on DRAM interface data, we were able to mimic real time behavior. We have verified the behavior of LPDDR5x 9600 DDRPHY for DFE feature in a real time like environment.

In below waveform snapshot, it is shown that the data valid window is more with DFE operation and data is center aligned with data strobe with real time silicon noise factors.

Figure 12. Result comparison with and without DFE

Below table shows the data valid window observed during memory read operation with different combinations of induced ISI and DFE.

Ideal data width ~=104ps
ISI applied =30ps

Table. 1. Result comparison with different combinations

Distortion Applied	DFE Enabled	Valid data width
NO	NO	104ps
NO	YES	112ps
YES	NO	74ps
YES	YES	83ps

Data valid window reduces when distortion is applied and it is improved when DFE is enabled. With DFE feature, even at high speed data rate and worst case ISI, it is guaranteed that there will not be any data corruption while reading the data from LPDDR5X. Our skew & noise injection model gives confidence for the proper operation of this feature at initial RTL design phase itself.

The behavior of the design is ensured by checking the actual and expected data valid window. The data strobe should be center aligned with data and it should have more valid window when DFE is enabled. Expected data valid window is defined by the VREF values we provided as input. By using this checker, we have found multiple design issues in design algorithm. Pseudo code for the checker is given below

```
@(data);
Data_change_time=Current_time;

@(data_strobe);
Data_strobe_change_time=Current_time;

//Data valid window checker
//valid window=setup_time + hold_time

//Setup_time_checker
Data_strobe_change_time - data_change_time >= expected_setup_time;

//Hold_time_checker
Data_change_time - Data_strobe_change_time >= expected_hold_time;
```

IX. FUTURE ENHANCEMENT

As we discussed above, we have simulated and verified the DFE functionality which is implemented in digital design by providing the VREF values as input. Enhancement to be done for the verification of analog-digital mixed design. Figure 12 shows the expected input to the design (receiver) in analog as well as in digital signal mode.

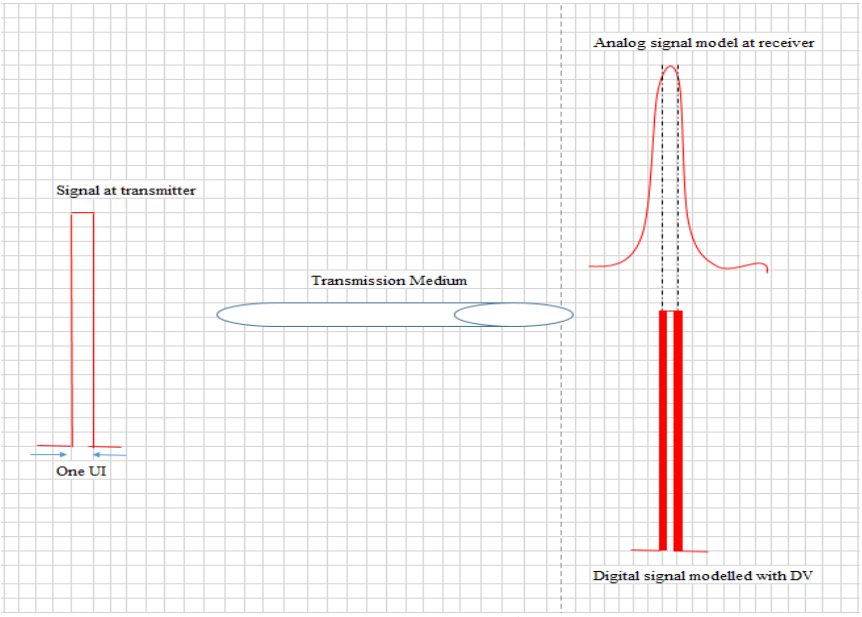

Figure 13. Receiver end signal modelling for analog and digital

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