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SV VQC UDN for Modeling Switch-Capacitor-based Circuits

Reusing SV Voltage-Current-Resistance Net Resolution Function with Voltage-Charge-Capacitance format for modeling a fully differential 40Mhz switched-capacitor crystal Oscillator

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The SystemVerilog User-Defined-Nettype in Voltage-Current-Resistance format has been gradually introduced to real-number modeling (RNM) of analog and radio blocks. As VIR format is defined as a structure of {Voltage, Current, Resistance}, it has a natural advantage for modeling the loading effect and driving capabilities comparing against the scalar Verilog-AMS wreal nettype. An example can be found for modeling a power regulation block[1]. And after introducing internal clocks for the building-blocks, VIR format is also capable for modeling capacitors and inductors, a corresponding application of charge pump modeling[2] was published in 2021. Within Renesas, an VIR format of SV UDN has been used to model LDO with current-limiting, smart-charger, DCDC buck/boost converters, etc.; and then it reaches its limitation for modeling a fully differential switched-capacitor crystal oscillator[3].

The limitation is not about the nettype's capability, it's about the never-ending balancing of modeling: accuracy vs speed. As capacitor and inductor modeled by VIR format rely on an internal clock. In order to achieve the required resolution of crystal device and internal switched-cap circuits, the internal clock period is at sub-Nano second level. The high throughput time can be barely paid at the block level simulation, but it's unacceptable at the chip level simulation where the Xtal is used as a main clock source.

When looking at the switched-cap circuit, the design focuses on the charge-redistribution. And the capacitor model of VIR format model with internal clock implements such feature by calculating how much charge is transferred within specified time period. But looking at the referenced crystal oscillator circuit[3], it relies more on the end-result of charge-redistribution, the circuits are designed to achieve the ideal situation where all the charges are properly transferred. From this perspective, aiming for the ideal behavior of the referenced crystal oscillator, the model can just give the resolved voltage after charge-redistribution, and skip the procedure of charge transition over time. To serve this purpose, the SV UDN structure has been redefined as {Voltage, Charge, 1/Capacitance}, which is named as VQC format and is presented in this paper.

The Nettype resolution function determines how the net is resolved with multiple inputs attached to the net. Within the VIR format resolution function for the normal unsaturated situation, the UDR sums all the currents (*IT*) and conductance (*GT*) from inputs and puts *IT/GT* as the resolved *V* element, and 1/*GT* as the resolved *R* element. The resolved *I* element is set to zero for obeying the Kirchhoff's current law.

Then, let's consider the situation of multiple charged capacitors connected by switches. Before connection, let's name the charge and capacitance in pairs as {*Q1*, *C1*}, {*Q2*, *C2*} and {*Q3*, *C3*}. Assume all capacitors' bottom plates are connected to ground, and top plates shall be connected to the node CapTop. Then, when all the capacitors' top plates are connected, the resolved voltage would be (*Q1*+*Q2*+*Q3*)/(*C1*+*C1*+*C3*). If we use '{0, *Q*, 1/*C*} to represent the contribution of charged capacitor to its connected SV UDN. Then following the UDR, the summed "Current" (*IT*) and "conductance" (*GT*) are:

$$IT = Q1 + Q2 + Q3 \tag{1}$$

$$GT = \frac{1}{1/C1} + \frac{1}{1/C2} + \frac{1}{1/C3} = C1 + C2 + C3 \tag{2}$$

Then we can find the resolved *V* element and *R* element are:

$$CapTop.V = \frac{IT}{GT} = \frac{Q1+Q2+Q3}{C1+C2+C3} \tag{3}$$

$$CapTop.R = \frac{1}{GT} = \frac{1}{C1+C2+C3} \tag{4}$$

So, the resolved *V* element is the exact voltage after charge redistribution among the connected capacitors, and the total capacitance can be retrieved from the resolved *R* element. On top of this, the summed "current" in the UDR also includes the contribution from the *V* element. So, an alternative definition of the charged-capacitor based VIR format is '{*V*, `*wrealZState*, 1/*C*}. When using it, the charge stored at the capacitor is calculated on the fly for summed "current" by the UDR as following.

$$IT = \frac{V1}{1/C1} + \frac{V2}{1/C2} + \frac{V3}{1/C3} = V1 * C1 + V2 * C2 + V3 * C3 = Q1 + Q2 + Q3 \tag{5}$$

According to the UDR, when both *V* and *I* elements have the value of `*wrealZState*, then the corresponding assignment is skipped for the net resolution. Then this can be used to model a cap has been removed from the node. From this point of view '{*V*, `*wrealZState*, 1/*C*} has an advantage that only one element needs to be changed. But '{0, *Q*, 1/*C*} has the flexibility to allow different equation rather than *Q*=*VC* for modeling different circuits. Both formats are used in the presented model to ease the coding.

The VQC format has been used to model a crystal devices and driver blocks. On the other hand, the internal differentiator, peak-valley detector and clock buffer are modeled in the VIR format. As these blocks only look at the voltage level appears at the crystal terminals, thus the conflicting *R* element between VIR and VQC format can be ignored. When putting all sub-blocks together, a model for a fully differential 40MHz switched-capacitor crystal oscillator presented in ESSCIRC 2022[3] has been implemented. As VQC format is strictly used only for the pins connected to the two terminals of crystal device, thus all other pins of Xtal oscillator are still in VIR format or logic signals. Then the Xtal oscillator model can be easily integrated into chip-level simulation, where other blocks are using VIR format.

The Xtal oscillator block has been simulated in both schematic and model. Due to the sub-block level modeling, the VQC model accurately mimics the schematic of the oscillation of crystal, especially the startup phase. On top of this, the Xtal oscillator model gives proper transient response of changing the trimming capacitor over time, which is aligned with theoretical behavior. Such simulation is not feasible for schematic simulation due to long through put time. When comparing the CPU time over the transient analysis stop time, the new VQC model gives 90,000x simulation speed boost. Thus, both the block level design and chip-level integration verification are benefited from the new VQC model.

Reference

[1] A. Caicedo, and S. Fritz, "Enabling Digital Mixed Signal Verification of Loading Effects in Power Regulation using System Verilog User-Defined Nettype", DVCON EUROPE, Munich, October 2019

[2] S. Li, T. Yang, A. Huq, "Accurate Charge-pump Regulator Modeling using SV EEnet", DVCON China, Shanghai, May 2021.

[3] W. Kruiskamp, "A Fully Differential 40MHz Switched-Capacitor Crystal Oscillator with Fast Start-up", ESSCIRC, Italy, Milan, Sep 2022.