2026
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
UNITED STATES
SANTA CLARA, CA, USA
MARCH 2 - 5, 2026

System Validation

“It’s the Protocol Stupid”

Johannes Stahl, Varun Agrawal, Rob Parris - Synopsys

Agenda

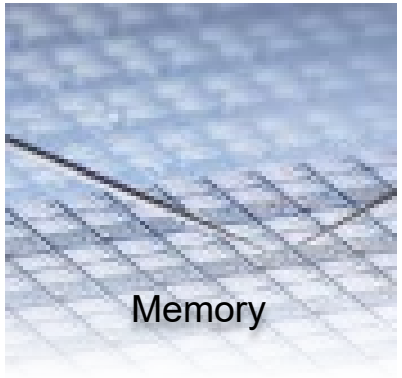
- High Performance Interface Protocols – Essential for AI
- 10 out of 10: Interface Solutions for Successful System Validation
- Interface Solutions and Video Demos
- Summary and Q&A

Live Demos
Visit Synopsys on the show floor

High Performance Interface Protocols – Essential for AI

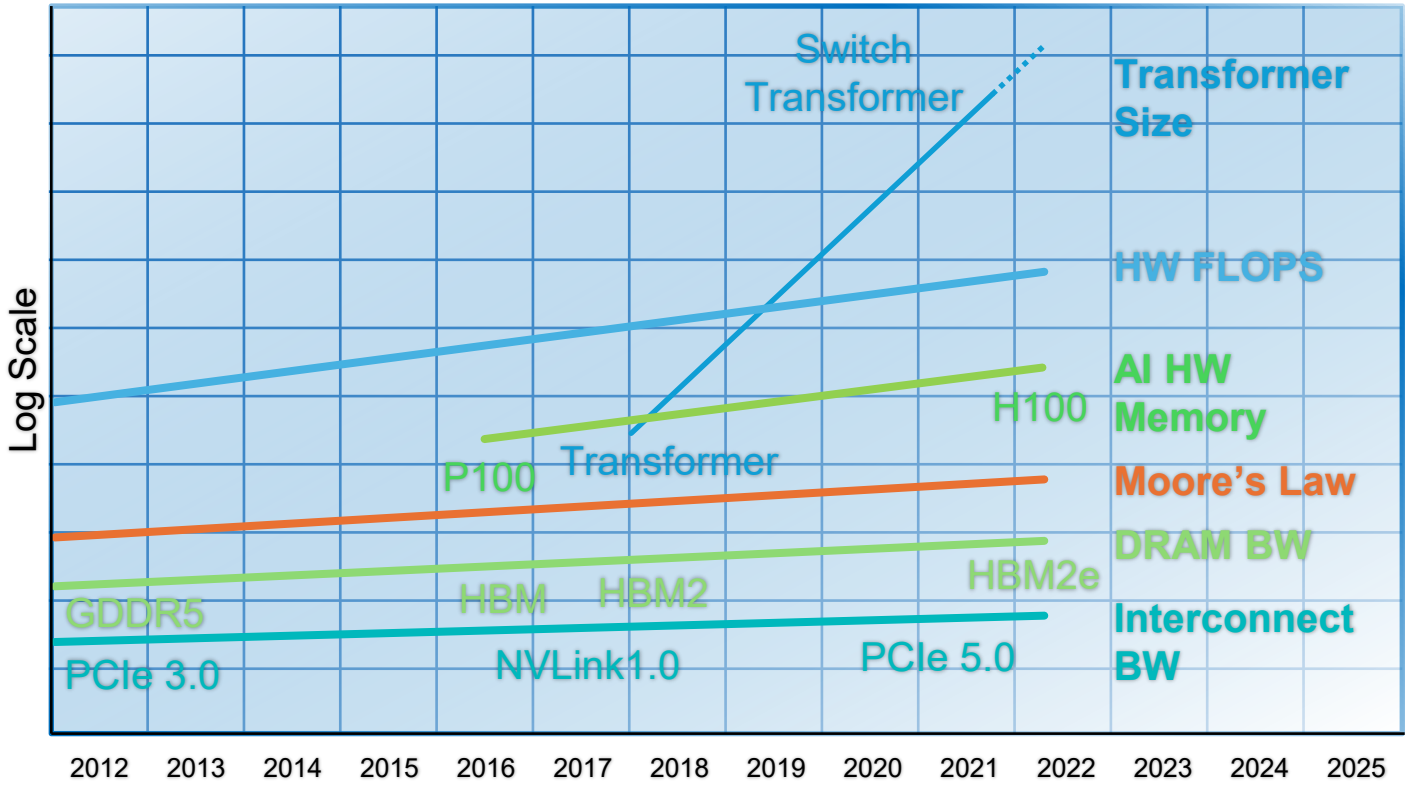
Era of Pervasive Intelligence

Semiconductors Appear Everywhere

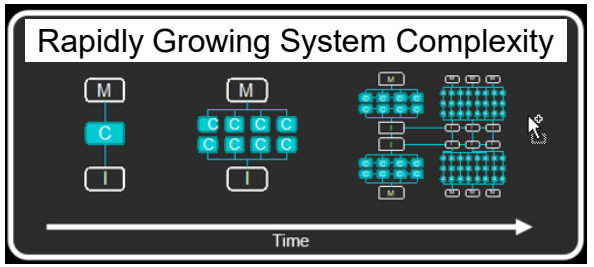


AI Drives New Design Paradigms

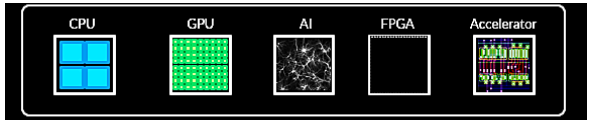
The need for hardware scaling leads to new architectures and design approaches



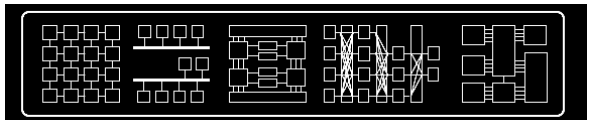
Wide range of optimizations & innovations



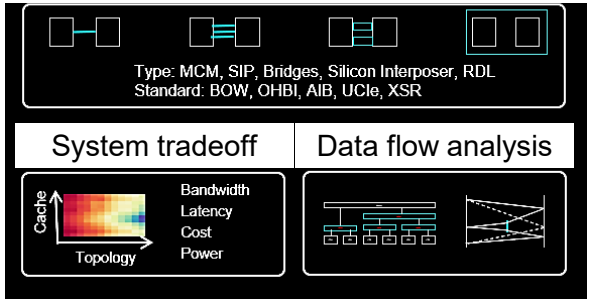
Optimal mix of compute type per workload



Fabric & cache innovations to accelerate data



Careful optimization of chiplet interface



Transformer Size: 410x / 2yrs

HW FLOPS: 3.0x / 2 yrs, 60000x / 20 yrs

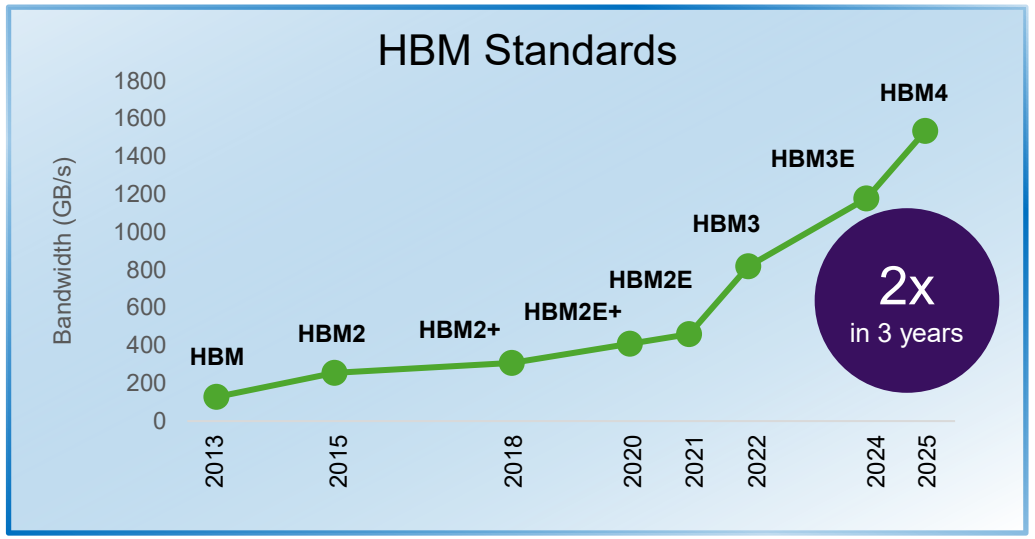
AI HW Memory: 2x /2 yrs

DRAM Bandwidth: 1.6x / 2 yrs

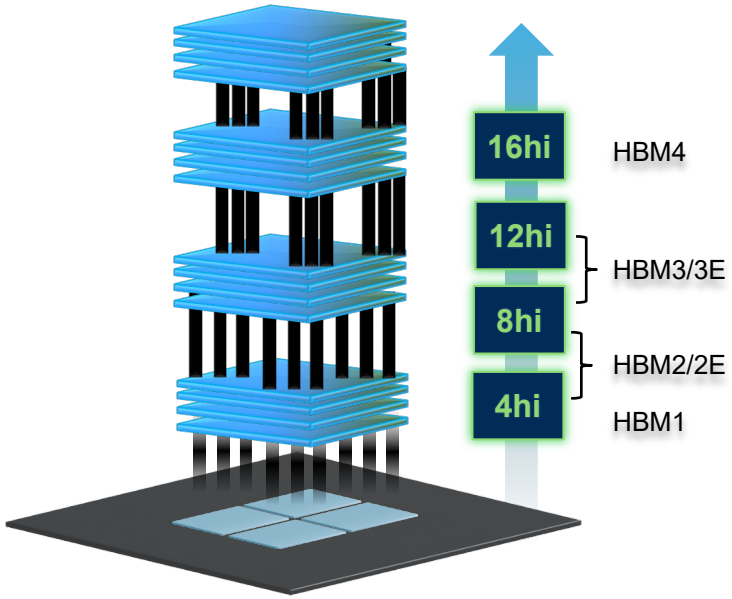
Interconnect Bandwidth: 1.4x / 2 yrs

Source: AI and Memory Wall: 2403.14123 (arxiv.org), Baya Systems @ EETimes Chiplet Summit

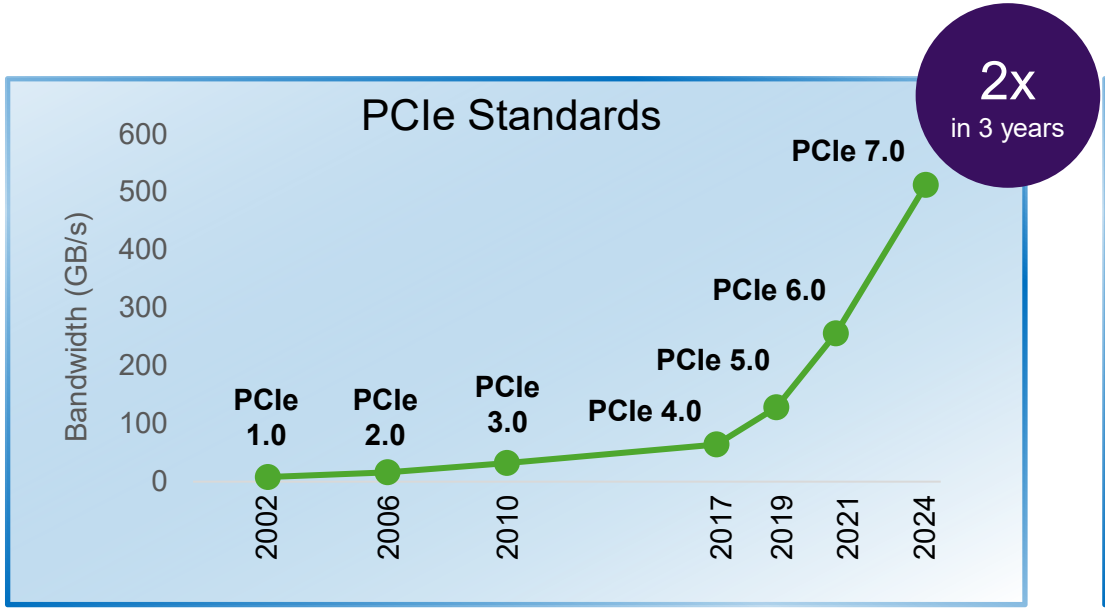
AI Demands Extreme Memory BW



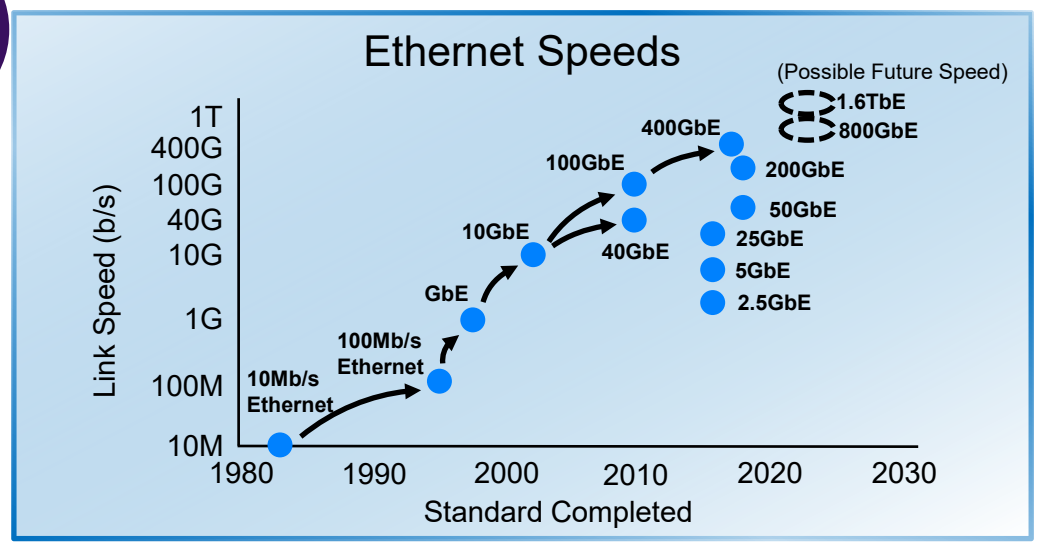
Source: Standards Bodies



AI Demands Extreme Interconnect BW



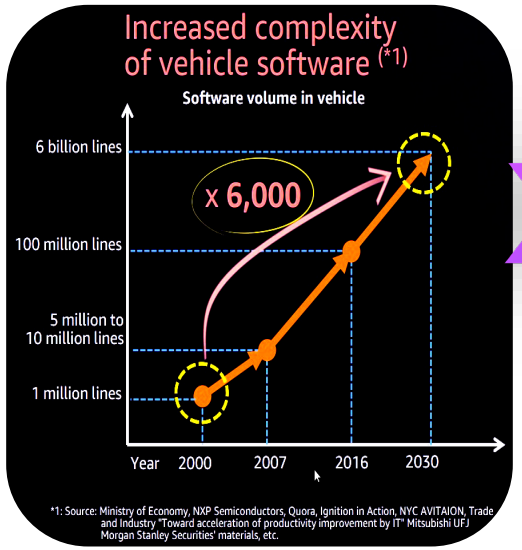
Source: Meta, OCP Summit Presentation



Source: Ethernet Alliance

Compounding Complexities

Software



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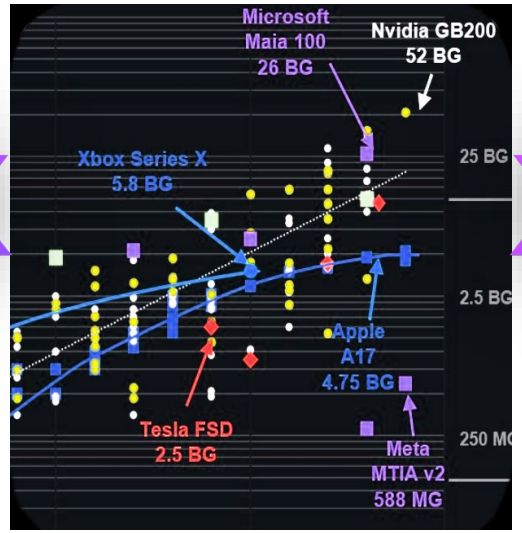
Hardware



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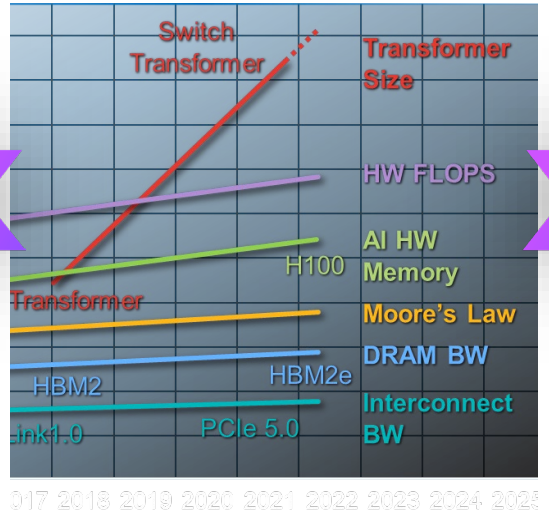
Interfaces



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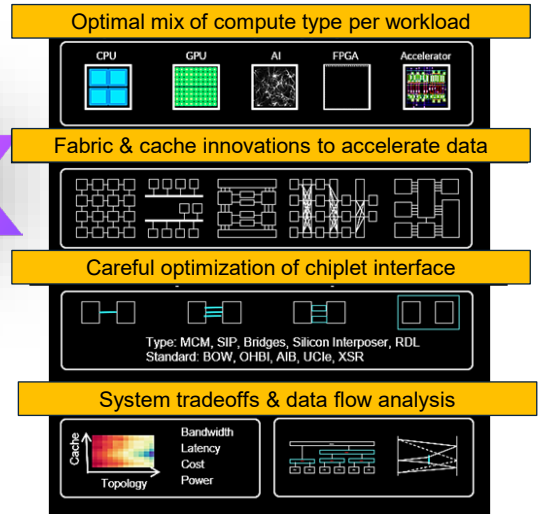
Architectures



Source: AWS, Synopsys, AI and Memory Wall: 2403.14123 (arxiv.org), Baya Systems, *"What Makes RISC-V Verification Unique?" https://bit.ly/4hDXCe9

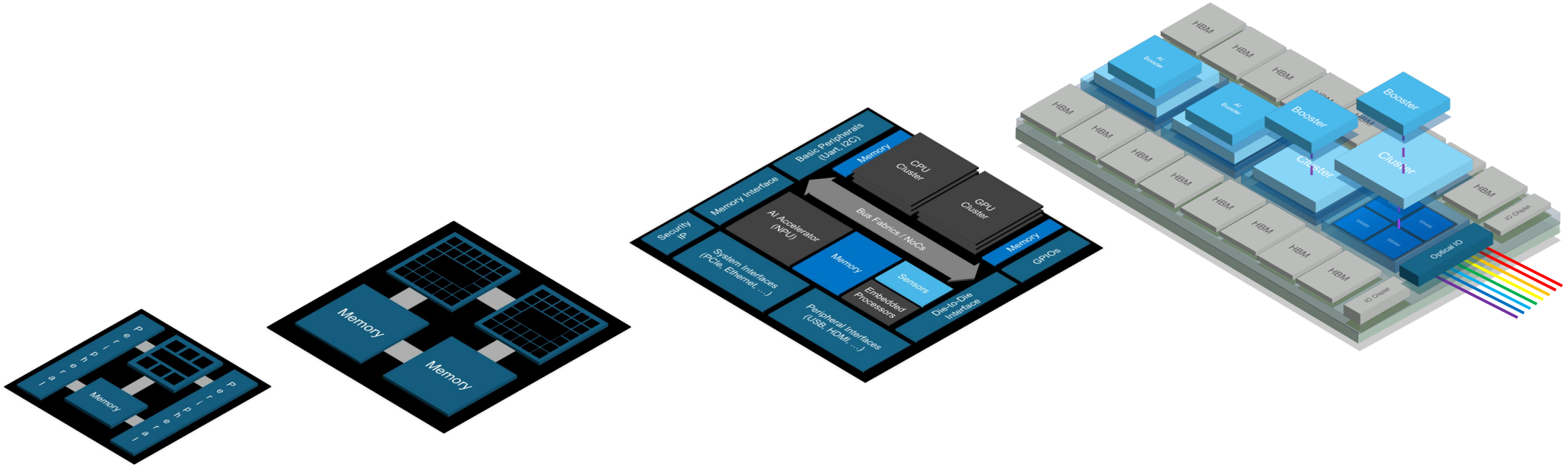
Verification Challenge: Quadrillions of Cycles*

10 out of 10:
Interface Solutions for Successful System Validation

Verification Happens in Phases – Quadrillions of Cycles!

Simulation **Silicon**

Hardware-Assisted Verification



IP/Core Centric → **Subsystem / Software** → **Full Chip(let) / Software** → **Multi-die / Software**

IP | Virtual Model | VIP | HAV Protocol Solution

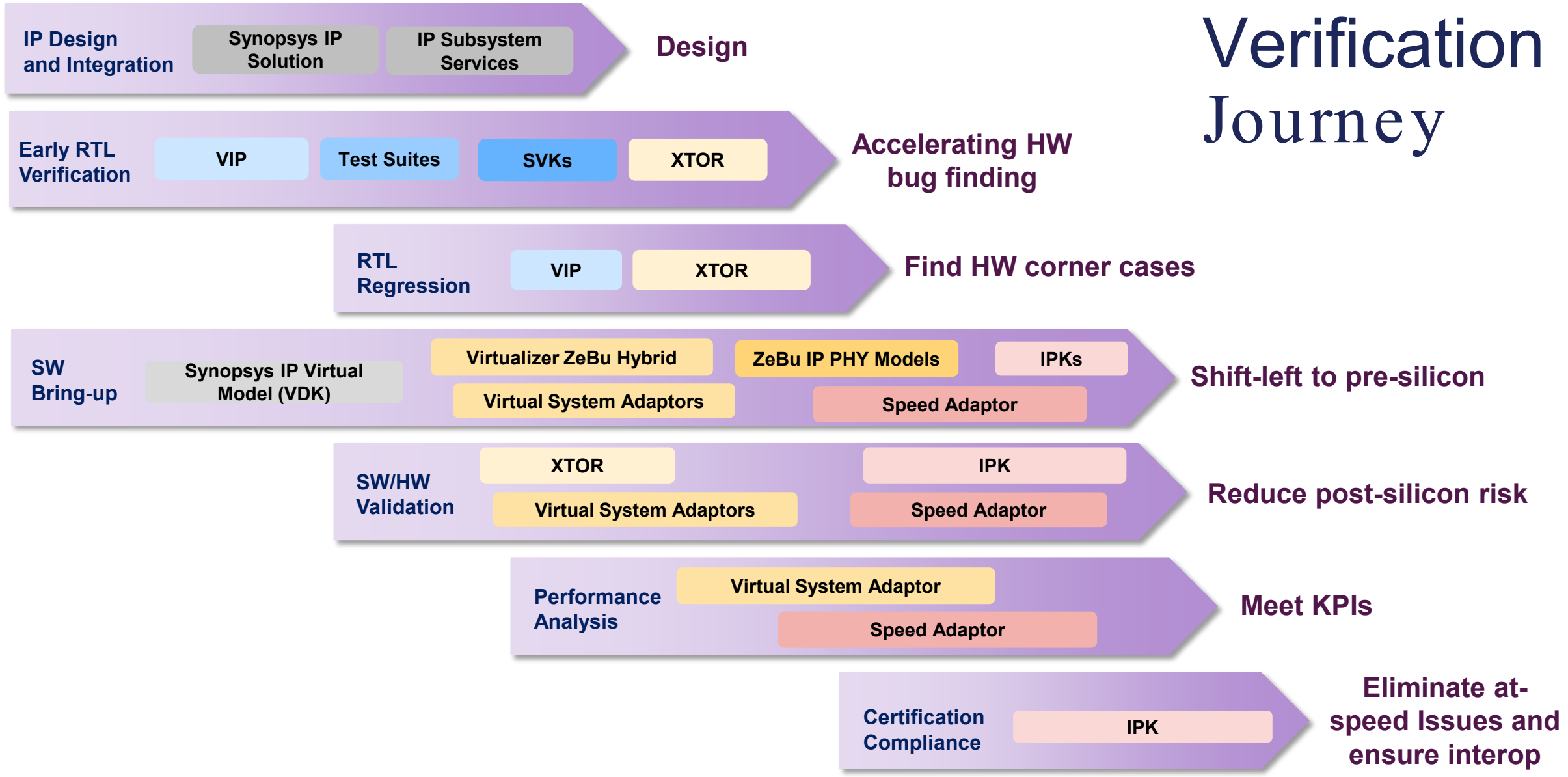
What you need:

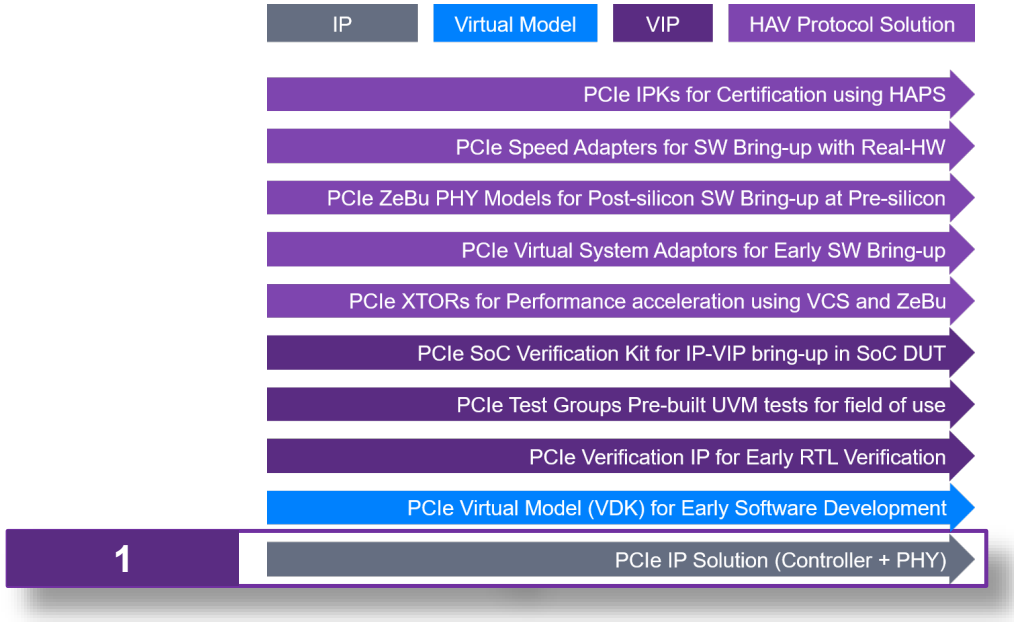
10 out of 10 Interface Solutions

Example: PCIe

- PCIe IPKs for Certification using HAPS
- PCIe Speed Adapters for SW Bring-up with Real-HW
- PCIe ZeBu PHY Models for Post-silicon SW Bring-up at Pre-silicon
- PCIe Virtual System Adaptors for Early SW Bring-up
- PCIe XTORs for Performance acceleration using VCS and ZeBu
- PCIe SoC Verification Kit for IP-VIP bring-up in SoC DUT
- PCIe Test Groups Pre-built UVM tests for field of use
- PCIe Verification IP for Early RTL Verification
- PCIe Virtual Model (VDK) for Early Software Development
- PCIe IP Solution (Controller + PHY)

Verification Journey





Interface IP

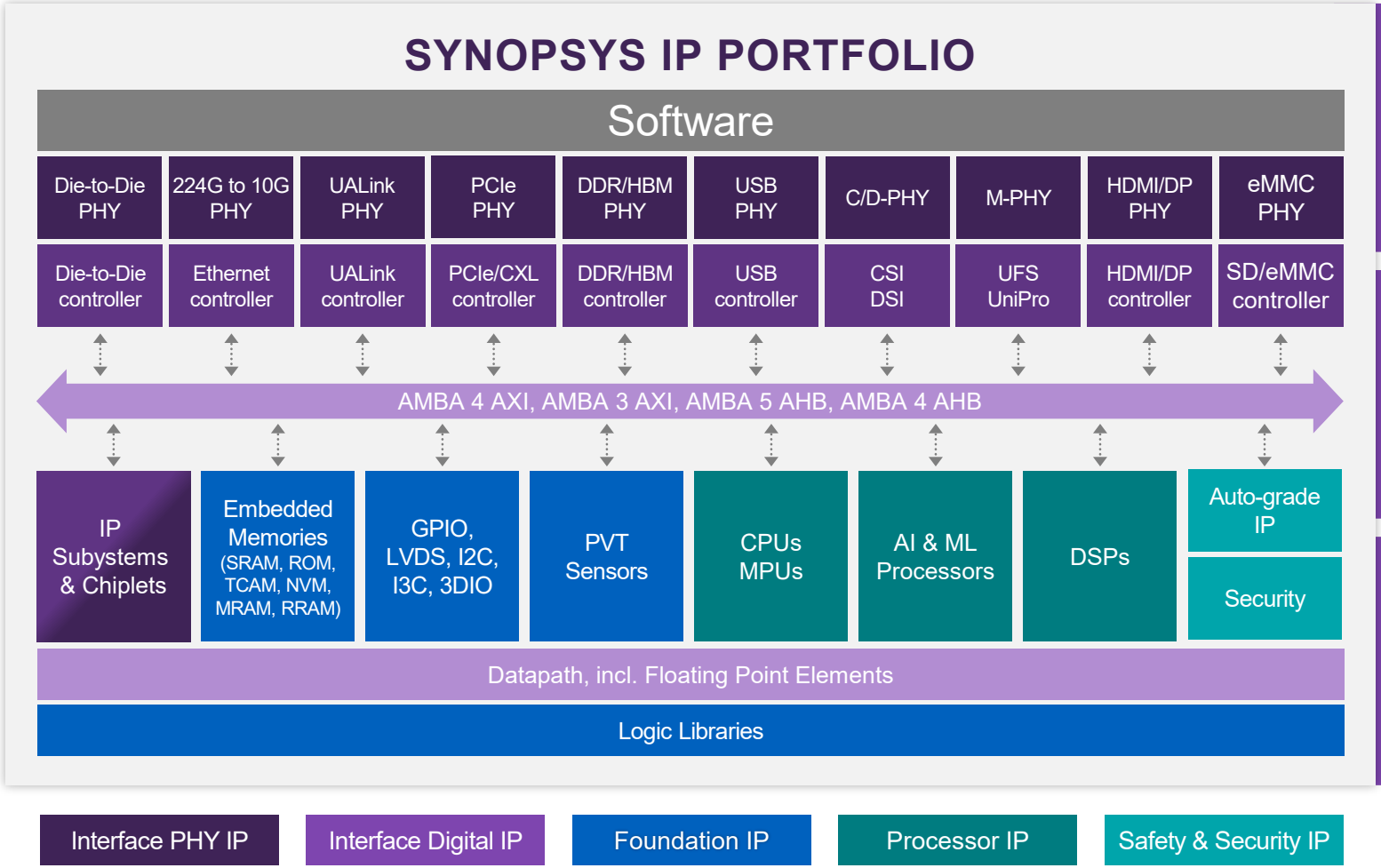
Interface Solution and Demo

Interface IP

Verification Challenge	Interface Solution	Value
• Protocol Compliance and Coverage • Interoperability and Integration • Debugging and Observability	• Leading member of standards organizations • Comprehensive validation with VIPs, HAV and test silicon • Compliance certifications	• High Compliance and Interoperability • Performance and Scalability • Comprehensive support

Synopsys IP Validation

Leveraging Synopsys VIP, VCS, Verdi, ZeBu and HAPS Verification Continuum Technologies



Broadest Portfolio

Foundation IP, interfaces, security, processors, subsystems

Highly Differentiated

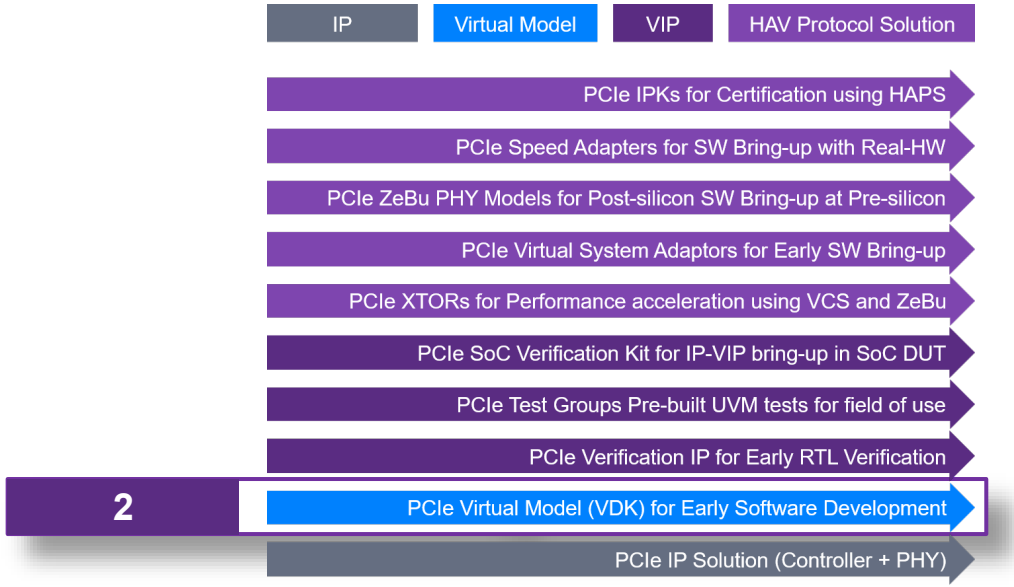
Delivering IP at the cutting edge of functionality and process technology across key markets

Committed to Your Success

Complete solution partner to enable faster time to market and first-time-right silicon

Interface PHY IP | Interface Digital IP | Foundation IP | Processor IP | Safety & Security IP

Synopsys PCIe 6 IP Demonstration



Virtual Model

Interface Solution and Demo

Virtual Models

Verification Challenge

- Growing SW complexity
- SW/HW integration
- HW can't be verified without SW

Interface Solution

- Virtualizer IDE for creation of virtual models
- Broadest model library for processors and interfaces
- Debug/analysis tools including 3rd party integration

Value

- Accelerated Software Development and Validation
- Improved Debugging and Observability
- Enhanced Collaboration and Productivity

Synopsys IP TLM Library

Developed from IP Spec – Validated against IP RTL

Interface IP
- PCIe
- CXL
- UCIe
- USB
- Mobile Storage
- Ethernet
- MIPI
- SATA

SoC Infra
- DMAC
- Interrupt Controller
- Timer
- UART
- SSI
- I2C
- I2S
- GPIO

Generic Models
- UART PHY
- Ethernet PHY
- SSD/MMC Device
- UFS Device
- USB Devices
- SPI Flash

Building Blocks
- NVMe
- DMA
- TCP
- Nand Flash
- Protocol Engines

- Highly configurable to match the application
- Virtual & Real-World I/O for connectivity
- FastTrack for debugging configuration issues
- Logging of internal state and operations

Synopsys Virtualizer Overview

VDK creation from TLM Models – VDK use for Early SW development

Virtualizer

Interface IP
- PCIe
- CXL
- UCIe
- USB
- Mobile Storage
- Ethernet
- MIPI
- SATA

SoC Infra
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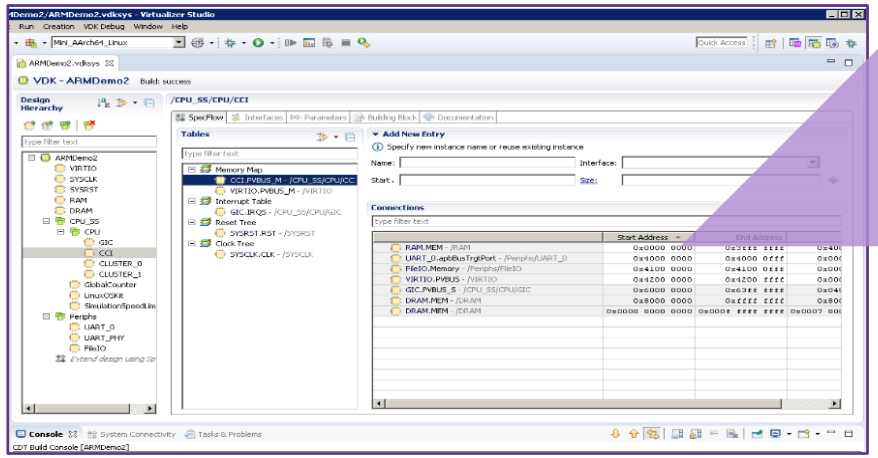
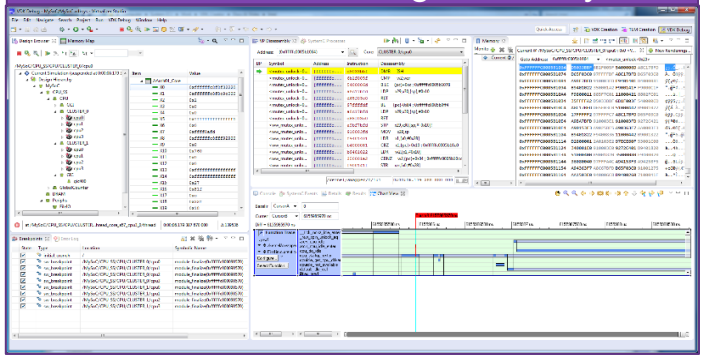


Virtualizer Development Kit (VDK)

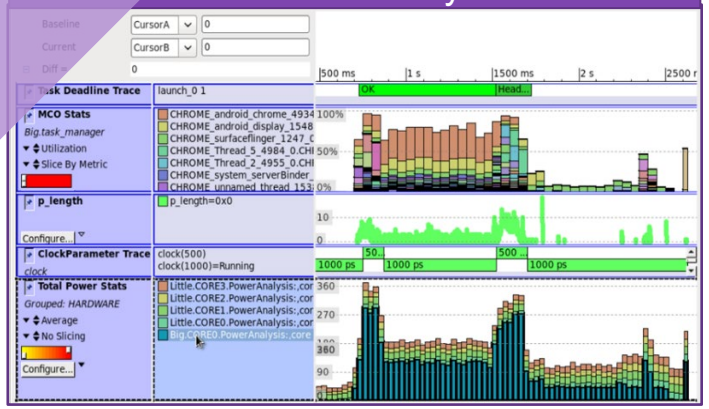
Embedded SW Debug

LAUTERBACH DEVELOPMENT TOOLS
Green Hills SOFTWARE
ARC Synopsys
ARM DS Development Tools
CEVA
IAR SYSTEMS
pls Development Tools
tensilica

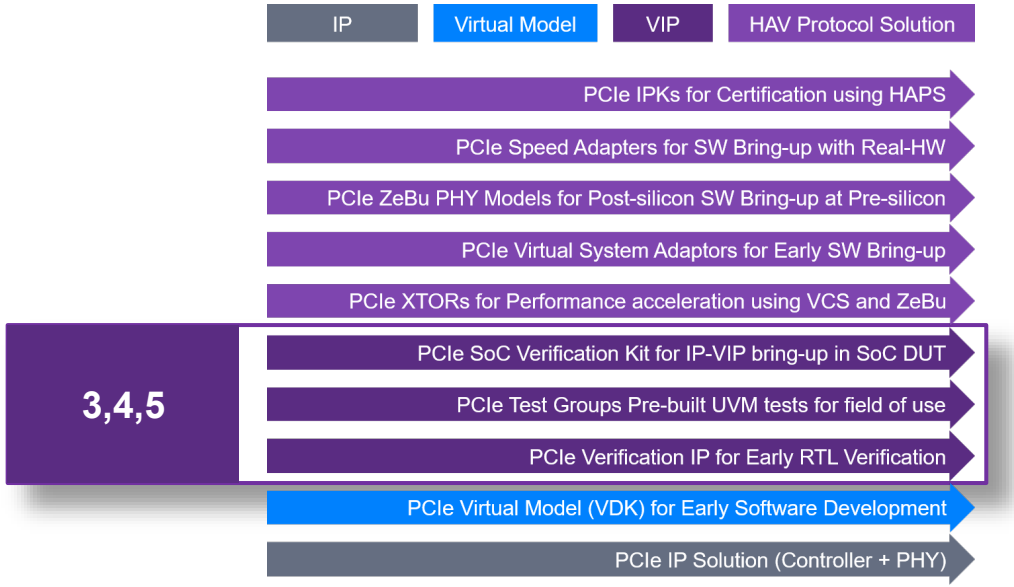
Embedded SW tracing and analysis



Hardware analysis



Transaction tracing and debug



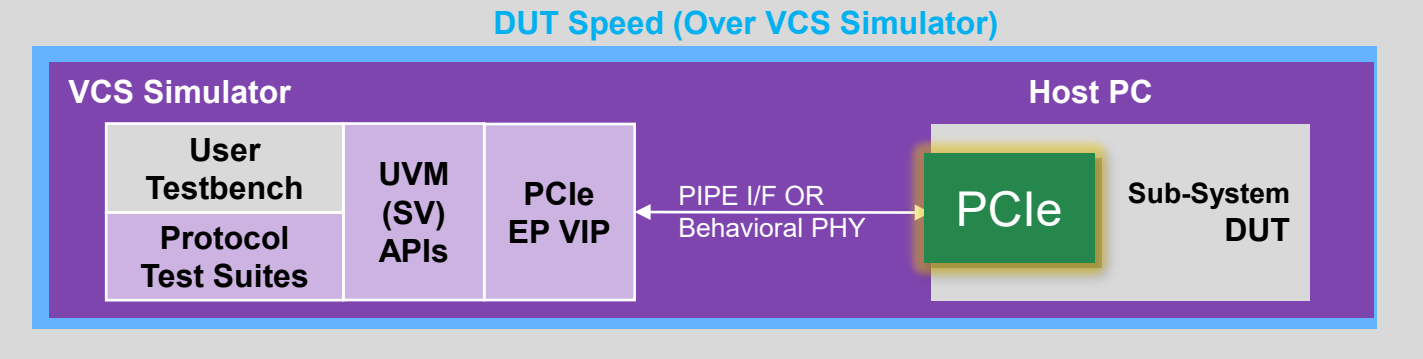
VIP, Test Groups, SoCVerification Kit

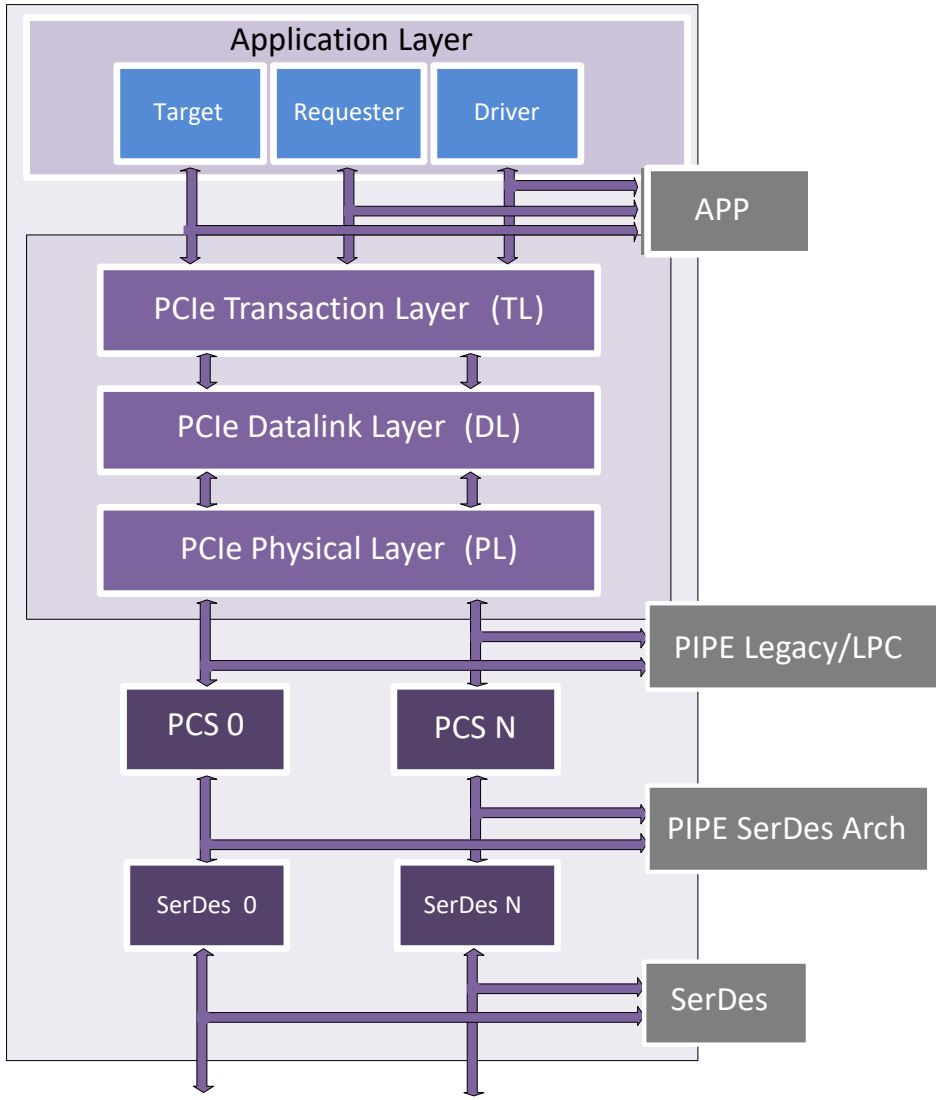
Interface Solution and Demo

VIP, Test Groups and SoC Verification Kits

Verification Challenge	Interface Solution	Value
• Protocol Compliance and Correctness • Test Coverage and Scenario Generation • Accelerated Debug and Productivity for SoC Integration	• Industry-first VIP • Use case specific test groups • Pre-integrated IP and VIP Kits for SOC Verification (SVKs)	• Latest standards • Quick bring-up • Deep bug hunting • Comprehensive coverage • Rapid SoC test bench

Early RTL Verification with VIPs





- Behavioral models for Protocols/PHYs
- Connects to DUT through PIPE I/F or PHY I/F
- Complete setup runs on Host PC at DUT speed
- Thorough protocol implementation and checkers (preserves protocol sequence)
- Specification-mapped verification plan, PCIe EP VIP, Test Suites, Highest debug productivity, multiple RTL-turns a day

SOC TB Acceleration with SVK

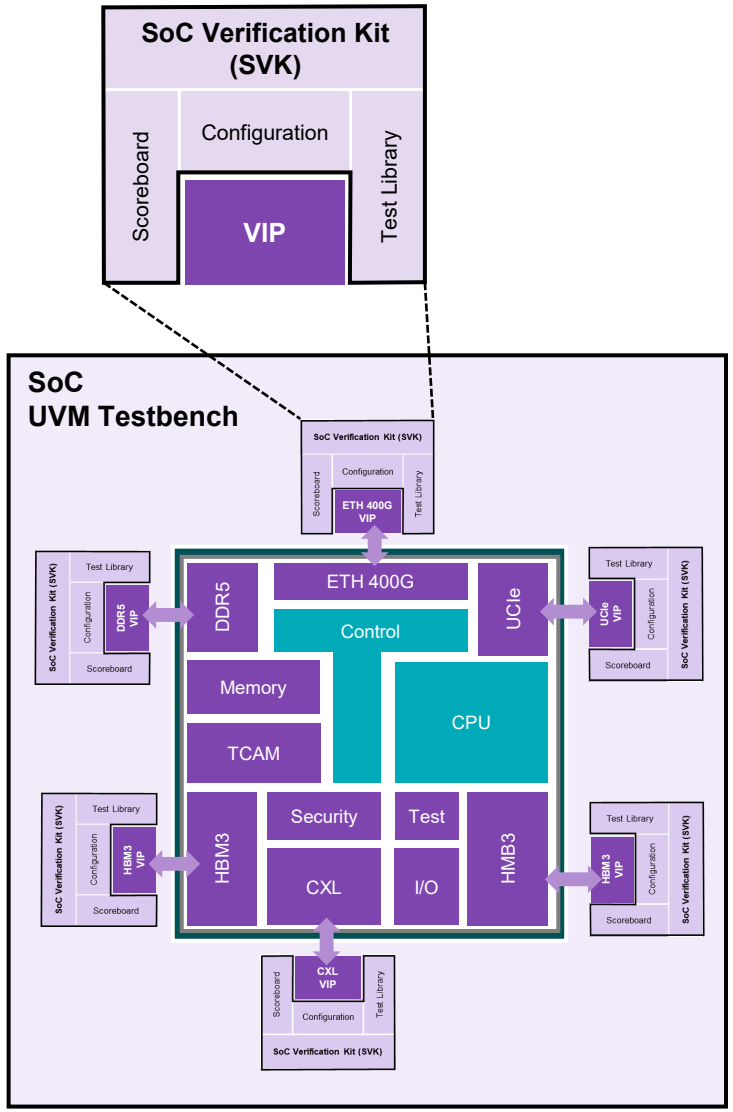
Pre-Integrated Verification solution for Synopsys Interface IP

Challenges

- Expertise for UVM-based, C-based/Application testbenches
- Verification resource limitations
- Time to setup creation and reusability

SVK Benefits

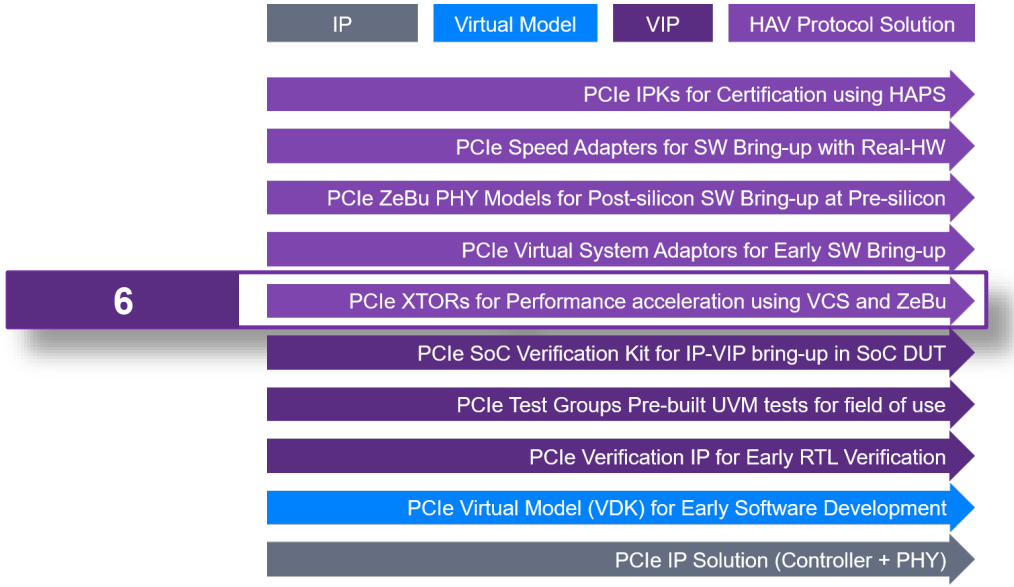
- Out-of-the-box verification solution for complex protocols
- Tailor made for project-specific IP configuration
- Accelerates the SoC testbench development
- Enables testing of Synopsys IPs in Subsystem/SoC environment
- Lowers integration risk through proven verification methodologies



Test Groups Are Aligned with IP Configuration

- ✓ Link Up
- ✓ Inbound and Outbound Transfers
- ✓ Speed Control
- ✓ Link Width Control
- ✓ Power Management
- ✓ Loopback
- ✓ Random Link Down (unplug)
- ✓ Polarity Inversion
- ✓ LTSSM transitions (Hot Reset, Disabled..)
- ✓ Physical Layer (Normal & Error)
- ✓ Data Link Layer (Normal & Error)
- ✓ Transaction Layer (Normal & Error)
- ✓ Precoding
- ✓ EQ via Loopback

Protocol feature	Sub feature	Test #	Subsystem features tests
DUT integration Link up Basic traffic	PCIE rates only Inbound/Outbound traffic in L0	3	1) ts.base_serdes_test.sv 2) test_linkup_to_max_speed.sv 3) ts.test_linkup_to_gen2_speed.sv
Speed control	Random change	1	ts.test_all_speed_changes_from_gen1_to_max_speed.sv
Link width control	Random change	1	ts.test_downconfigure_upconfigure.sv
Power management	ASPM L1	1	ts.test_l1_power_state.sv
	PM L1	1	ts.test_l1_power_state.sv
	L2	1	ts.test_l2_power_state.sv
	L0s	2	1) ts.test_rx_l0s_to_l0.sv 2) ts.test_tx_l0s_to_l0.sv
Loopback	Master/Slave	1	ts.test_loopback.sv
Link down	Mid sim reset	1	ts.test_mid_sim_reset.sv
Polarity Inversion	Inverted polarity	1	ts.test_polarity_inversion_lane_reversal.sv
Receiver Detection	Detecting receiver	NA	Already covered under tests listed in this column from rows 4-19
LTSSM transitions	Various LTSSM transitions as per specification	2	1) ts.test_disable_to_detect_state.sv 2) ts.test_hot_reset.sv
Framing	Error scenarios	1	ts.test_framing_error.sv
PPM	SRNS/SRIS	1	ts.test_dut_clk_compensation_with_ppm.sv
Data Link Layer	Normal/Error scenarios	3	1) ts.test_corr_err_lcrc.sv 2) ts.test_low_credits_backpressure.sv 3) ts.test_nak_retries_followed_by_link_retrain.sv
Transaction Layer	Normal/Error scenarios	9	1) ts.test_all_tlp_types.sv 2) ts.test_ep_dut_enumeration.sv (EP DUT only) 3) ts.test_inbound_mem_transaction.sv 4) ts.test_malformed_tlp_error.sv 5) ts.test_max_payload_size.sv 6) ts.test_mem_access_cross_4k_boundary.sv 7) ts.test_pcie_outbound_traffic.sv 8) ts.test_pcie_outbound_traffic_to_invalid_range.sv 9) ts.test_performance_with_max_payload.sv



Transactors

Interface Solution and Demo

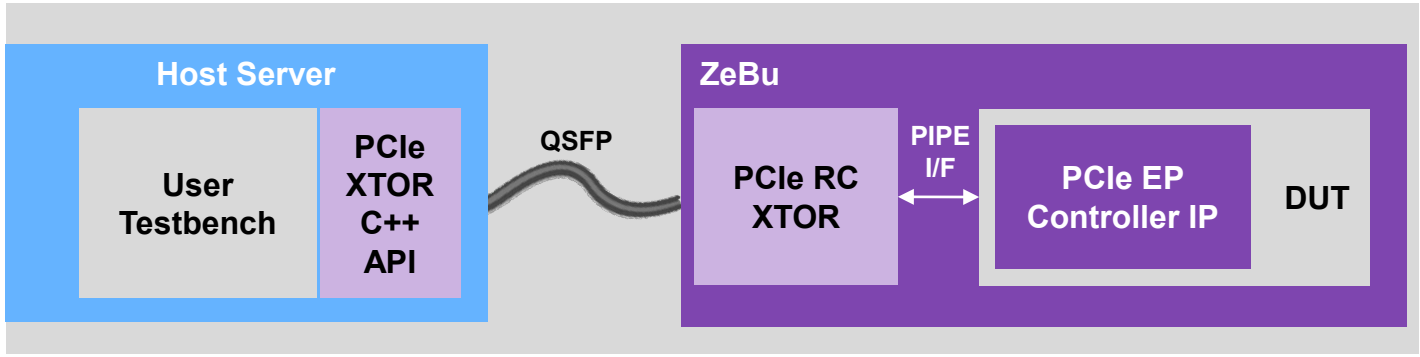
Transactors

Verification Challenge	Interface Solution	Value
• System scenario complexity • Protocol complexity • Performance Measurements • Emulation efficiency	• Protocol translation from transaction-level in SW to pin-level in HW • Functional and performance visibility into the protocol through monitors	• Best throughput • Early availability • Scalablity • Alignment with Synopsys Interface IP

Transactors Enable Protocol Validation

XTORs are aligned and validated with Synopsys IP

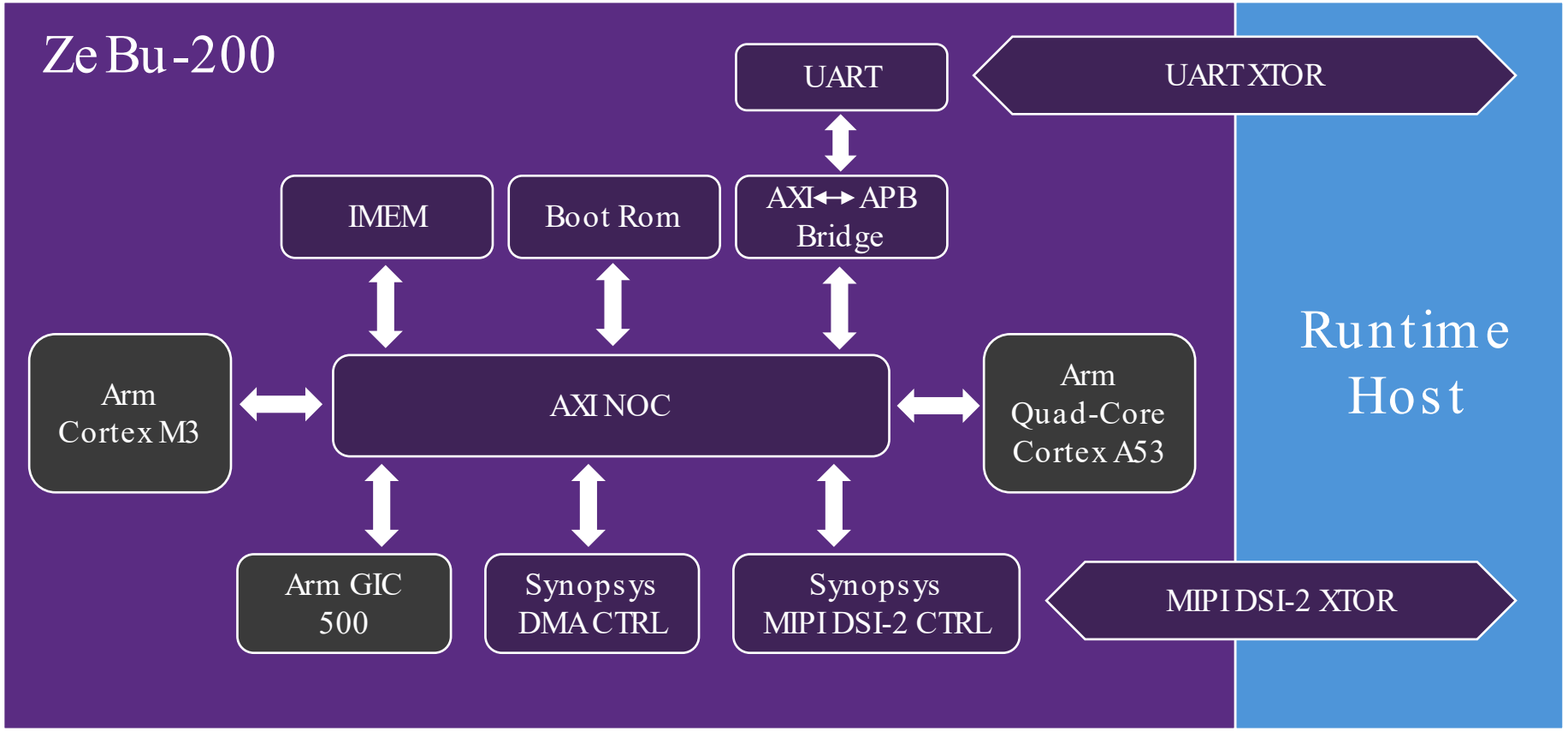
ZeBu Transactor (XTOR)

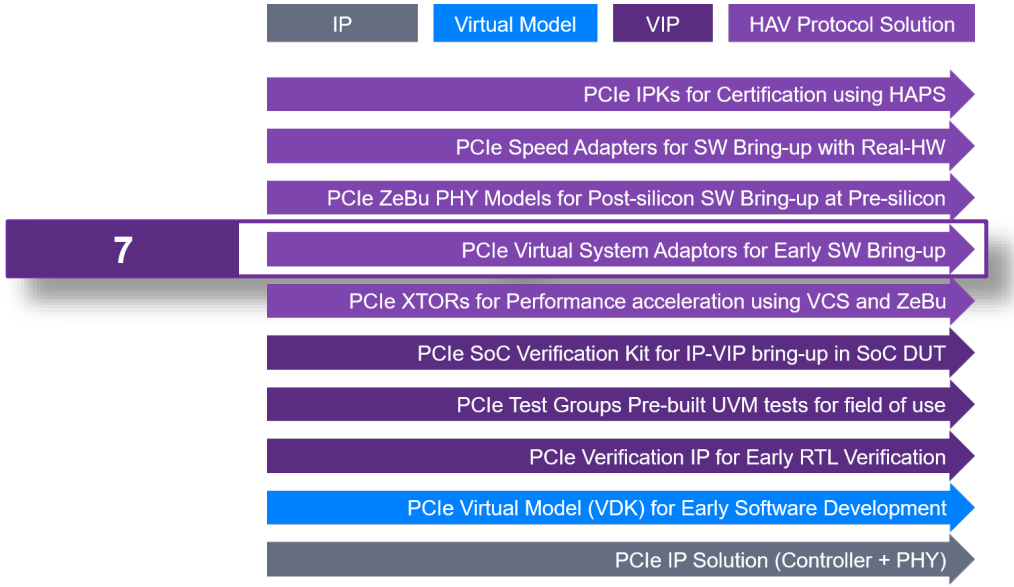


- DUT PHY IP replaced by a XTOR lane or PHY model
- Connects to DUT through PIPE I/F
- No real-world devices needed
- Virtual devices model run on Host PC
- Preserves protocol sequence

Transactor Demo: ARM Sub-system

Booting Linux and Executing Video Application





Virtual System Adaptors

Interface Solution and Demo

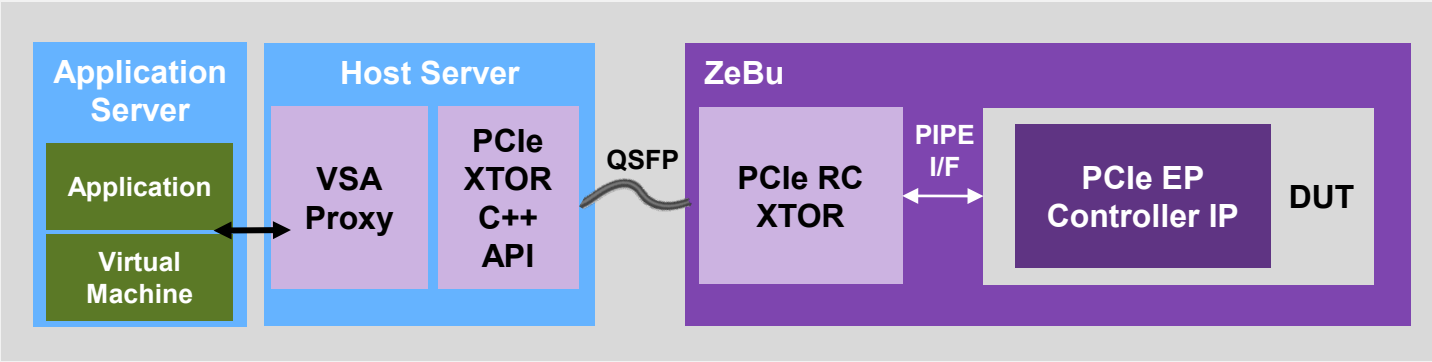
Virtual System Adaptors

Verification Challenge	Interface Solution	Value
• Driver, firmware development on target OS • System validation • Pre to post silicon sanity	• Virtual Host/Device Interface • Virtual Network Tester Interface • Arm architecture compliance with SBSA	• Early SW development • Pre-silicon networking validation • Arm system compliance

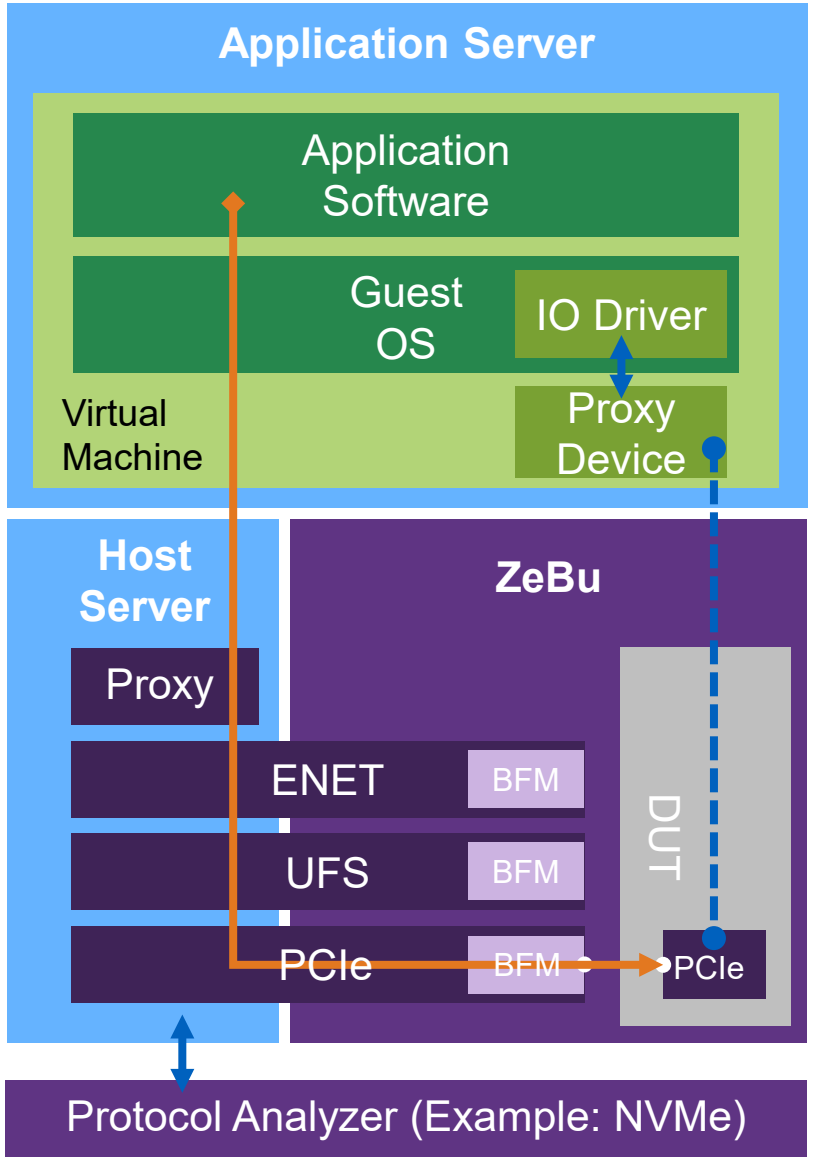
SW Development

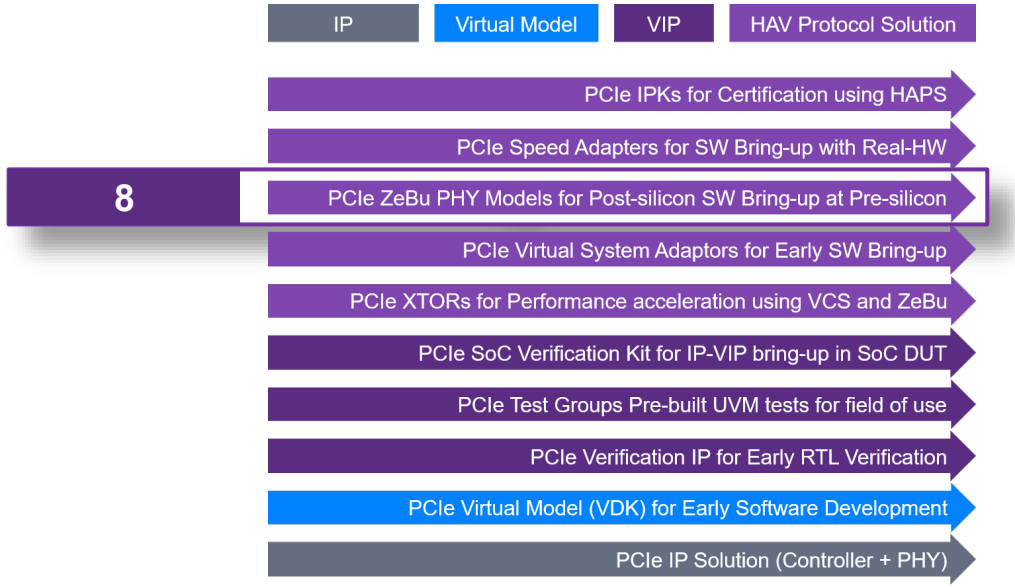
Synopsys IP works with ZeBu Virtual System Adaptors

ZeBu Virtual Host (Virtual System Adaptor)



- DUT PHY IP replaced by a XTOR lane or PHY model
- Connects to DUT through PIPE I/F or PHY I/F
- Real-world applications over Virtual Machine(QEMU) running on host PC
- Full setup runs at Multi-MHz DUT speed, preserves protocol sequence
- Simulation speed, system flow debug, software debuggers support, application platform support, rare RTL turns





ZeBu PHY Models

Interface Solution and Demo

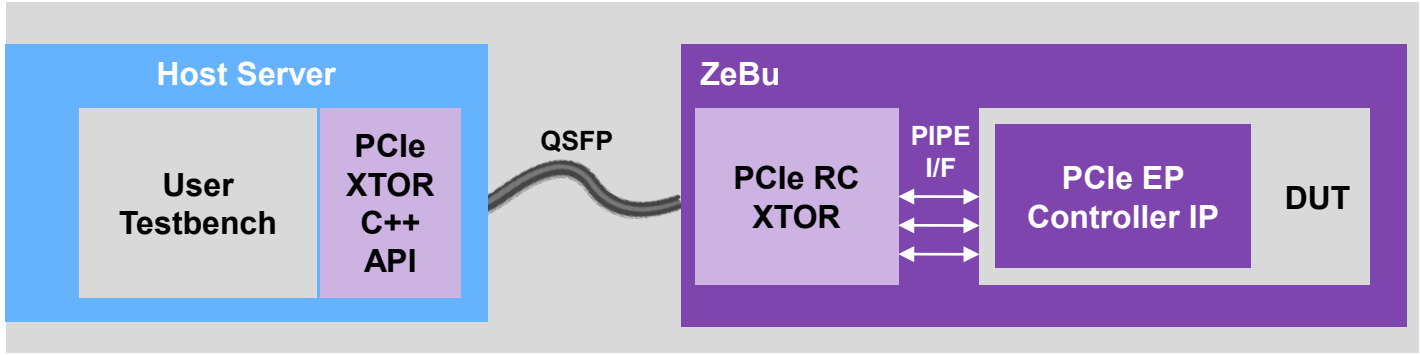
ZeBu PHY Models

Verification Challenge	Interface Solution	Value
• Post-silicon software and firmware Validation at pre-silicon • Post-silicon PHY integration • Full system/subsystem bring-up	• Synthesizable model of digital part of PHY • Aligned with customer configuration of PHY	• Accelerating driver and firmware • More complete system validation for the interface

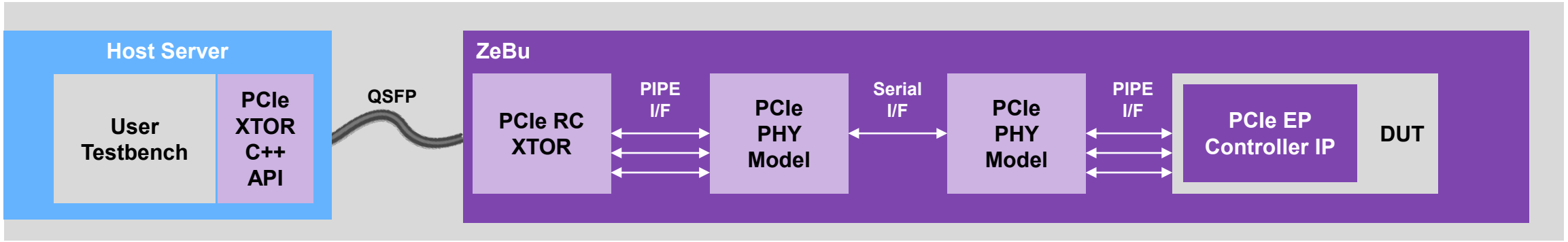
PHY Models enable additional Validation

Synopsys IP PHY models represent Customer IP configuration

ZeBu Transactor (XTOR) + Controller IP



ZeBu Transactor (XTOR) + Controller IP + PHY Model



When to Use PHY Models

Transactor + Controller IP

Use-Model

- Validation scope doesn't include PHY behavior
- Develop/validate software for other IPs or full SoC

Modeling Considerations

- No serial or analog component modeling
- Minimalistic PHY functionality support through lane models
- Better emulation performance

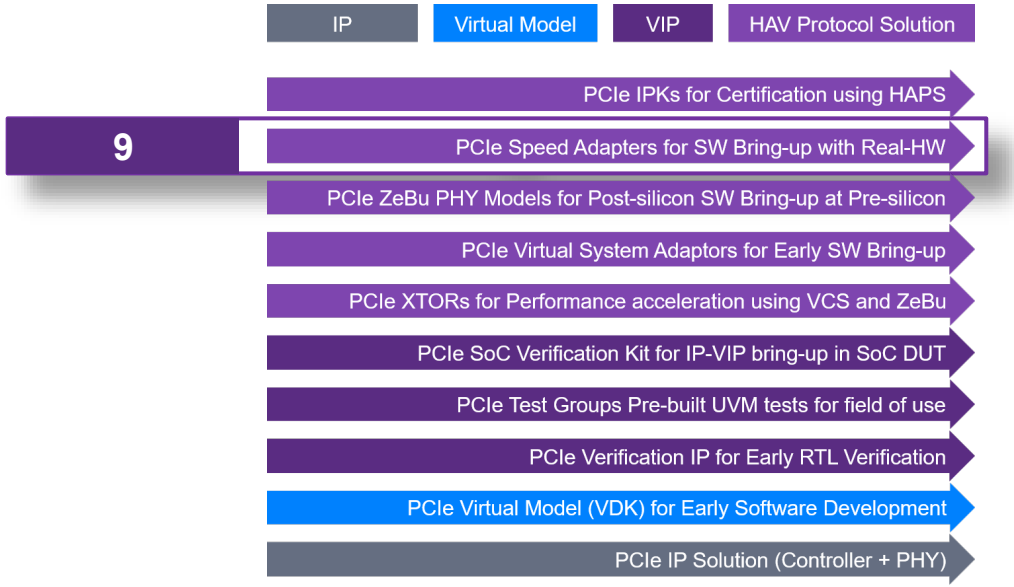
Transactor + Controller IP + IP PHY Model

Use-Model

- Validate scope and scenarios specific to configuration of Synopsys PHY IP
- Develop or run post-silicon software specific to the PHY IP

Modeling Considerations

- Digital PHY modeling only (no analog modeling)
- Slower emulation performance
- Potentially higher emulation capacity utilization



Speed Adaptors

Interface Solution and Demo

Synopsys Speed Adaptors

Verification Challenge

- Validation of real-world scenarios
- Eco-system interoperability
- Pre-silicon system integration

Interface Solution

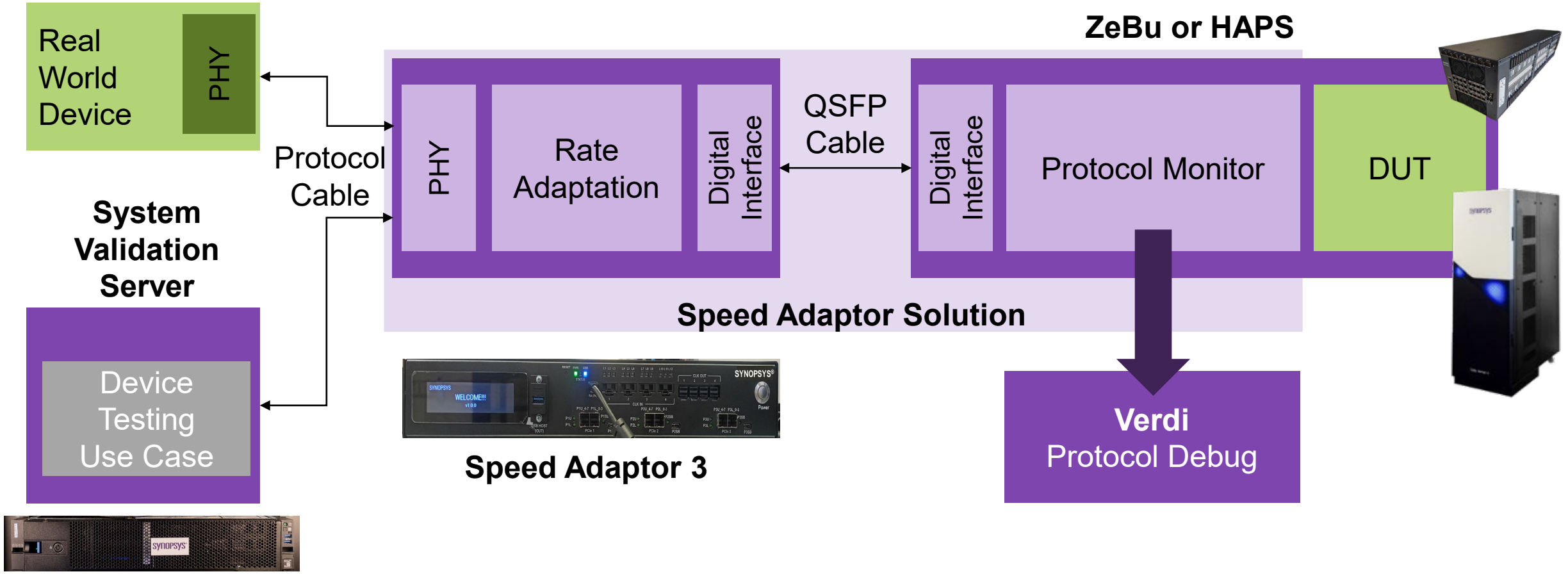
- Protocol compliant rate adaption
- Support for latest protocol version
- Validation server for accurate environment behavior

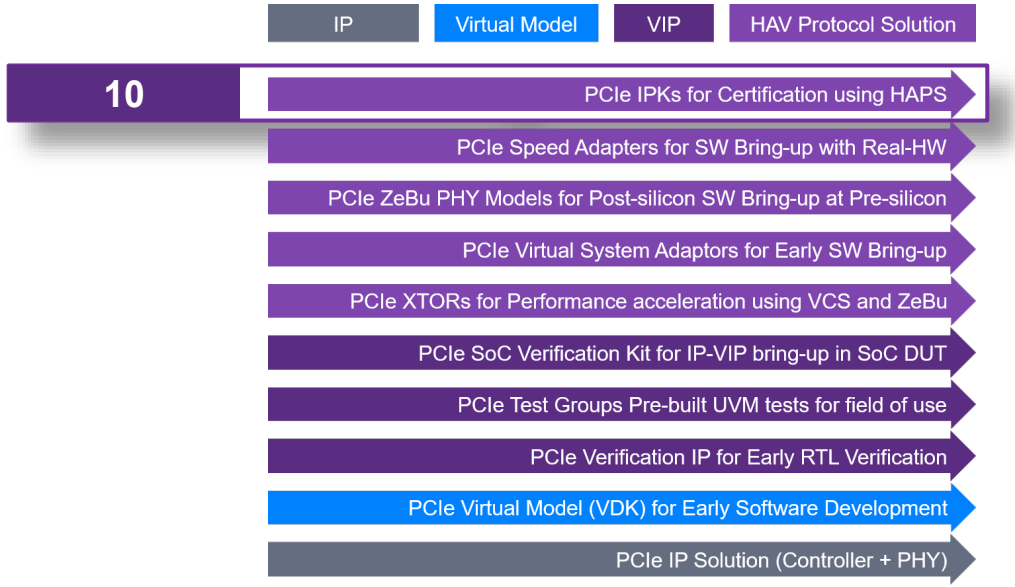
Value

- Eliminate validation gaps from synthetic tests
- Test interoperability with real systems

Protocol Compliant Speed Adaptor Solution

System Validation Server enables Protocol Compliance testing and manages SW rate adoption





Interface Prototyping Kit

Interface Solution and Demo

Interface Prototyping Kit

Verification Challenge

- Protocol compliance needs to be verified before tape-out
- Proven IP ≠ Protocol Compliance

Interface Solution

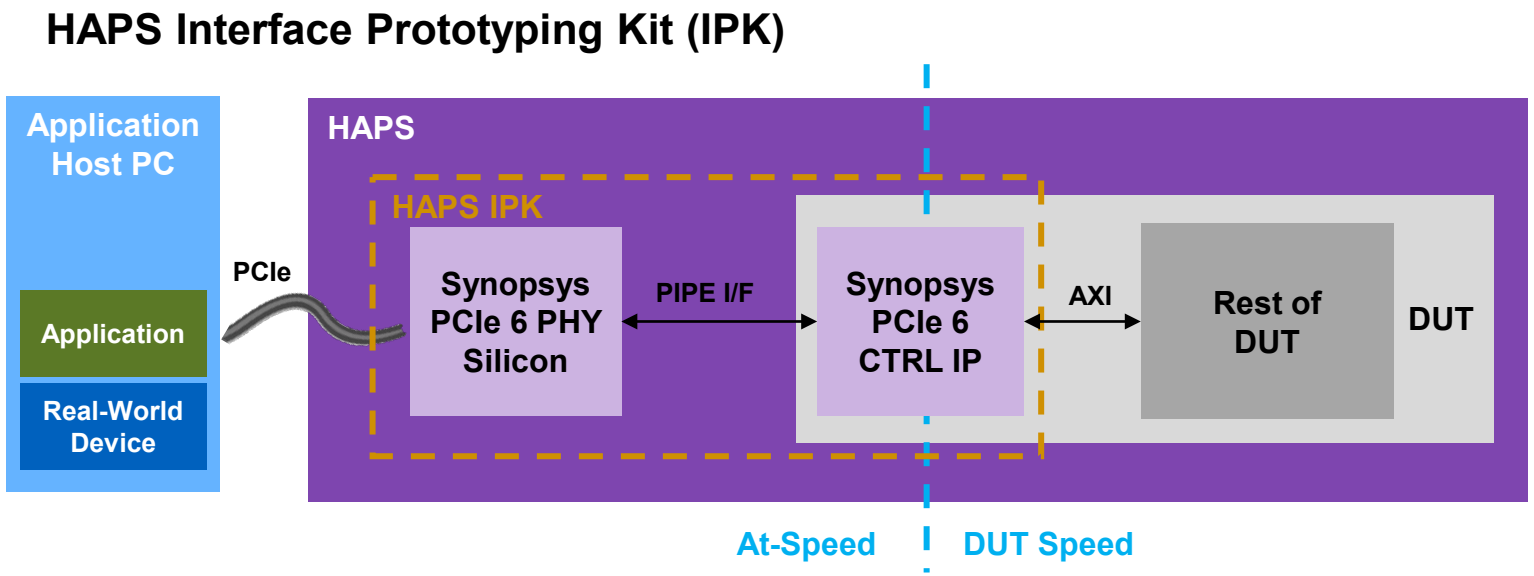
- Synopsys controller IP prototyped out-of-the box
- Synopsys PHY IP card plugged into prototyping system
- Proven compliance setup

Value

- Risc reduction silicon interface compliance
- Driver development platform
- SW development including real-world interface

Validating Interface Compliance At Speed

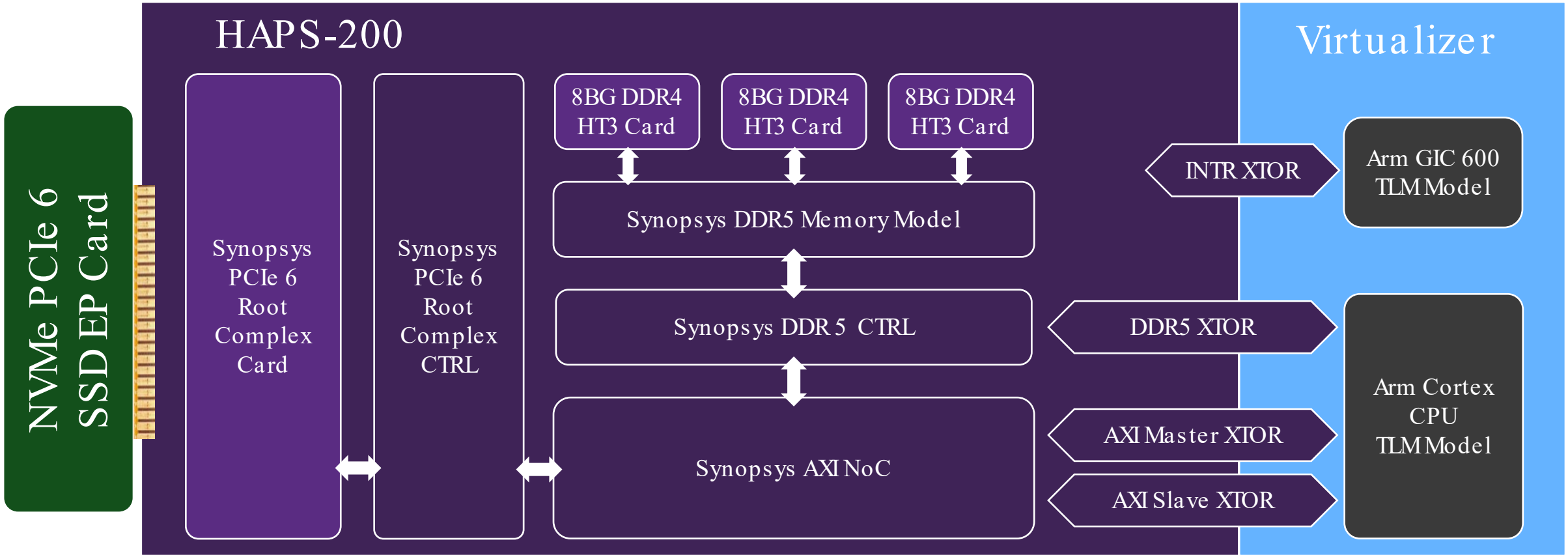
HAPS Interface Prototyping Kit provides out-of-box Synopsys IP (Controller and PHY) Prototype



- IPK running at speed
- Synopsys CTRL IP Prototyping Reference design
- Synopsys IP PHY Silicon
- Speed rate adaptation in the SNPS PCIe CTRL

NVMe Storage Design on HAPS-200

Transactors, Memory Model, IPK Interface Solutions together with Real World NVMe Card



“It’s the Protocol Stupid”

You need:

10 out of 10

Interface Solutions

IP | Virtual Model | VIP | HAV Protocol Solution

- PCIe IPKs for Certification using HAPS
- PCIe Speed Adapters for SW Bring-up with Real-HW
- PCIe ZeBu PHY Models for Post-silicon SW Bring-up at Pre-silicon
- PCIe Virtual System Adaptors for Early SW Bring-up
- PCIe XTORs for Performance acceleration using VCS and ZeBu
- PCIe SoC Verification Kit for IP-VIP bring-up in SoC DUT
- PCIe Test Groups Pre-built UVM tests for field of use
- PCIe Verification IP for Early RTL Verification
- PCIe Virtual Model (VDK) for Early Software Development
- PCIe IP Solution (Controller + PHY)

THANK YOU!

Visit Synopsys at the show floor