Types of Robustness Test According to DO-254 Guideline for Avionic Systems

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What is DO-254?

• RTCA DO-254 is a safety-critical guideline for aircraft electronic hardware, which consists of five Design Assurance Levels (DAL) to make flights as safe as possible and to prevent time and financial losses.
  • DAL A (Catastrophic)
  • DAL B (Hazardous)
  • DAL C (Major)
  • DAL D (Minor)
  • DAL E (No safety effects)
Robustness Tests

• Robustness testing has two main goals:
  • Guarantee that the product functions properly in normal conditions.
  • Tests and identifies the hardware design limitations that are outside of the requirements to ensure how the system reacts to abnormal conditions.
Robustness Test Types

• Invalid Access Error Tests
• Clock Robustness Tests
• Reset Robustness Tests
• Glitch Filter Tests (Data Disruption Tests)
• Invalid State Transition Robustness Tests
Invalid Access Error Tests

• Receiving incorrect combinations of inputs
• Toggling inputs that are not listed in the associated requirement
• Unexpected combinations of inputs
Invalid Access Error Tests

- Start invalid access test
- Send read request to write only register via interface
- Send write request to read only register via interface
- Is invalid access error occurred?
  - YES: Test passes
  - NO: Test fails
Clock Robustness Tests

• Variation of the system clock duty cycle and/or frequency between given tolerances and beyond the tolerances
• Invalid input timing (e.g., setup and hold violations)
• Asserting and de-asserting input signals between clock edges given to systems
Clock Robustness Tests

Start clock robustness test

Is data transfer/FPGA configuration correct?

NO

Observe how robust the design for clock changes.

YES

Increase/Decrease clock frequency/duty cycle.

Finish clock robustness test
Reset Robustness Tests

- Application of reset input to the FPGA while the system is working under normal conditions.
Reset Robustness Tests

1. Start reset robustness test
2. Send random write data to register/port via interface
3. Apply reset to the system
4. Is register return reset value?
   - YES: Test passes
   - NO: Test fails

YES

Test passes

NO

Test fails
Glitch Filter Tests (Data Disruption Tests)

- Data ports are driven to disrupt the data transfer temporarily, while data transfers are continuing for different interfaces.

![Filtered glitch](image1.png)

![Unfiltered glitch](image2.png)
Invalid State Transition Robustness Tests

• The system would be forced to enter an unwanted state rather than the states mentioned in design blocks.
Questions?