

MUNICH, GERMANY DECEMBER 6 - 7, 2022

Reusable Verification Environment for a RISC-V Vector Accelerator

R. Ignacio Genovese, Josue Quiroga, Ivan Diaz, Henrique Yano, Asif Ali, Nehir Sonmez, Oscar Palomar, Victor Jimenez, Mario Rodriguez, Marc Dominguez.







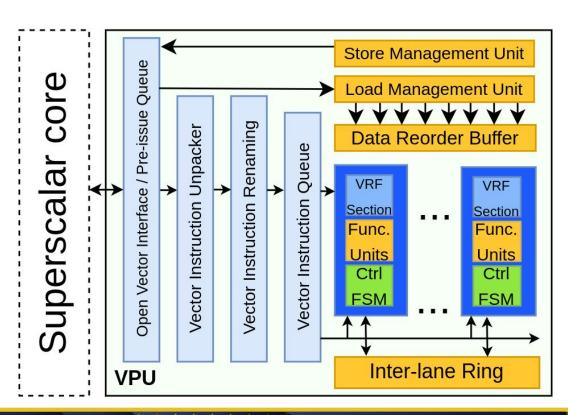
- Free and open Instruction Set Architecture
- Growing rapidly, open collaboration
- HPC, automotive, transportation, cloud, communications, consumer, IoT, etc.
- Modular ISA
 - Vector extension





Vector Processing Unit (VPU)

- DUT
- Vector extension 0.7.1
 - Updating to 1.0
- Different "flavors"
 - EPI*
 - eProcessor*

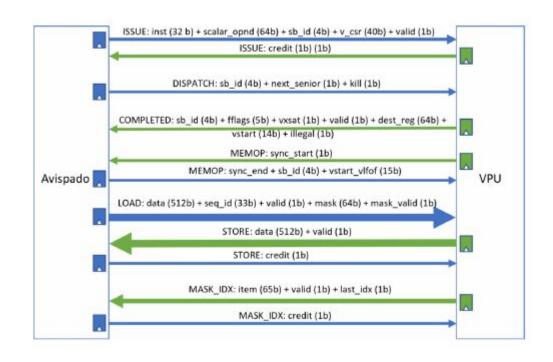








- Core (Avispado) developed by partner (Semidynamics)
- Communicates with the VPU through OVI
- Vector memory accesses are performed by the core

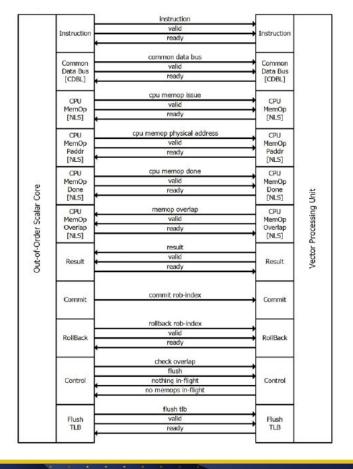








- Different interface for communicating with the core
- VPU access memory directly through AMBA5 CHI interface
- Interface needs signals to solve memory aliasing issues

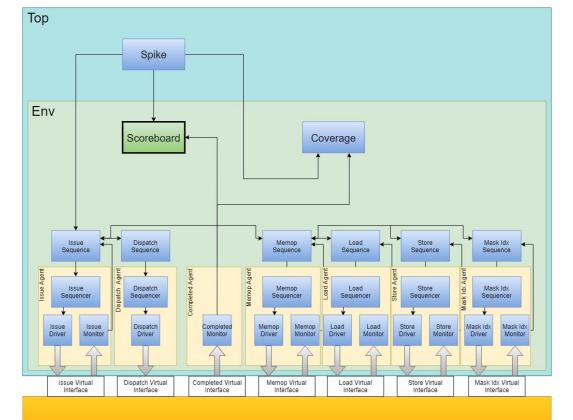






Previous environment

- One agent per each OVI channel
 - Massive interprocess communication
- Difficult to maintain, adapt and evolve



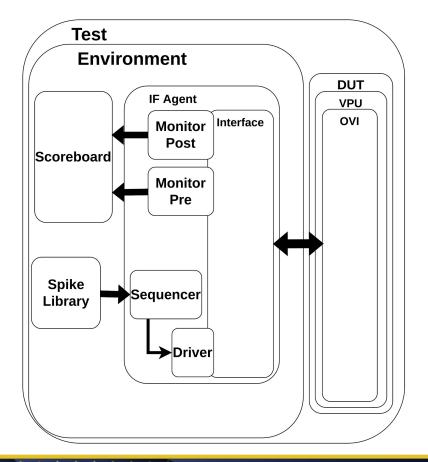
VPU





New UVM environment

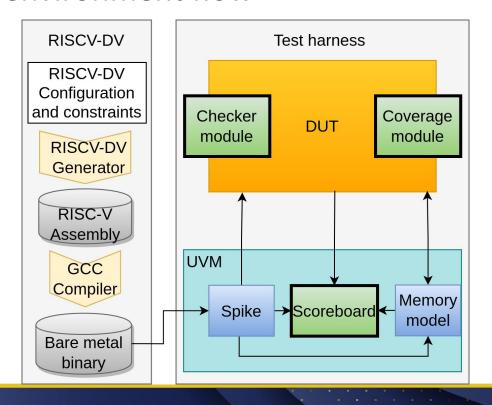
- Common to all projects using the VPU
- Base interface-agnostic verification environment with common components (vpu-dv)
 - Test generation
 - Reference model usage
 - UVCs
 - Interface abstract class
 - Continuous integration
 - Coverage collection and reporting
- Project-specific environment
 - Interface implementation
 - Modified reference model library
 - Specific configurations







Verification environment flow







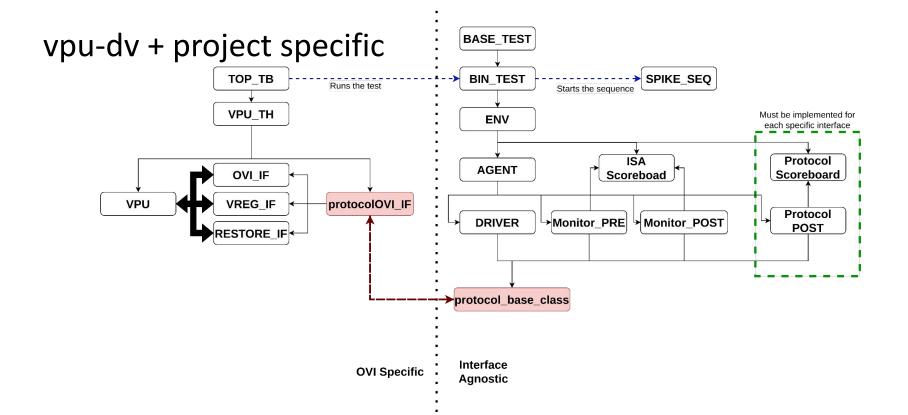
vpu-dv

- Interface base abstract class
 - With methods called by UVCs
 - Implemented in specific project environment

```
pure virtual task do_protocol(); //Runs the specific protocol of the interface to stimulate the DUT
pure virtual task wait_for_clk(int unsigned num_cycles = 1); //Waits for as many num_cycles cycles of the interface clock
pure virtual function drive (ins_tx req); //Pushes the instruction inside the transaction into the pending instructions queue
pure virtual function bit new_ins_tx(); //Returns whether or not there are new instructions received from the driver
pure virtual function iss_state_t monitor_pre(); //Returns the first pending instruction received from the driver
pure virtual function bit new_dut_tx(); //Returns whether or not there are new completed instructions
pure virtual function dut_state_t monitor_post(); //Returns the first pending completed instructions
pure virtual function bit new_protocol_tx(); //Returns whether or not there are new completed instructions
pure virtual function protocol_instr_t monitor_protocol(); //Returns the first pending completed instruction
protocol_instr_t monitor_protocol(); //Returns the first inflight instruction
```











vpu-dv

- Reference model
 - Wrapper abstract class

 - Declares methods to be implemented by ISS.
 Wrapper class overridden in build phase of uvm_test:

 set_type_override_by_type(env_pkg::env::get_type());
 e(), eprocessor_env::get_type());
 - Derived class
 - Implements methods
- Spike
 - C++ implemented
 - Communication done using DPI.
 - Specific versions for each project, with different configurations





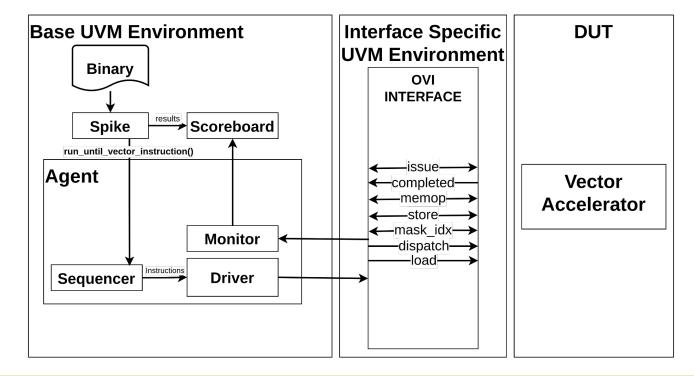
vpu-dv

- Test generation
 - tests repository as submodule
 - ISA tests with different configurations
 - Branch of submodule specified by project environment
 - RISCV-DV random binary generator
 - Modified according to our needs and for different projects.
 - Executed as first step in CI pipelines flow





epac-vpu-dv







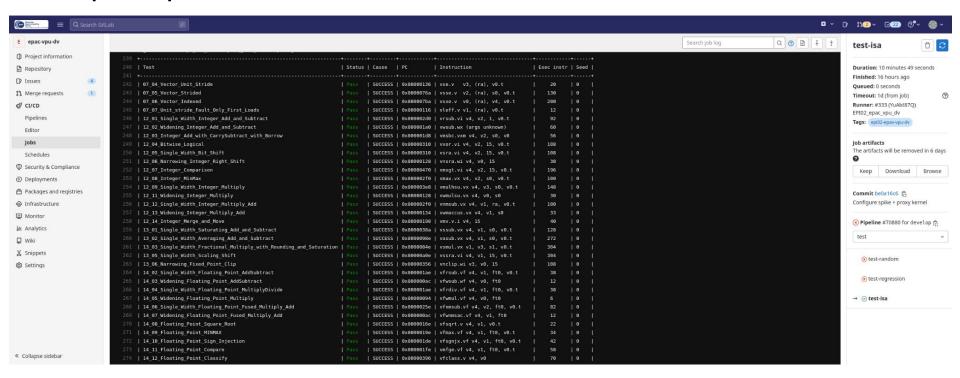
epac-vpu-dv

```
vpu-dv
                                                                     (develop)
                                                                                           :: (a209c5cf)
                                                                    (develop)
   epac-vpu-dv
                                                                                           :: (0f0ef84e)
            Vector_Accelerator
                                                                  :: (develop)
                                                                                           :: (28b841a7)
               src
                    modules
                    └─ vector_lane
                          — functional_unit
                                fpu-encrypted
                                                                  :: (c8db523)
                                                                                           :: (c8db523a)
                                                                                              (86a8f136)
   tests
```





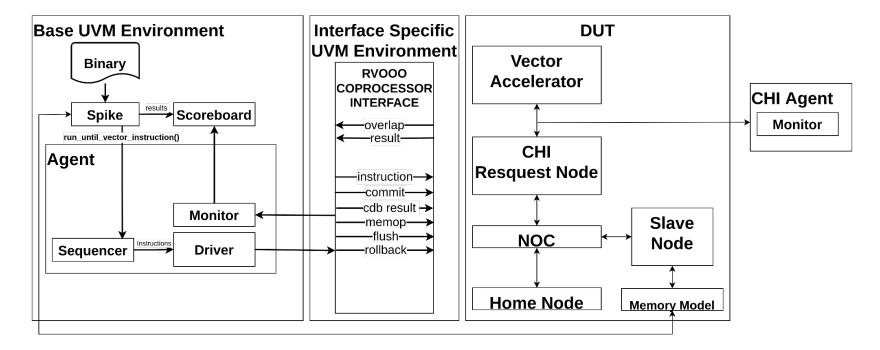
epac-vpu-dv







eprocessor-vpu-dv







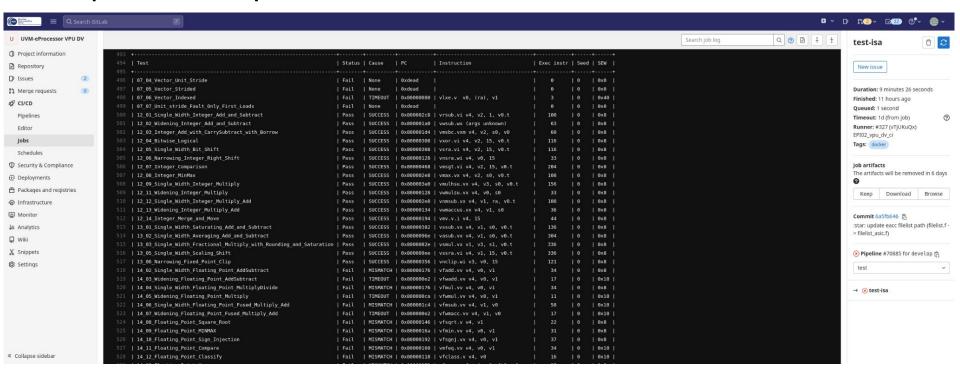
eprocessor-vpu-dv

```
vpu-dv
                                                                  :: (develop)
                                                                                            :: (a209c5cf)
                                                                     (develop)
   eprocessor-vpu-dv
                                                                                            :: (473c2506)
      - rtl
            eAccelerator
                                                                  :: (develop)
                                                                                            :: (06d011bc)
                docs
                  specs
                                                                     (d088cc5)
                                                                                            :: (d088cc5f)
                SIC
                    package
                     riscv_pkg
                                                                                               (b2a90d84)
            epi_nocsim
                                                                  :: (dev)
                                                                                            :: (b34c3283)
                modules
                    ep-fake-snf
                                                                                              (57dea70a)
                                                                                            :: (15e118a2)
                    ep-rni
                    12hn
                                                                                              (7f07a642)
                    noc_ep0
                                                                                            :: (29897d7a)
                    ProNoC
                                                                                              (7d728b19)
                    vpu_chi_interface
                                                                                              (e0ecafe1)
    tests
                                                                                            :: (86a8f136)
```





eprocessor-vpu-dv







Conclusions

- Developed a verification infrastructure reusable for many projects
 - Currently for EPI SGA1 and eProcessor
 - In development for EPI SGA2 (RVV 1.0)
- Easy to extend and maintain
- Ability to uncover more bugs





Acknowledgments

*This research has received funding from the European High Performance Computing Joint Undertaking (JU) under Framework Partnership Agreement No 800928 (European Processor Initiative) and Specific Grant Agreement No 101036168 (EPI SGA2) and No 956702 (eProcessor).

The JU receives support from the European Union's Horizon 2020 research and innovation programme and from Croatia, France, Germany, Greece, Italy, Netherlands, Portugal, Spain, Sweden, and Switzerland.

The EPI-SGA2 project, PCI2022-132935_N1618737 is also co-funded by MCIN/AEI /10.13039/501100011033 and by the UE NextGeneration EU/PRTR.

Proyecto PCI2022-132935 financiado por:















Questions?

