2022 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

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# Using Open-Source EDA Tools in an Industrial Design Flow

Daniela Sánchez Lopera, Prajwal Kashyap,
Nicolas Gerlin, Sven Wenzek, Wolfgang Ecker



accellera SYSTEMS INITIATIVE

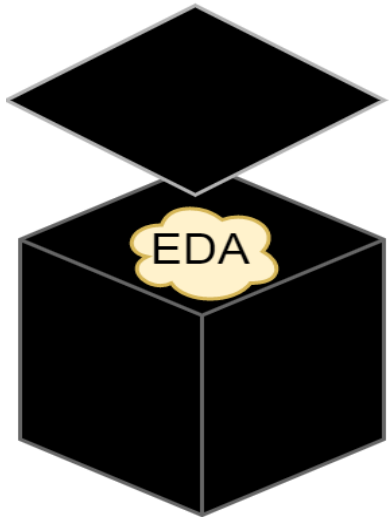
# Outline

- Motivation
- Background – Digital design flow
- What is OpenROAD?
- Our design flow
- Use Cases
- Results
- Summary & Conclusion

# Motivation: Open-Source Software for EDA?

**Advantages:**

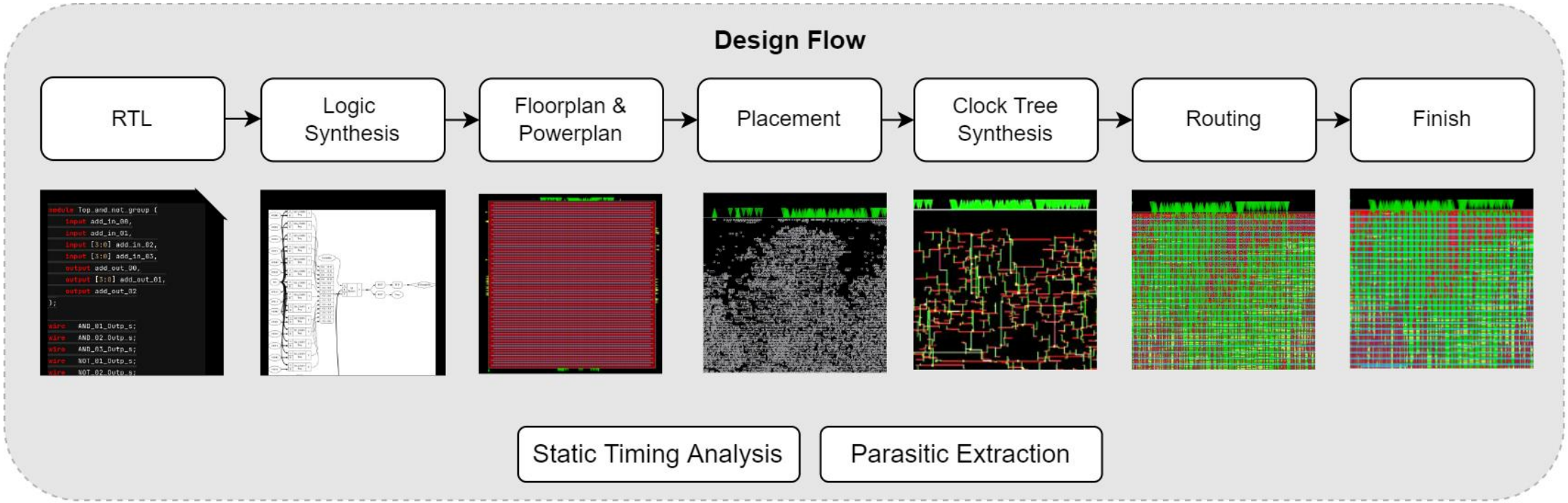
- Extensibility
- Accessibility
- Scalability




For **industries** even more:

- Playground for:
  - Students, researchers & inhouse trainings
- Suitable for:
  - Experiments
  - Collecting huge amount of data
  - Analysing design and flow
- Enabling:
  - Machine Learning (ML) applications
  - Innovation

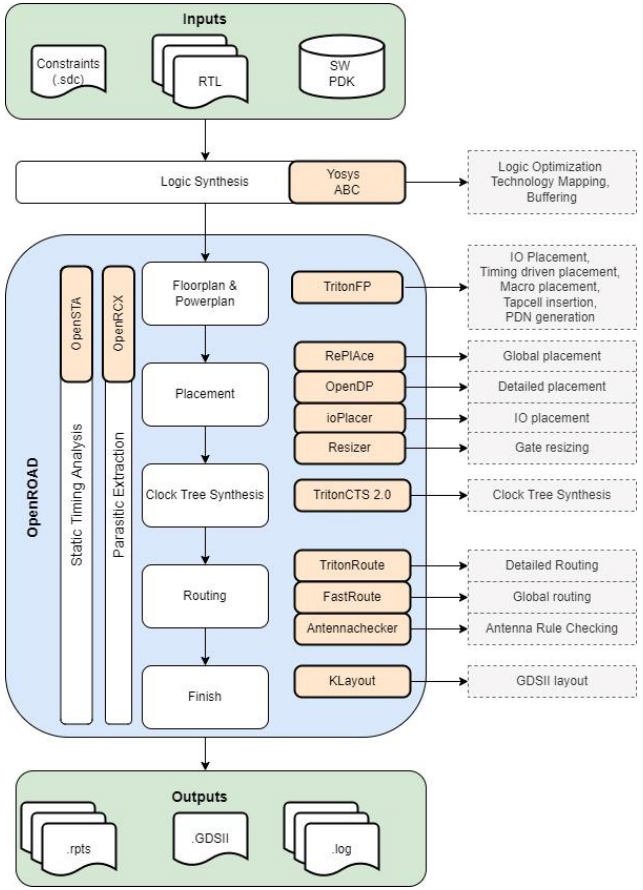
# Background
# Digital Design Flow




Images generated by OpenROAD using random die configuration and open-source PDK

# What is OpenROAD?

- RTL-to-GDSII framework for design exploration and physical design implementation
- Three existing ”flow controllers”
  - OpenROAD-flow-scripts[1]
  - OpenLANE[2]
  - Robust Design Flow (RDF)-2021[3]




[1] https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts
[2] https://github.com/The-OpenROAD-Project/OpenLane
[3] https://github.com/ieee-ceda-datc/datc-rdf

# What is OpenROAD?
## Related work

**ML applications optimizing tool configurations:**

- LSOracle[4]
- OpenABC-D[5]
- VeriGOOD-ML[6]

**ML applications learning from OpenROAD outcomes:**

- Congestion[7]
- Arrival times and slack[8]

[4] Neto, Walter, et al. "LSOracle: A logic synthesis framework driven by artificial intelligence", *ICCAD 2019*.
[5] Chowdhury, Animesh Basak, et al. "OpenABC-D: A Large-Scale Dataset For Machine Learning Guided Integrated Circuit Synthesis", *arXiv preprint:2110.11292* (2021).
[6] Esmaeilzadeh, Hadi, et al. "VeriGOOD-ML: An Open-Source Flow for Automated ML Hardware Synthesis", *ICCAD 2021*.
[7] Ghose, Amur, et al. "Generalizable Cross-Graph Embedding for GNN-based Congestion Prediction", *ICCAD 2021*
[8] Guo, Zizheng, et al. "A Timing Engine Inspired Graph Neural Network Model for Pre-Routing Slack Prediction", DAC 2022.

# What is OpenROAD?

## Challenges

Lück, C., Sánchez Lopera, D., Wenzek, S., & Ecker, W. Industrial Experience with Open-Source EDA Tools. MLCAD 2022

Adaptations on source code to cope with:

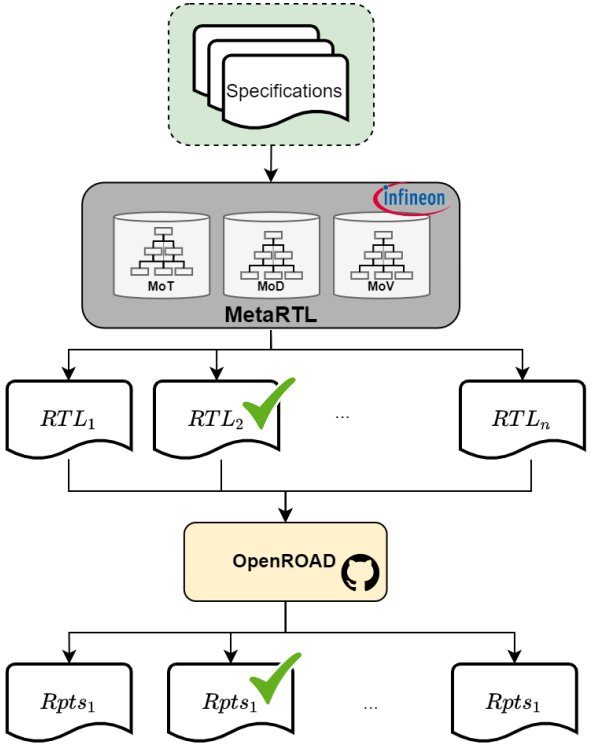
- Infrastructure restrictions: No super user, no Docker
- Proprietary PDKs
- Parallelization on compute farm

# What is OpenROAD?

## Envisioned use-cases

Lück, C., Sánchez Lopera, D., Wenzek, S., & Ecker, W. Industrial Experience with Open-Source EDA Tools. MLCAD 2022

- Design Space Exploration
- Data generation for ML models
  - Design metric prediction




Sánchez Lopera D., Ecker W., Applying GNNs to Timing Estimation at RTL, ICCAD 2022.
**MetaRTL**: Ecker, W., and Schreiner, J.. "Introducing Model-of-Things (MoT) and Model-of-Design (MoD) for simpler and more efficient hardware generators. *VLSI-SoC 2016*.

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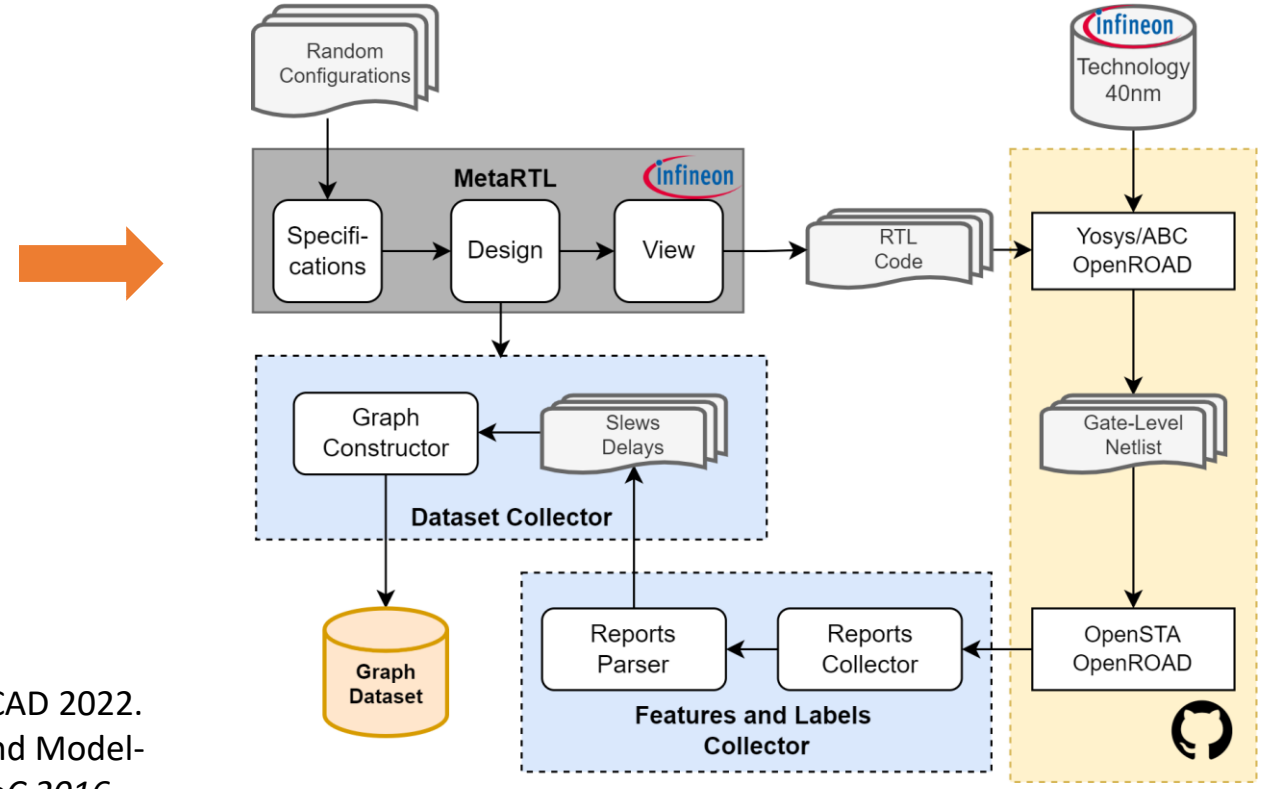


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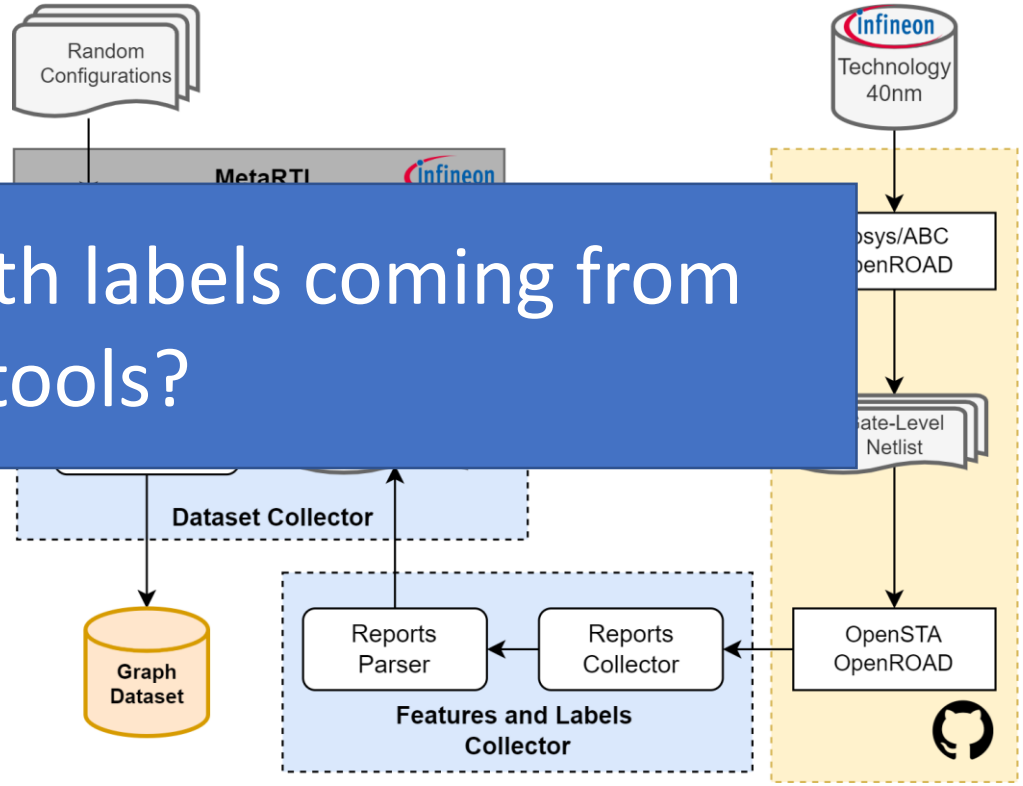
How good are our ground truth labels coming from open-source tools?

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# OpenROAD vs Commercial Tools

| Feature | Open-source | Commercial |
|---|---|---|
| Extensibility | x | |
| Accesibility | x | |
| Scalability | x | |
| Customer Support | | x |
| Reliability | | x |
| Technology & Engineering | | x |
| Workforce development | x | x |

A Mixed Open-Source and Proprietary EDA Commons for Education and Prototyping Invited Paper. Andrew B. Kahng. ICCAD 2022

# OpenROAD vs Commercial Tools

| Feature | Open-source | Commercial |
|---|---|---|
| Extensibility | x | |
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Open and free software

Years of experience and billions of investments

A Mixed Open-Source and Proprietary EDA Commons for Education and Prototyping Invited Paper. Andrew B. Kahng. ICCAD 2022

# OpenROAD vs Commercial Tools

| Feature | Open-source | Commercial |
|---|---|---|
| Extensibility | x | |
| Accesibility | x | |
| S | | |
| C | | |
| [illegible] | | |
| Technology & Engineering | | x |
| Workforce development | x | x |

Open and free software

Q1: But how do they compare w.r.t PPA results?

[illegible] years of experience and billions of investments

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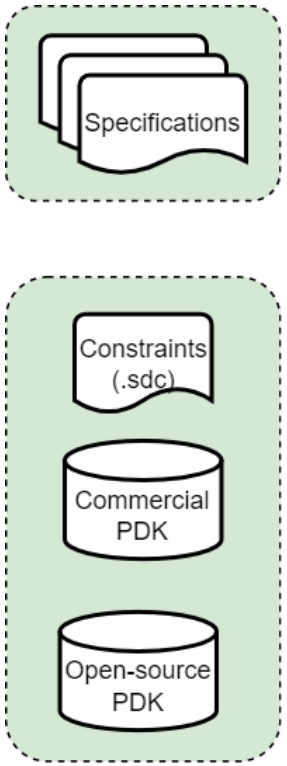
# Our Design Flow (1)

## Inputs



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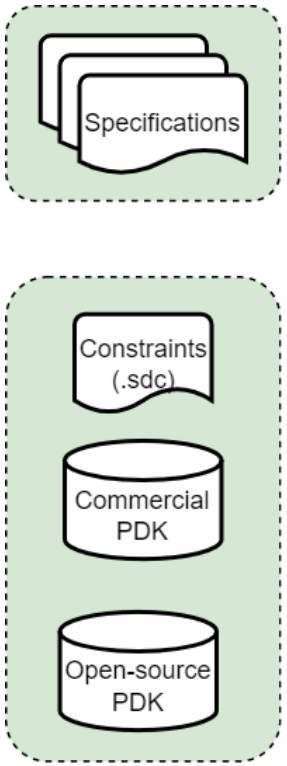
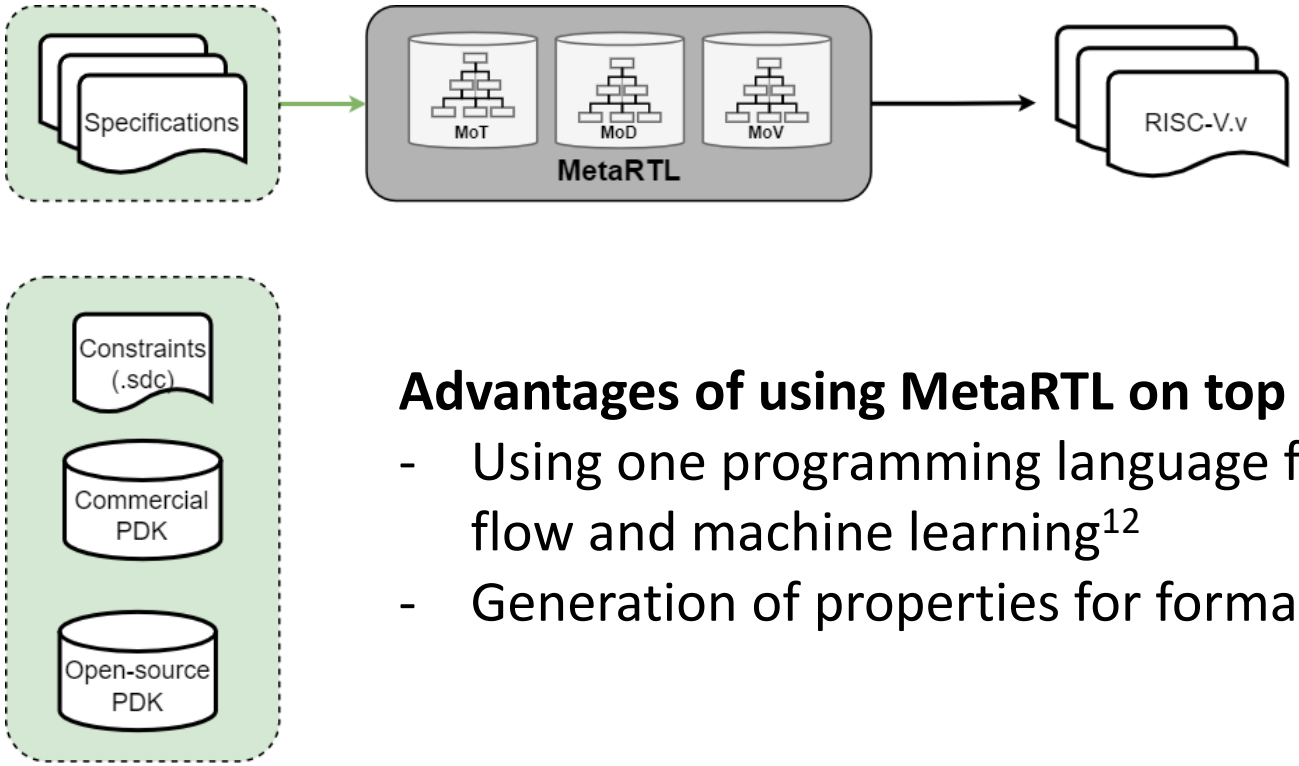



| PDK | Type | # Lines Lib. File | # Standard Cells |
|---|---|---|---|
| 40nm | Proprietary | 14678.9 K | 852 |
| 130nm | Open-source | 333.5 K | 753 |

*Open-source: https://skywater-pdk.readthedocs.io/en/main/

# Our Design Flow (2)

## RTL Generation




**Advantages of using MetaRTL on top of OpenROAD:**

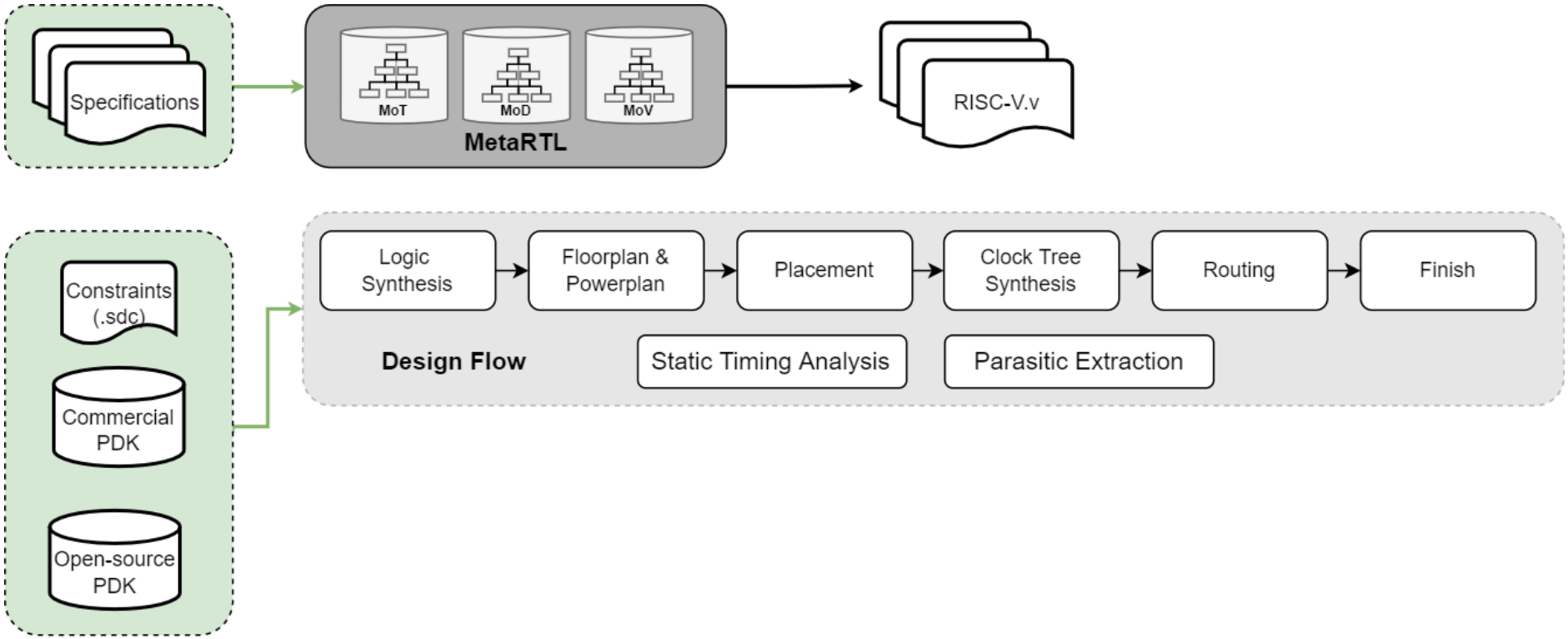
- Using one programming language for hardware generation, synthesis flow and machine learning[12]
- Generation of properties for formal verification[13]

[12] K. Devarajegowda, et al., "Python based framework for HDSLs with an underlying formal semantics". ICCAD 2017

[13] K. Devarajegowda, et al., "How to Keep 4-Eyes Principle in a Design and Property Generation Flow", MBMV 2019

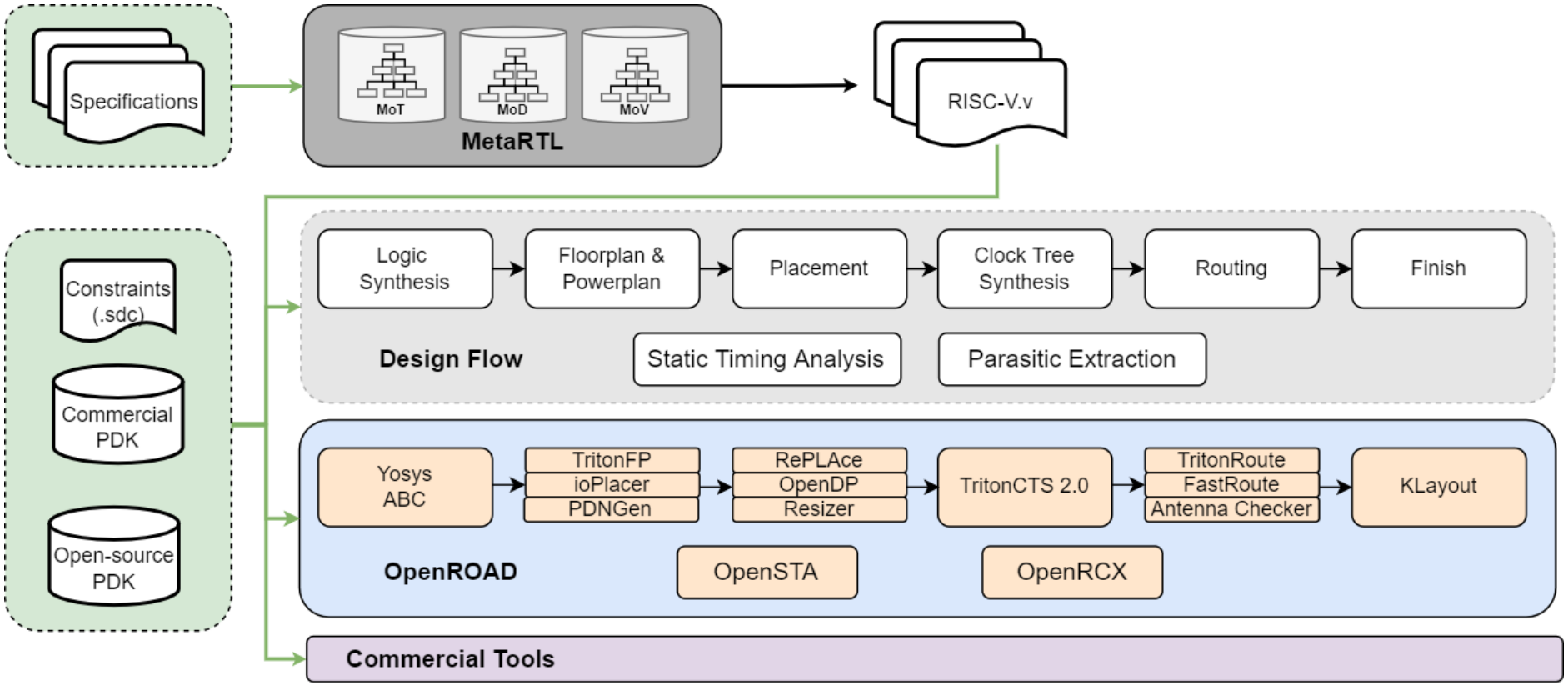
# Our Design Flow (3)

## RTL2GDS Flow



# Our Design Flow (4)

## RTL2GDS Tools



# Generated Use-Cases

## RISC-V - RV32IMCX

| Designs | Extension Units | # Lines of Code | # Components | # Input bits | # Output bits |
|---|---|---|---|---|---|
| **RISC-V[1]** | CRC, PFC | 16496 | 810 | 71 | 157 |
| **RISC-V[2]** | Exception | 28377 | 1430 | 170 | 164 |
| **RISC-V[3]** | MAC | 39487 | 2271 | 171 | 164 |
| **RISC-V[4]** | Event Counters | 16391 | 844 | 70 | 157 |
| **RISC-V[5]** | CRC, PFC, MAC, Event Counters, Exception | 42121 | 2403 | 170 | 165 |

# Generated Use-Cases

## RISC-V

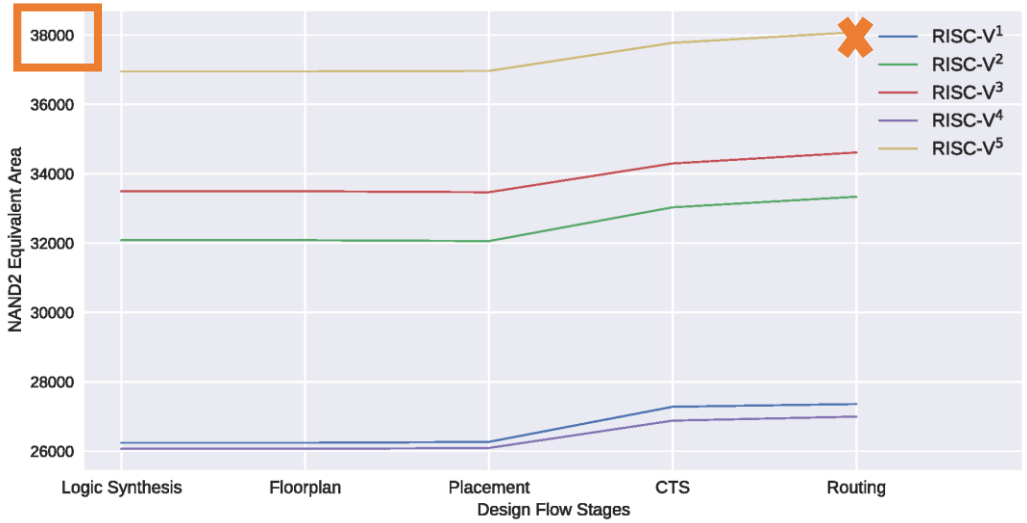
| Designs | Extension Units | # Lines of Code | # Components | # Input bits | # Output bits | Complexity Flag |
|---|---|---|---|---|---|---|
| **RISC-V**[1] | CRC, PFC | 16496 | 810 | 71 | 157 | + |
| **RISC-V**[2] | Exception | 28377 | 1430 | 170 | 164 | ++ |
| **RISC-V**[3] | MAC | 39487 | 2271 | 171 | 164 | ++ |
| **RISC-V**[4] | Event Counters | 16391 | 844 | 70 | 157 | + |
| **RISC-V**[5] | CRC, PFC, MAC, Event Counters, Exception | 42121 | 2403 | 170 | 165 | +++ |

# Post Routing Results

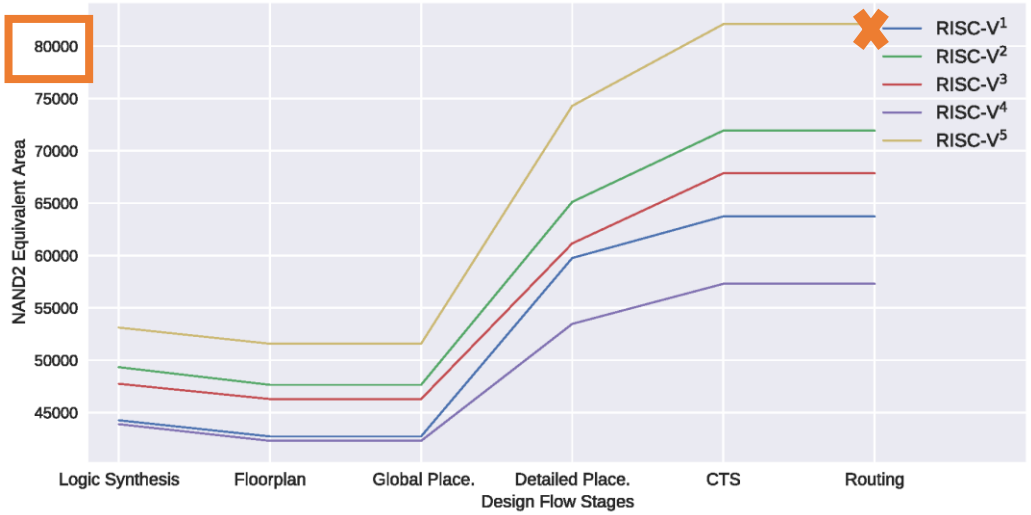
# Results (1)

## **Post Routing** – Area

### Commercial Tool



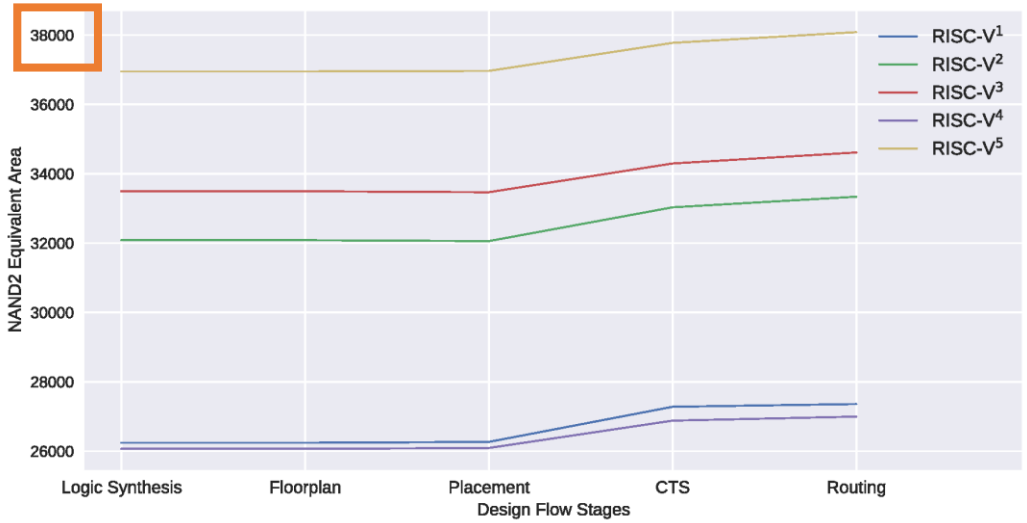

### OpenROAD



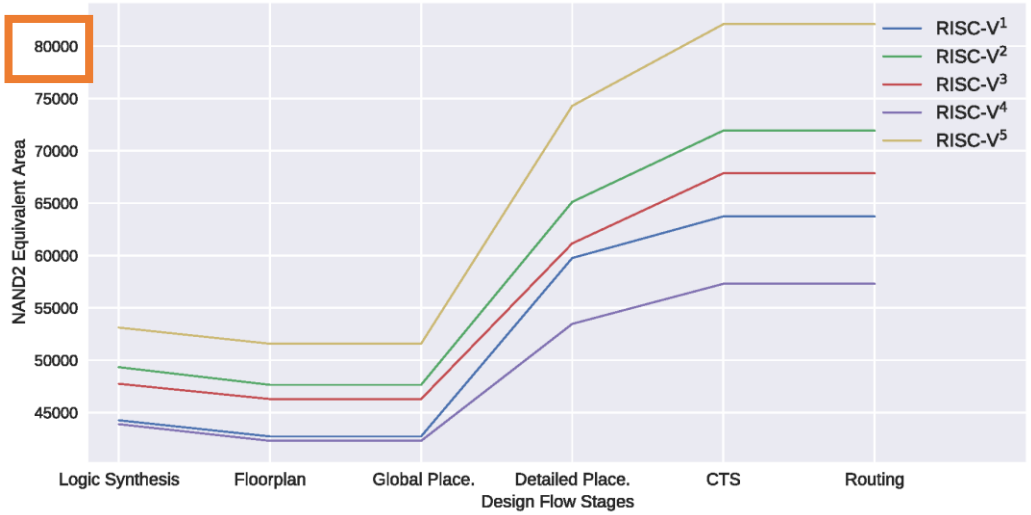

$$Avg.ratio = \frac{1}{5}\sum \frac{Yosys/OpenROAD}{Commercial\ Tool}\ \forall \text{ RISC-V}$$

# Results (1)
## **Post Routing** – Area

### Commercial Tool




### OpenROAD



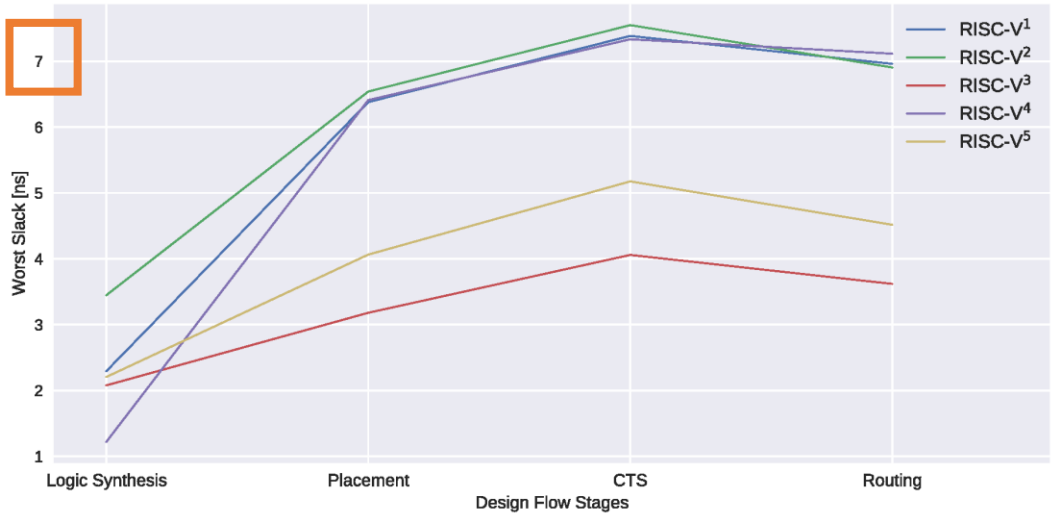

Averaging the results for all 5 RISC-Vs, OpenROAD occupies more area:

- NAND2 Eq. Area: 2.1x more area
- # Standard Cells: 2.4x more cells

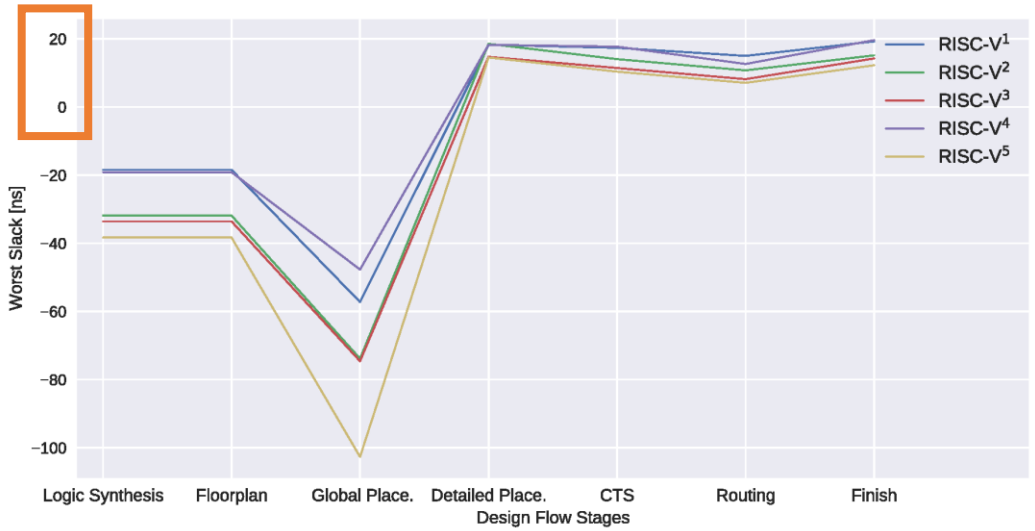
# Results (2)

## **Post Routing** – Worst Slack

### Commercial Tool




### OpenROAD



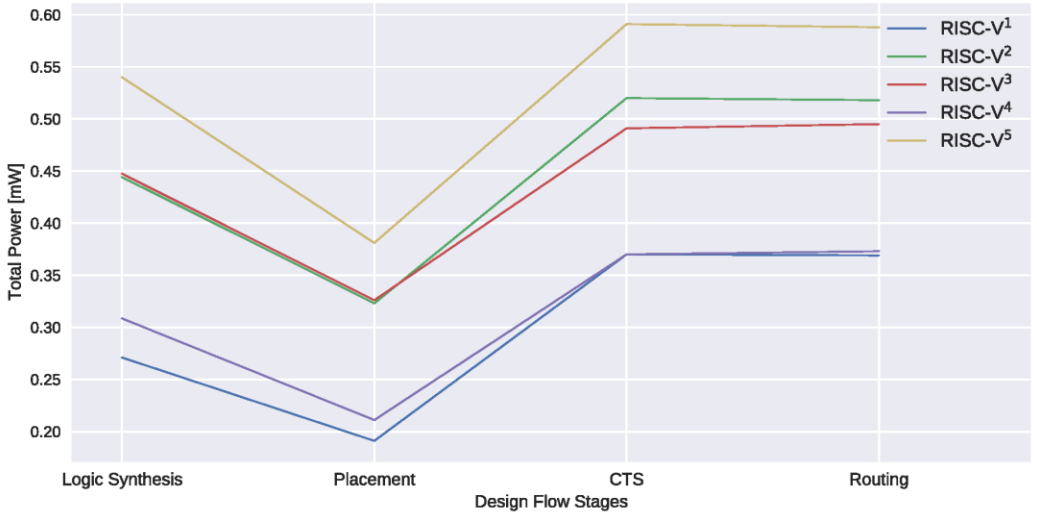

Averaging the results for all 5 RISC-Vs, OpenROAD worst slack after routing is:

- Critical path worst slack:  2.9x higher

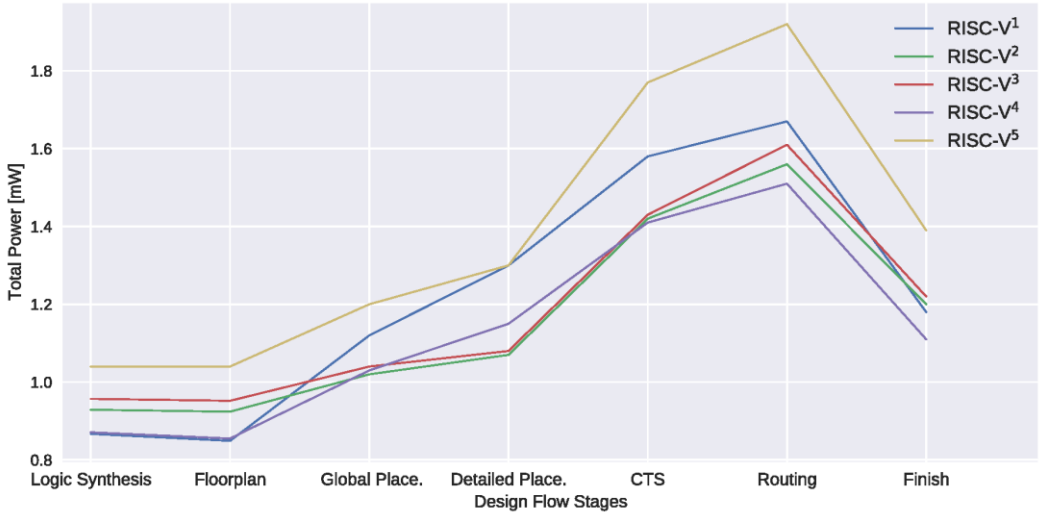
# Results (3)

## **Post Routing** – Total Power

### Commercial Tool




### OpenROAD




Averaging the results for all 5 RISC-Vs, OpenROAD consumes more power:

- Total power: 2.7x more

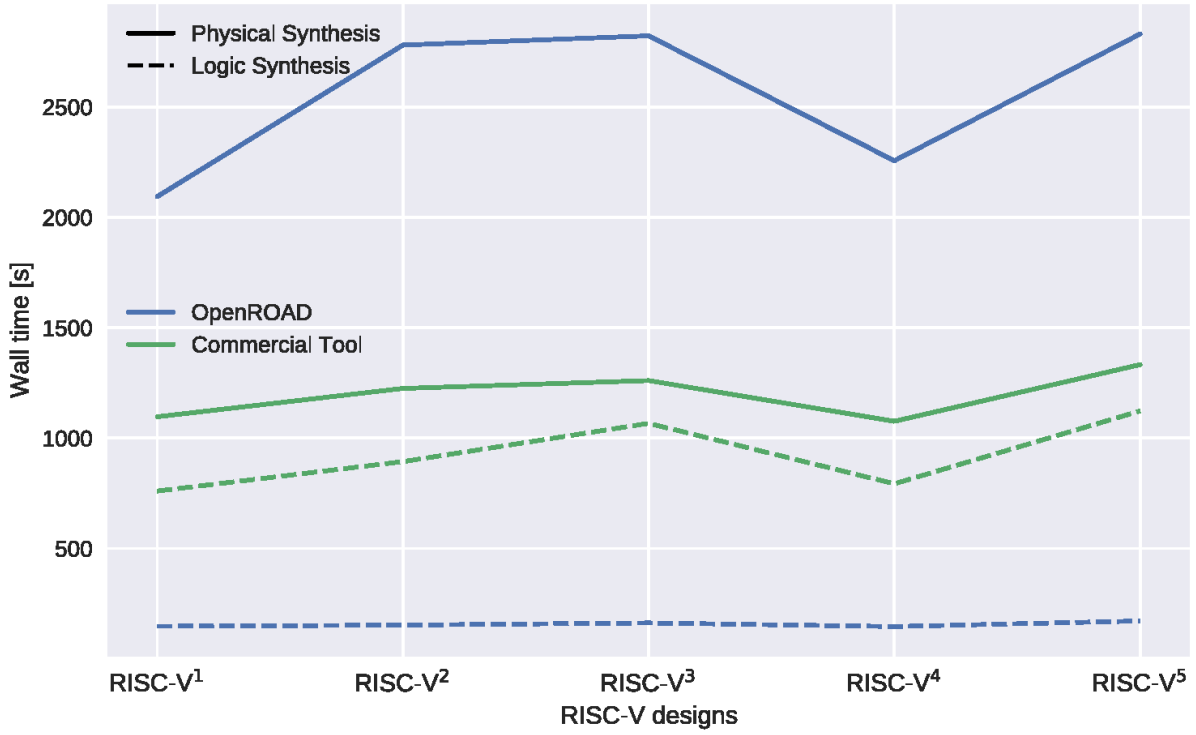
# Runtimes

# Results (4)
## Wall times – Routing

- Under fair conditions:
  - No multi-threading
  - Same CPU:

    Linux CPU Intel® Xeon® Gold 6248R

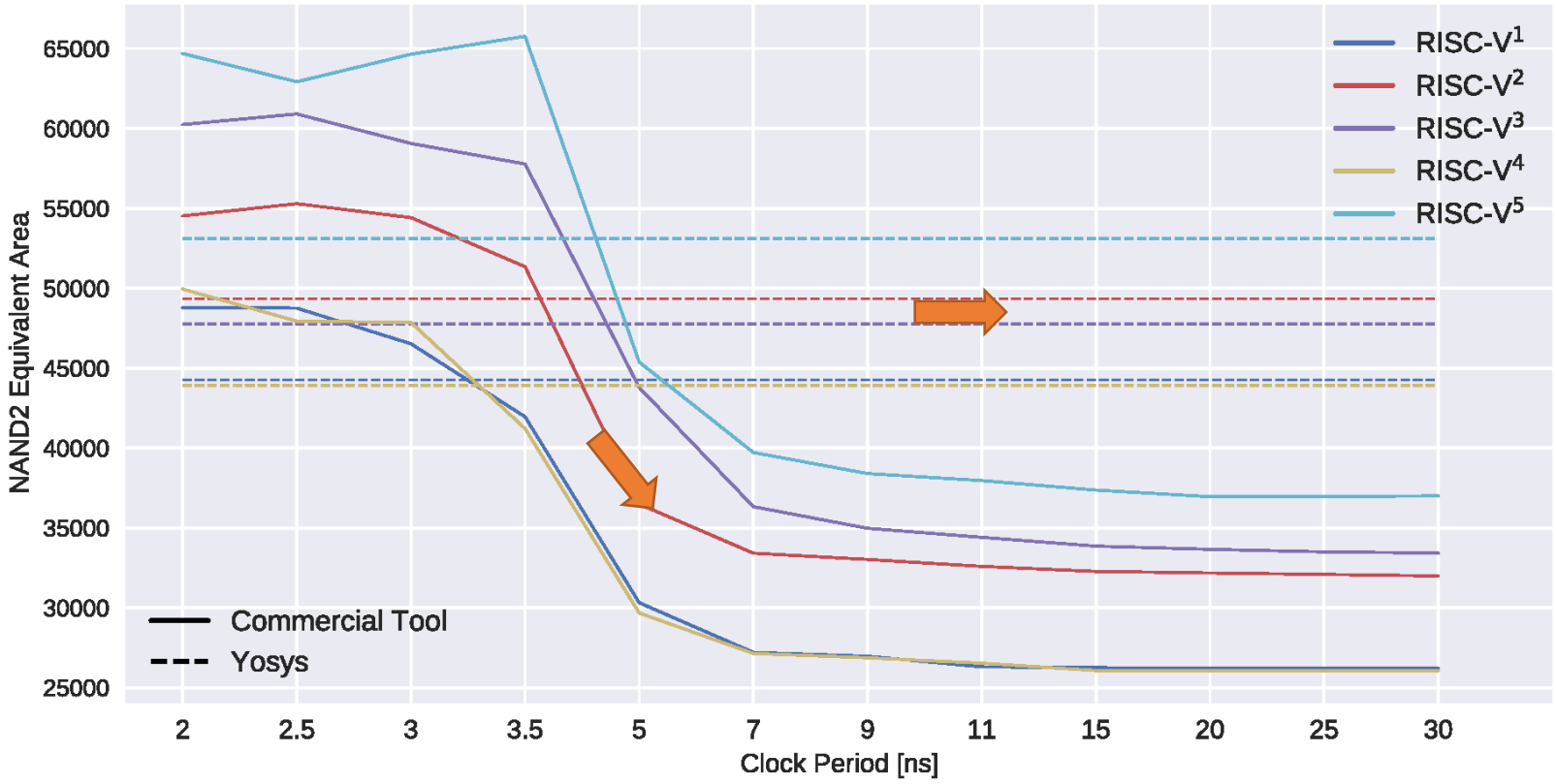
    at 3.00 GHz and 80 GiB system memory



# Sweeping clock

# Results (5)

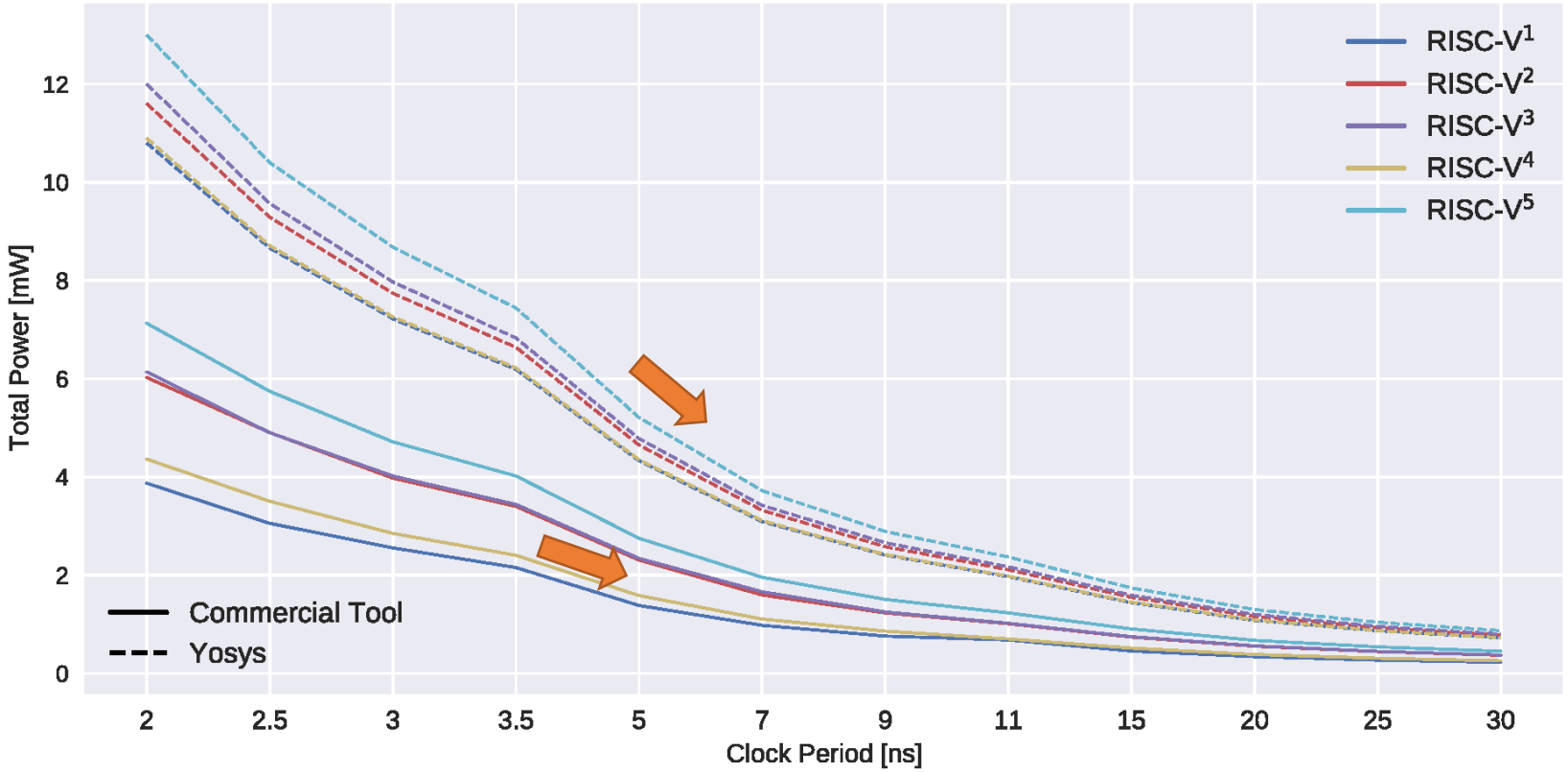
## Sweeping clock - Logic Synthesis - Area




OpenROAD keeps area constant while varying clock period

# Results (6)

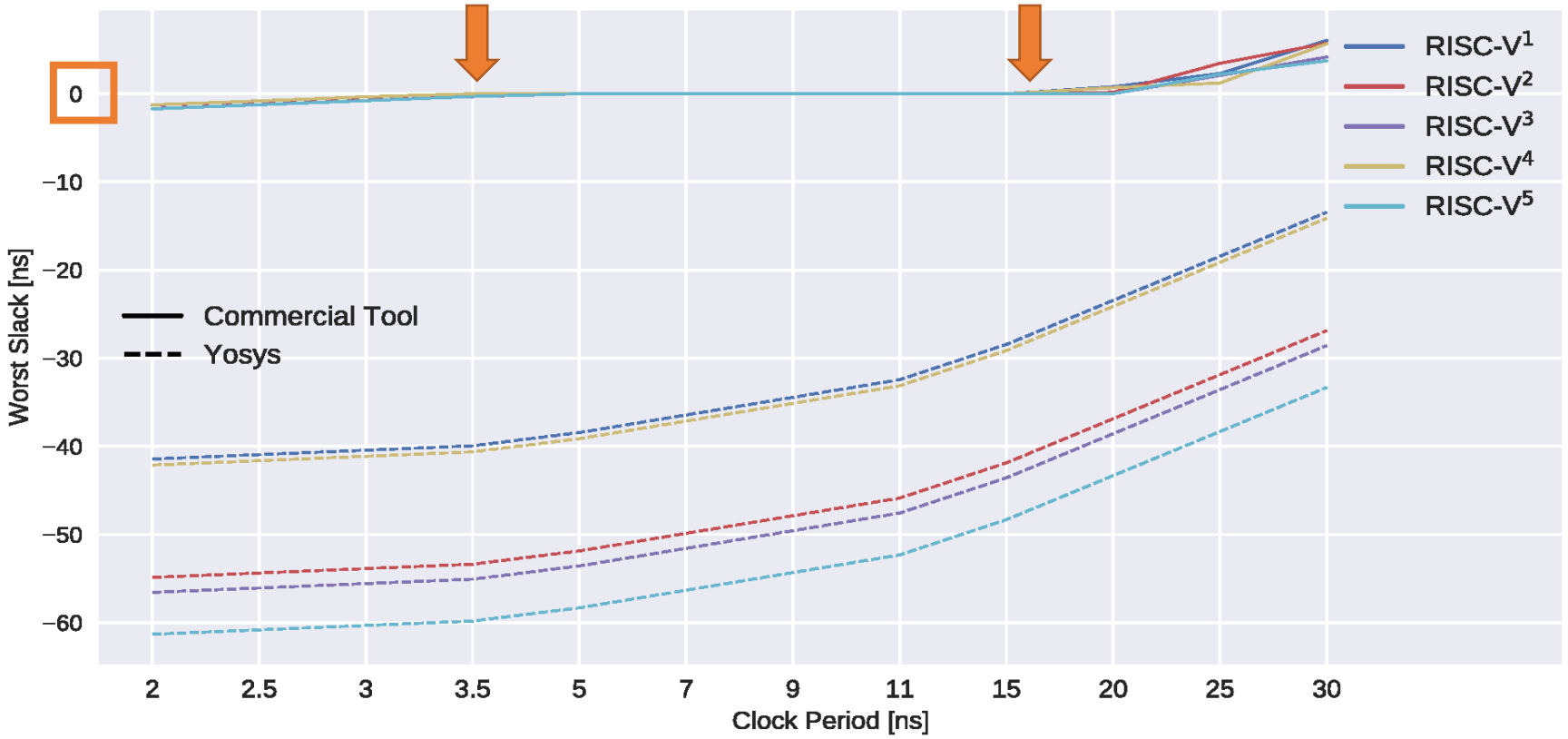
## Sweeping clock - Logic Synthesis - Power




Higher clock, less total power

# Results (7)

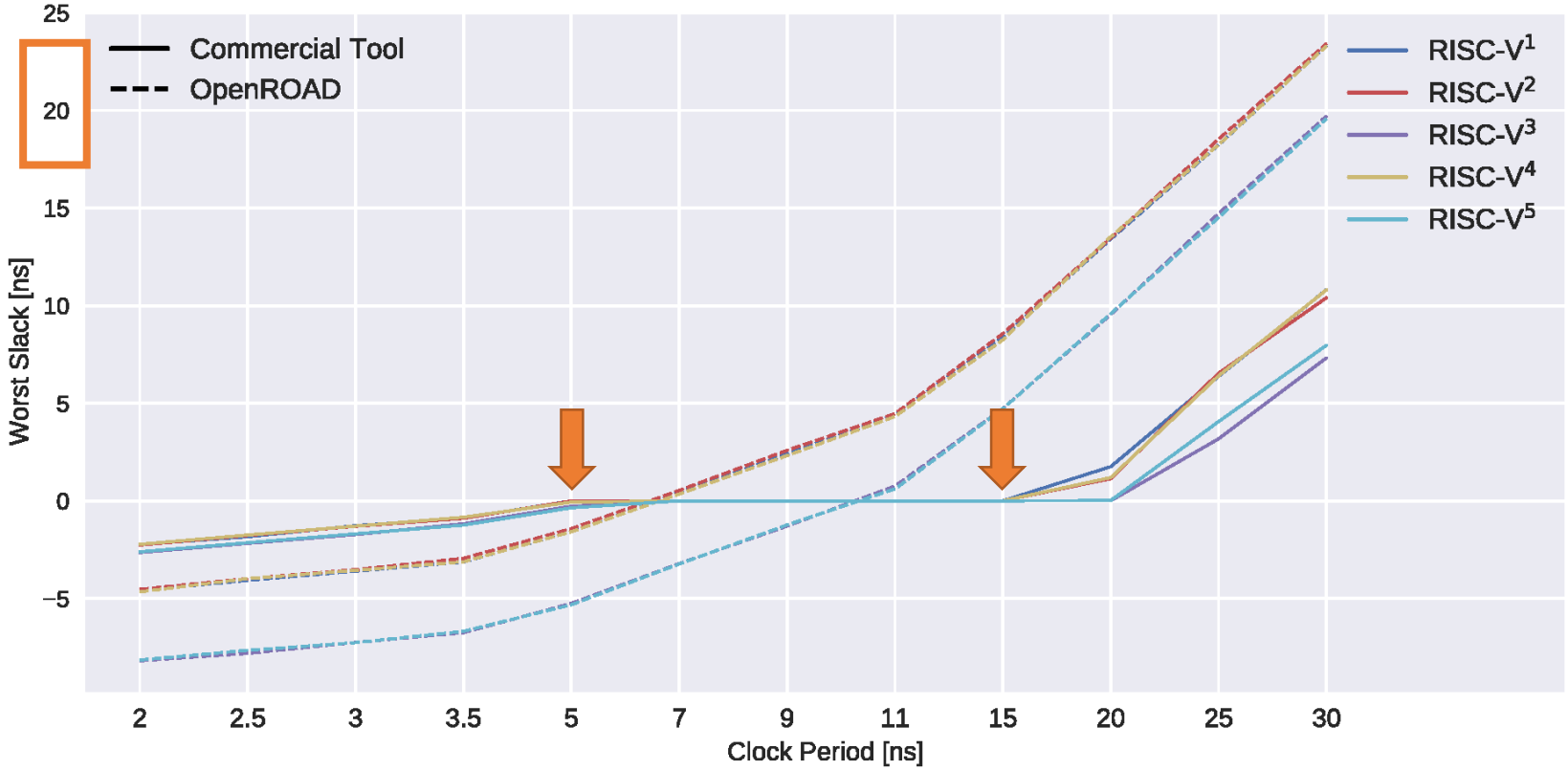
## Sweeping clock - Logic Synthesis - Worst Slack




OpenROAD needs very high clock periods for meeting timing requirements after logic synthesis

# Results (8)

## Sweeping clock – Routing - Worst Slack




OpenROAD needs higher clocks for meeting timing requirements after routing

# Summary

Q1: But how do they compare w.r.t PPA results?

# Summary

| Stage | Ratio [Open-Source Tool/Commercial Tool] | | | |
|---|---|---|---|---|
| | NAND2 Eq. Area | # Standard Cells | WS | Total Power |
| Post logic synthesis | 1.5 | 1.8 | <0 | 2.4 |
| Post routing | 2.1 | 2.4 | 2.9 | 2.7 |

→ **Avg = 2.5x**

* For PDK 40nm
* For flatten synthesis
* For clock 25ns

# Summary

| Stage | Ratio [Open-Source Tool/Commercial Tool] | | | |
|---|---|---|---|---|
| | NAND2 Eq. Area | # Standard Cells | WS | Total Power |
| Pos syn | | | | |
| Pos | | | | |

How good are our ground truth labels coming from open-source tools?

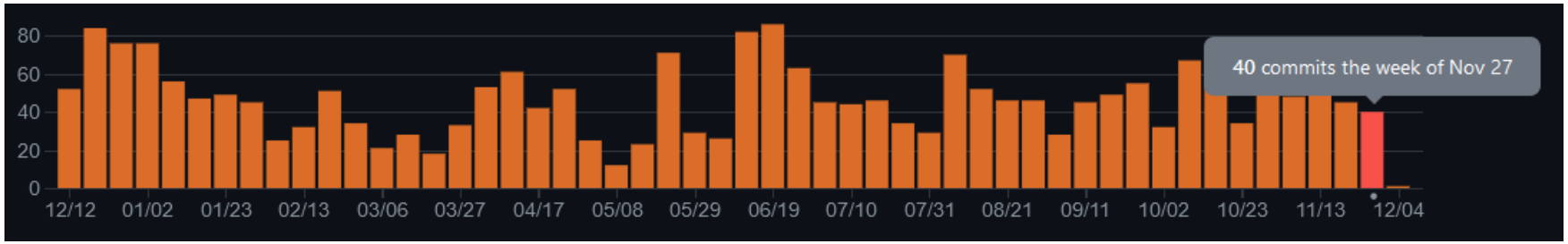
* Fo
* For flatten synthesis
* For clock 25ns

# Conclusion

- We outline our industrial flow **from initial specifications to GDS** using different RISC-Vs as use cases.
- Averaging the reported post-routing PPA factors for a 25 ns clock period, the **commercial tool outperforms OpenROAD by a factor of 2.52x**.
- The **commercial tool is faster** without any parallelization, and it **meets timing constraints for lower clock periods** than OpenROAD.

# Conclusion

**But** OpenROAD is evolving fast: more than 1.4K commits in 2022 and 19 active pull requests[14].




https://github.com/The-OpenROAD-Project/OpenROAD/graphs/commit-activity. Visited on Dec. 05, 2022.

**Future:**

- Commercial and open-source EDA working together to enable research and progress on the field
- Analyze generated output of commercial tools using OpenROAD and vice versa

[14] https://github.com/The-OpenROAD-Project/OpenROAD/graphs/commit-activity. Visited on Sept. 07, 2022

# Questions?

Thank you!

# What is OpenROAD?
## Related work

**OpenROAD published papers describe some attempts of benchmarking:**

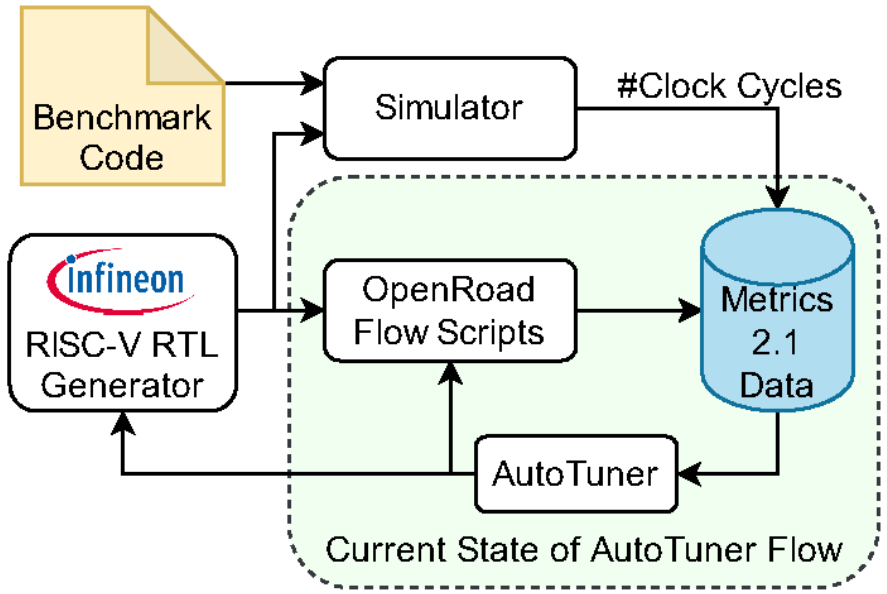
- Number of commits, citations, community engagement[9]
- Comparing results of their AutoTuner with two different SkyWater libraries[10]
- Comparing the OpenROAD placer, OpenSTA and OpenRCX w.r.t commercial tools[11]

[9] Jung, Jinwook, et al. "METRICS2. 1 and Flow Tuning in the IEEE CEDA Robust Design Flow and OpenROAD ICCAD Special Session Paper", ICCAD 2021.
[10] A. B. Kahng, "Looking into the Mirror of Open Source: Invited Paper", *ICCAD 2019*
[11] A. B. Kahng and T. Spyrou, "The OpenROAD Project: Unleashing Hardware Innovation", GOMAC 2021

# What is OpenROAD?

## Envisioned use-cases

- *Design Space Exploration (DSE)*



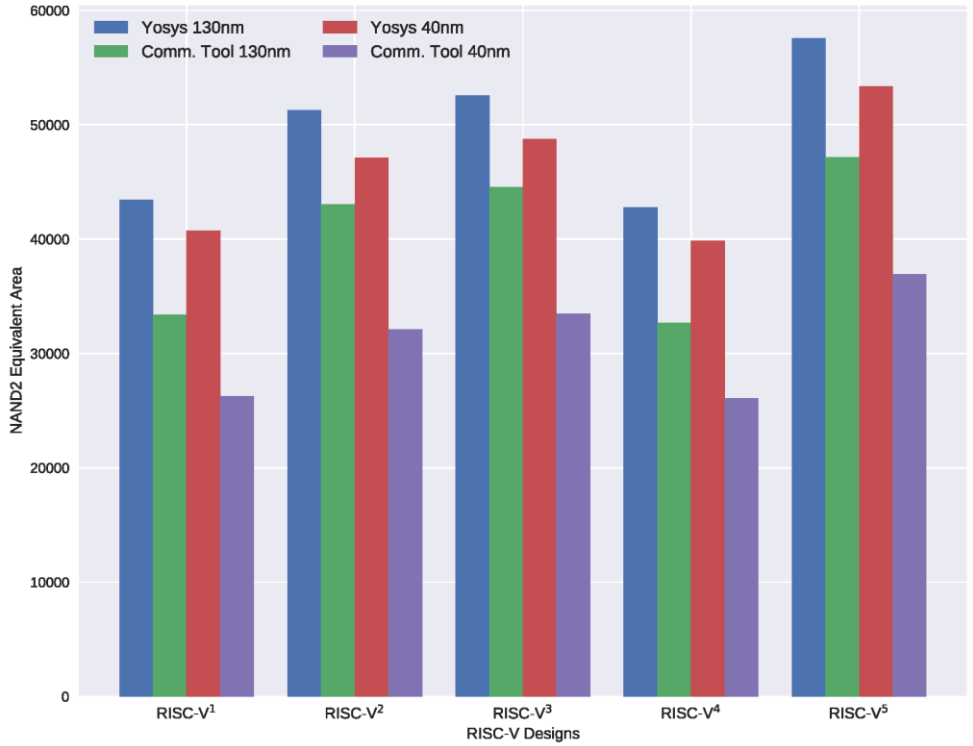

Lück, C., Sánchez Lopera, D., Wenzek, S., & Ecker, W. Industrial Experience with Open-Source EDA Tools. MLCAD 2022

# Post Logic Synthesis Results

# Results (1)

## Post Logic Synthesis – Area

### NAND2 Equivalent Area



# Results (1)

## Post Logic Synthesis – Area

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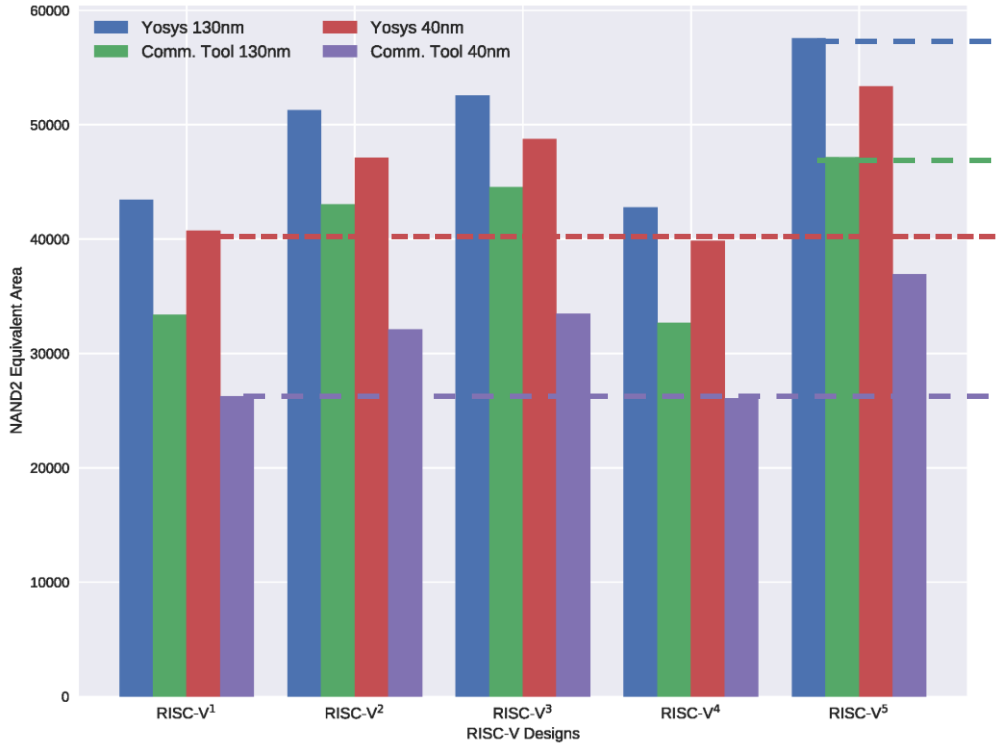



$$ratio = \frac{Yosys/OpenROAD}{Commercial\ Tool} = 1.2$$

$$ratio = \frac{Yosys/OpenROAD}{Commercial\ Tool} = 1.6$$

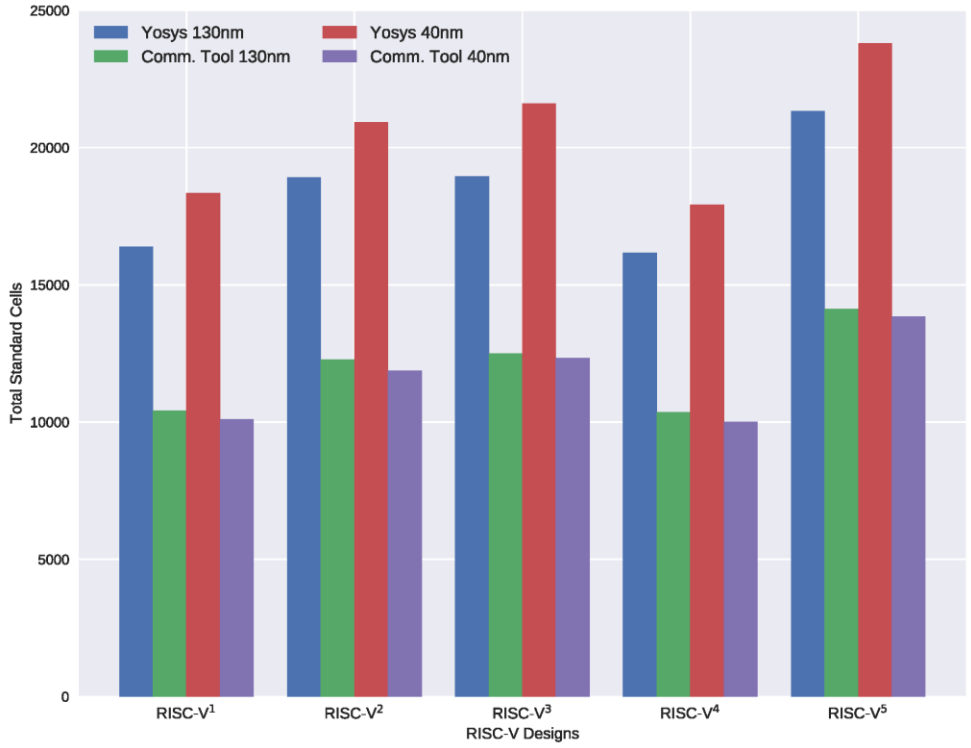
Averaging the results for all 5 RISC-Vs, Yosys/OpenROAD occupies higher area:

- For 130nm: 1.2x more area
- For 40nm: 1.5x more area

# Results (2)

## Post Logic Synthesis – Area

### Total Standard Cells




Averaging the results for all 5 RISC-Vs, Yosys/OpenROAD occupies higher area:

- For 130nm: 1.5x more cells
- For 40nm: 1.8x more cells

# Results (3)

## **Post Logic Synthesis** – Worst Negative Slack (WNS)

**For both PDKs: 130nm and 40nm**

| Synthesis Type | Commercial Tool | OpenROAD |
|---|---|---|
| Flatten | 0 | <0 |
| Non-flatten (hierarchical) | 0 | 0 |

# Results (3)

## **Post Logic Synthesis** – Worst Negative Slack (WNS)

**For both PDKs: 130nm and 40nm**

| Synthesis Type | Commercial Tool | OpenROAD |
|---|---|---|
| Flatten | 0 | <0 |
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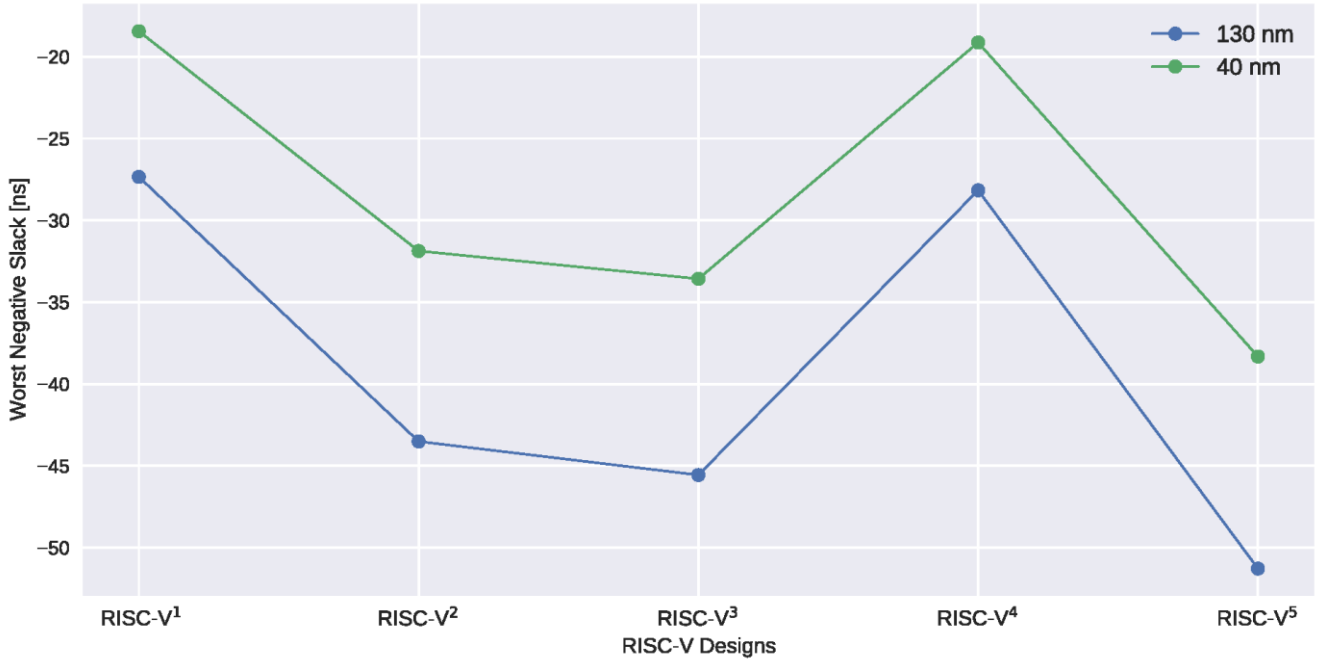
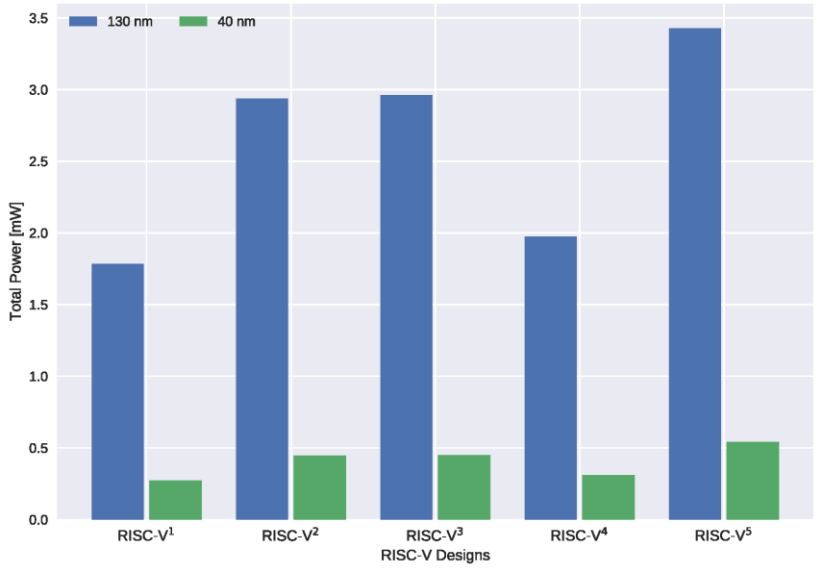


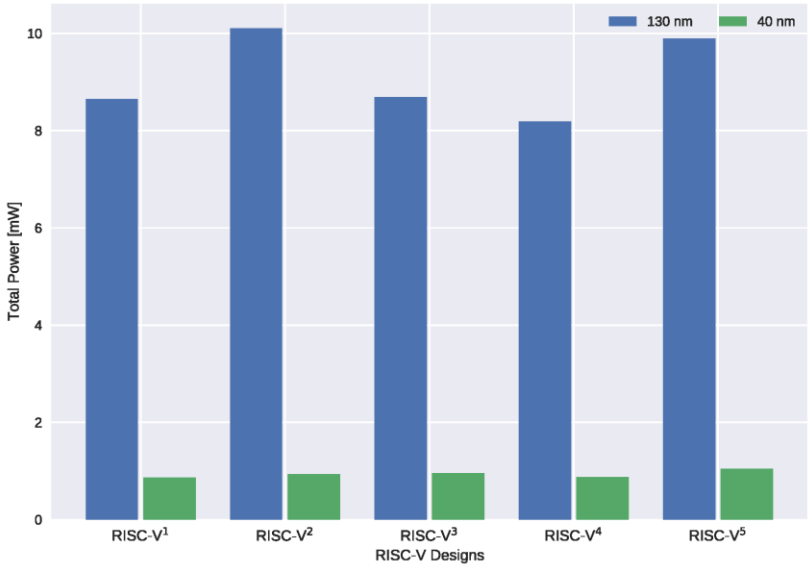
# Results (4)

## **Post Logic Synthesis** – Total Power

### Commercial Tool



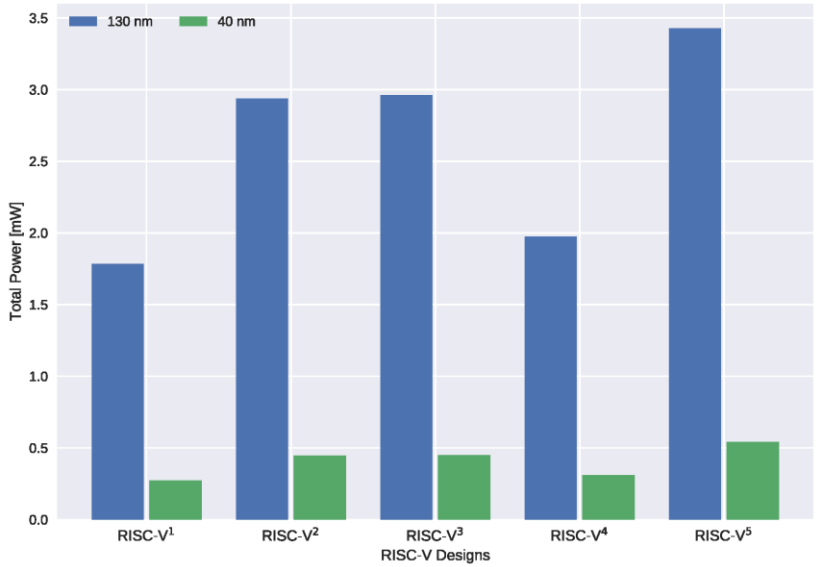

### OpenROAD



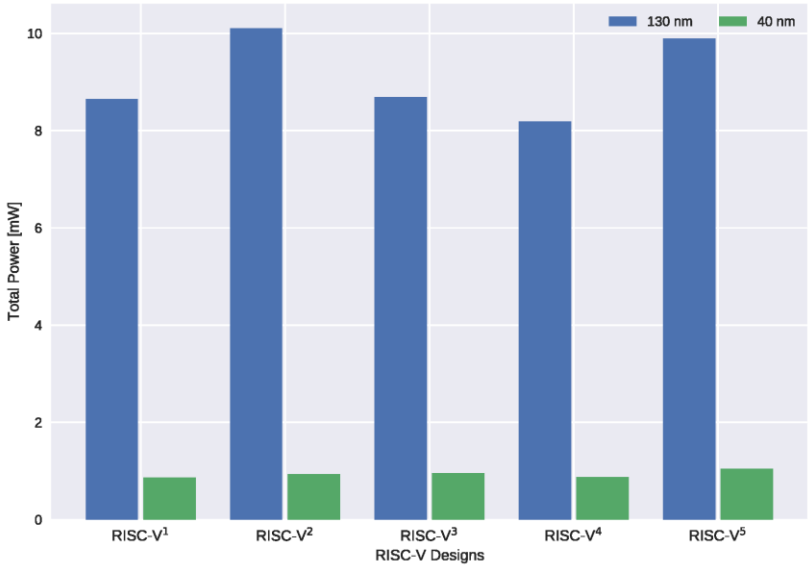
# Results (4)

## **Post Logic Synthesis** – Total Power

### Commercial Tool




### OpenROAD



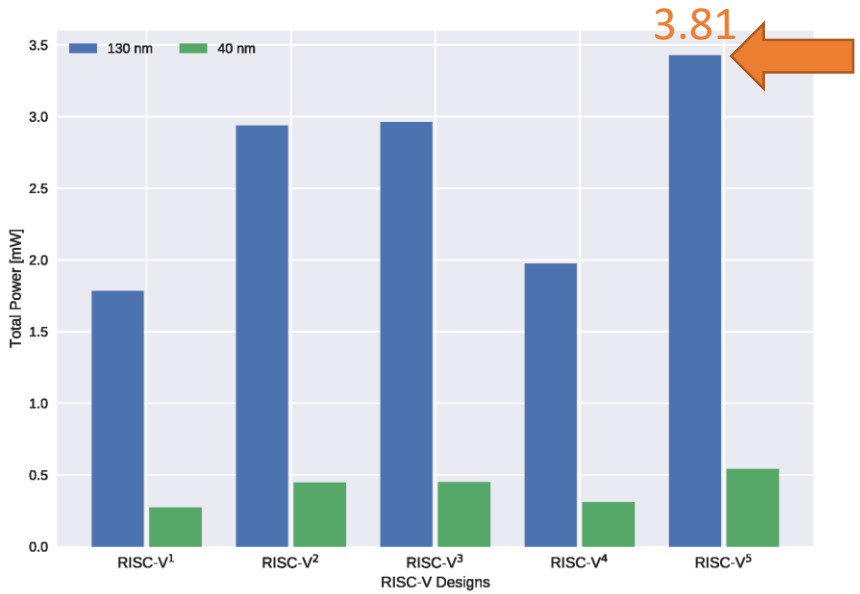

Averaging the results for all 5 RISC-Vs, Yosys/OpenROAD consumes more power:

- For 130nm: 3.8x more power
- For 40nm: 2.4x more power

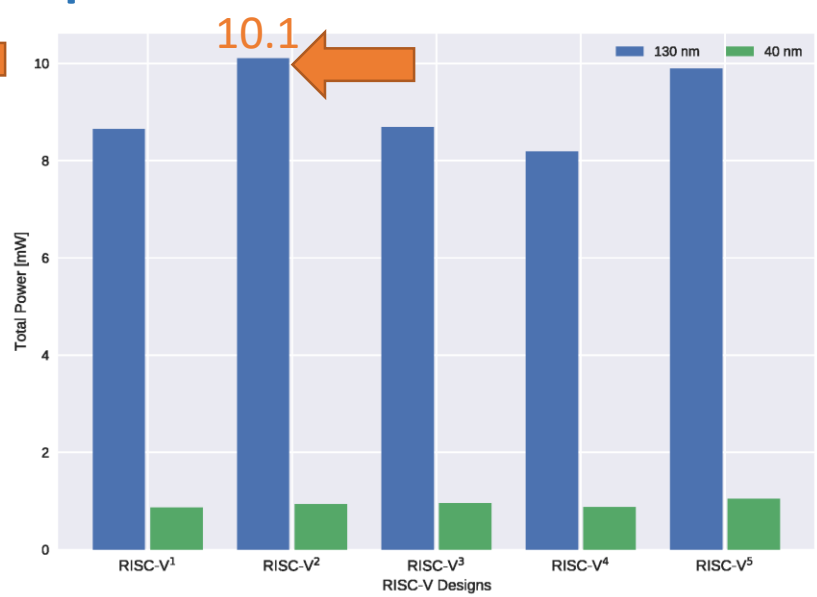
# Results (4)

## **Post Logic Synthesis** – Total Power

### Commercial Tool




### OpenROAD

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