A novel approach to standardize reusable Modular Plug and Play Skeleton Structure (MPPSS) to expedite verification closure

Chandrachud Murali (chandru.m@samsung.com),
Himanshu Dixit (hd.dixit@samsung.com),
Sriram Kazhiyur Soundarrajan (sriram.k.s@samsung.com),
Somasunder Kattepura Sreenath (soma.ks@samsung.com)
Samsung Semiconductors India Research, Bangalore, India

accellera SYSTEMS INITIATIVE
2022 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE
MUNICH, GERMANY
DECEMBER 6 - 7, 2022

INTRODUCTION

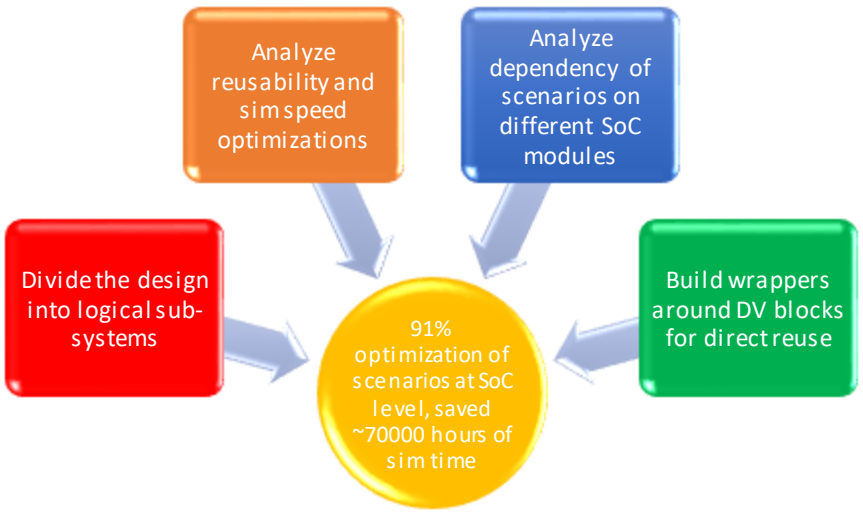

Figure 1. Overall approach and architecture

PROBLEM STATEMENT

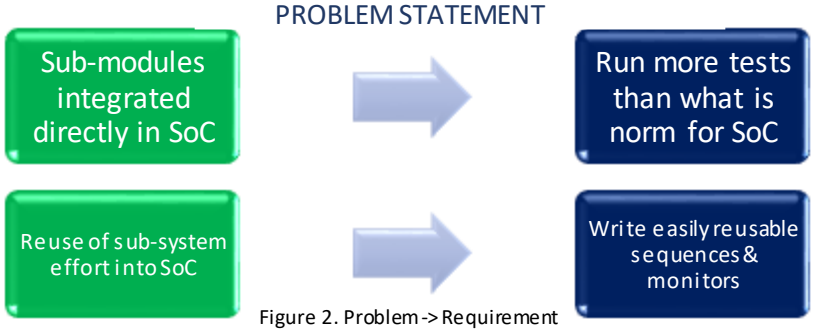

Figure 2. Problem -> Requirement

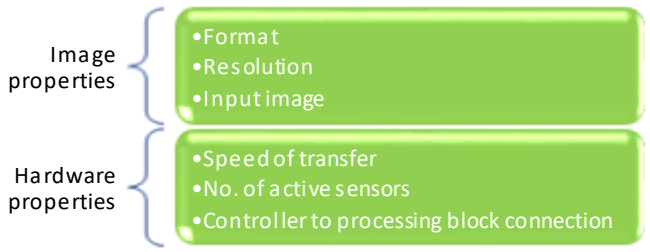

Figure 3. Feature classification

IMPLEMENTATION

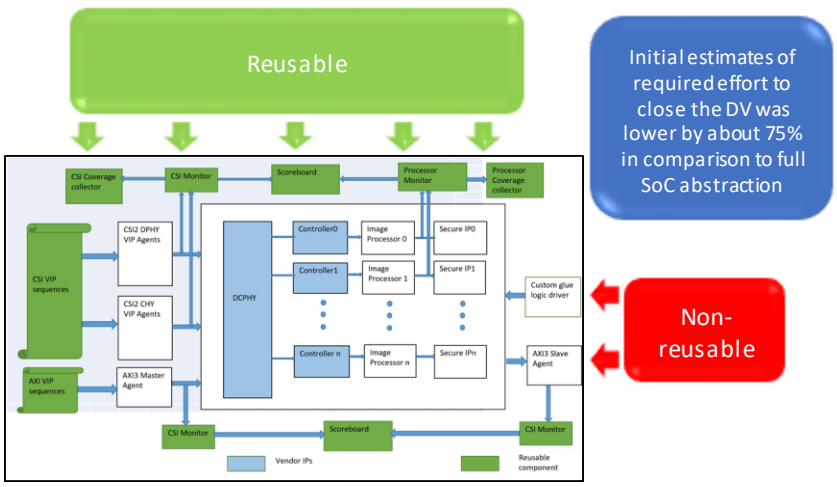

Figure 4. Sub-system testbench environment

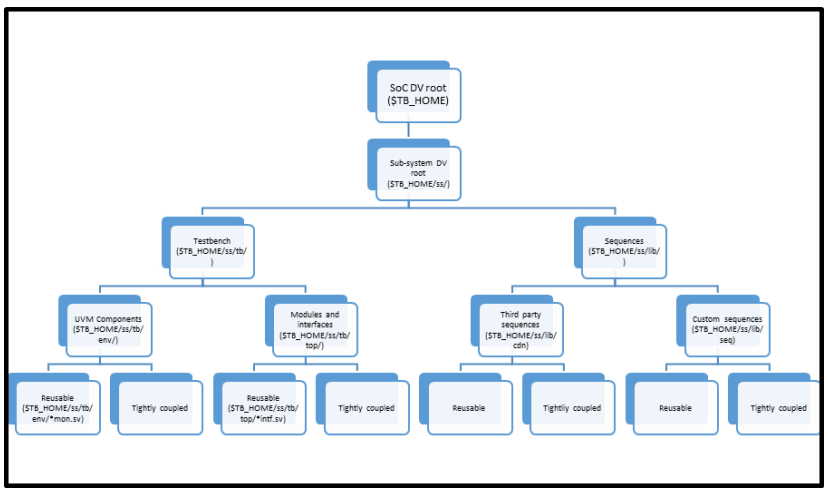

Figure 5. MPPSS architecture

RESULTS

No. of active lanes	PHY type	Speed of transfer	Lane multiplexing	Total combinations of the scenarios possible	Smoke test set at the Sub-system level	Percentage decrease in scenarios (smoke)	Total number of scenarios run at SoC level	Percentage decrease in scenarios (SoC)	Bugs found in sub-system
4	DPHY	4 slow lanes	Random	240	42	82.5	18	92.5	3
		2 slow lanes + 1 fast lane	Straight ahead	60	11	81.7	2	96.7	0
		2 fast lanes	Straight ahead	10	2	80	1	90	1
	CPHY	4 slow lanes	Random	240	52	78.3	22	90.8	4
		2 slow lanes + 1 fast lane	Straight ahead	60	12	80	2	96.7	2
		2 fast lanes	Straight ahead	10	2	80	1	90	1
3	DPHY	3 slow lanes	Random	960	142	85.2	82	91.4	2
		1 slow lane + 1 fast lane	Straight ahead	120	28	76.7	2	98.3	0
	CPHY	3 slow lanes	Random	960	145	84.9	85	91.1	3
		1 slow lanes + 1 fast lane	Straight ahead	120	31	74.1	2	98.3	1
2	DPHY	2 slow lanes	Random	720	132	81.7	62	91.4	2
		1 fast lane	Straight ahead	40	12	70	6	85	0
	CPHY	2 slow lanes	Random	720	138	81.7	65	90.9	3
		1 fast lane	Straight ahead	40	14	65	6	85	0
1	DPHY	1 slow lane	Random	160	18	88.7	8	95	2
	CPHY	1 slow lane	Random	160	21	86.8	12	92.5	2
Total				4620	802	82.6	376	91.8	26

Table 1. Design related scenario combinations

Simulation Flavor (Simulation time in minutes)	Test category	Reusable from sub-system to SoC? (Y/N)	Average SoC simulation time	Average subsystem simulation time	Improvement factor	Total SoC Simulation time per iteration (without SS)	Total SoC Simulation time per iteration (with SS)	Percentage reduction in SoC simulation time
RTL	4 sensor parallel	Y	390	18	21.67	46800	12120	74.1
	2 sensor parallel	Y	480	21	22.86	163200	76800	52.9
	Register access	N	240	9	26.67	2160	2160	0
	Clock gating	N	210	7	30	840	840	0
	Interrupt Scenario	N	330	12	27.5	2640	2640	0
GLS (Unit Delay)	4 sensor parallel	NA	690	21	32.86	8280	8280	NA
	2 sensor parallel	NA	870	23	37.83	29580	29580	NA
	Use case scenario	NA	780	21.5	36.28	7800	7800	NA
POST-GLS (Timing + SDF)	4 sensor parallel	NA	930	NA	NA	11160	11160	NA
	2 sensor parallel	NA	1020	NA	NA	31620	31620	NA

Table 2. SoC simulation vs. Sub-system simulation time

REFERENCES AND ACKNOWLEDGEMENTS

Pavithran, T.M. & Bhakthavatchalu, Ramesh (2017). UVM based testbench architecture for logic sub-system verification. *2017 International Conference on Technological Advancements in Power and Energy (TAP Energy)*,doi: 10.1109/TAPENERGY.2017.8397323
Juan Francesconi, J. Agustin Rodriguez and Pedro M. Julian, "UVM-Based Testbench Architecture for Unit Verification", *2014 Argentine Conference on Micro-Nanoelectronics, Technology and Applications (EAMTA)*, doi: 10.1109/EAMTA.2014.6906085

Samsung Semiconductors India Research, Bangalore, India