

## Introduction and Objective

Simulator Independent Verification Platform Development (SIVPD) being vendor agnostic addresses the following issues:-

- Integration of pre verified IPs/Sub Systems into a common SoC DV environment
- Less TAT for rebuilding complex verification environments onto SoC
- Reduction of both development cycle time and license cost
- Faster run times after evaluating simulation performance and options like Save and Restart, Capture and Replay

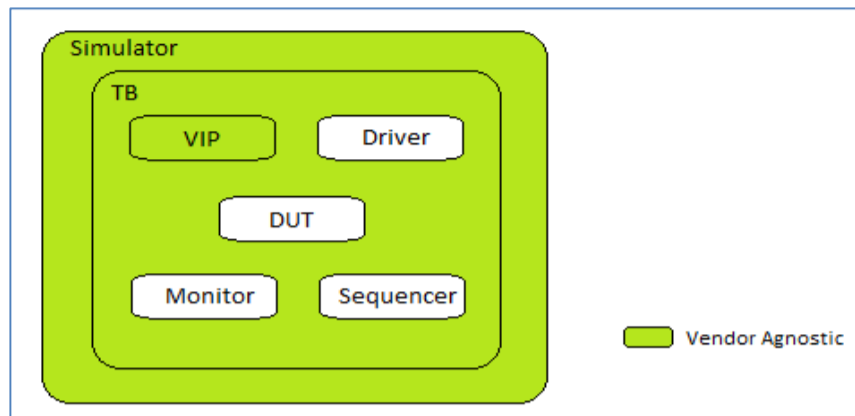


Figure 1. SIVPD Verification Environment depicting the vendor agnostic components

## Implementation

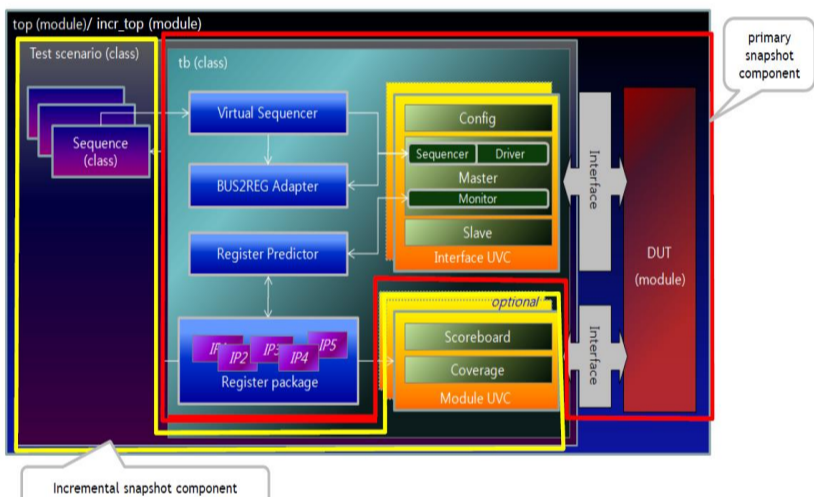


Figure 2. SIVPD Testbench using 2 TB Tops

Key differentiation for simulator specific syntax and options were handled via highly flexible perl based macro configuration approach or SystemVerilog defines.

As the SoC design is huge, multi-step incremental elaboration flow is adopted to ensure any change in tests or sequences does not necessitate re-elaboration of Design Under Test (DUT).

The testbench generation is automated based on excel input spec. It has same look and feel on various verification scopes (IP/Sub-system/SoC) (Figure 2).

This also bolsters the reusability aspect of an IP or sub-system verification environment at SoC level and vice-versa.

## Simulation Flow

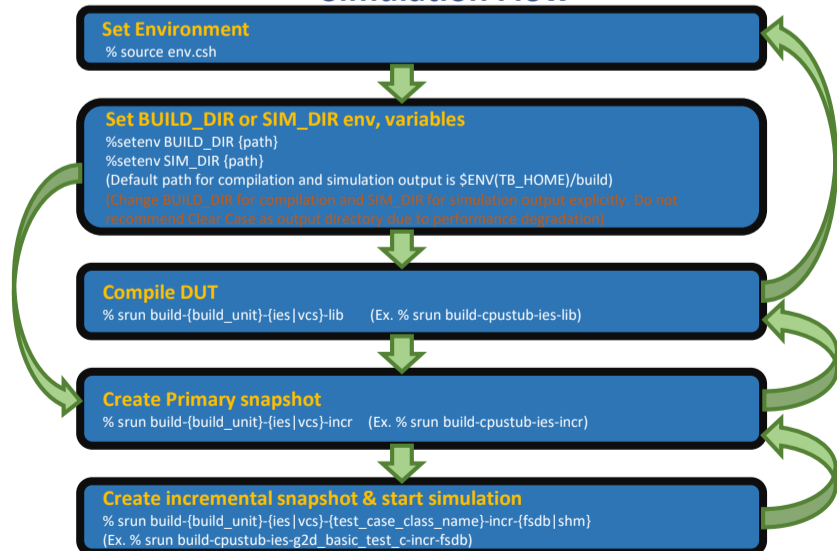


Figure 3. Simulation flow with multiple simulators

## Results

Multiple design environment (DE) created as per the IP/block use case - encapsulate all verification environment (VE) or simulator related options and switches

Plug and play TB for multiple simulators at different abstraction levels

Benefits resulted in driving Accelerated SIVPD (ASIVPD) - simulator speed improvements up to 7 times on RTL and 9 Times on PA sims

Type Of Sim/Vendor Run Time (Seconds)	Tool1	Tool2	Tool2 Vs Tool1
RTL Sim	29501	7305	4.04
RTL Sim With Dump	62145	9207	6.75
PA RTL Sim	63405	10807	5.87
PA RTL Sim With Dump	130005	14550	8.94

Table 1. Tool1 vs Tool2 Run Times