A novel approach to expedite MCU verification and enabling efficacious inter-processor communication in a multiprocessor SoC

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Introduction

- Streamlined approach to verify the processors at different level of abstractions.
- Modular Reusable MCU Testbench (MRMT) architecture developed resulting in 41% savings of overall verification effort and to detect ~25 critical Silicon breaking issues.

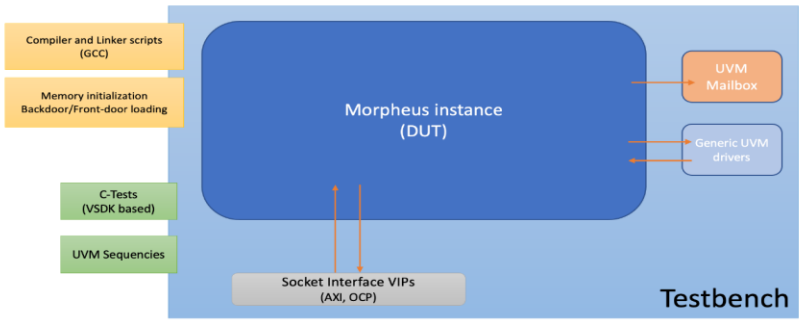
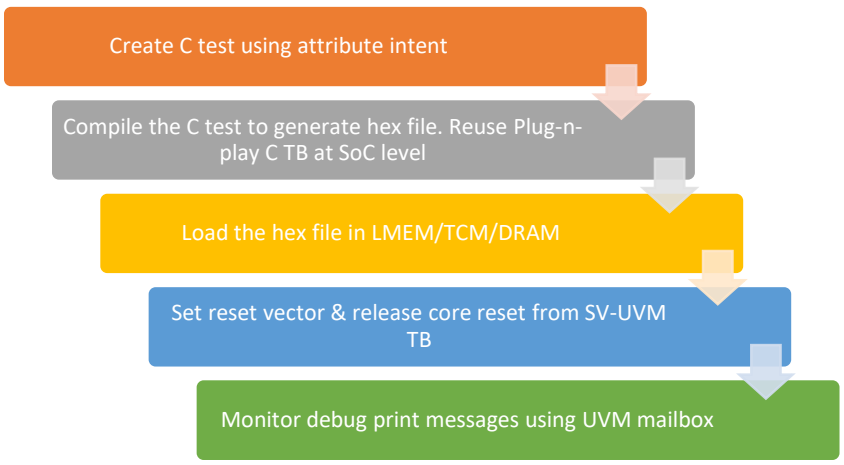


Figure 1. MRMT testbench architecture

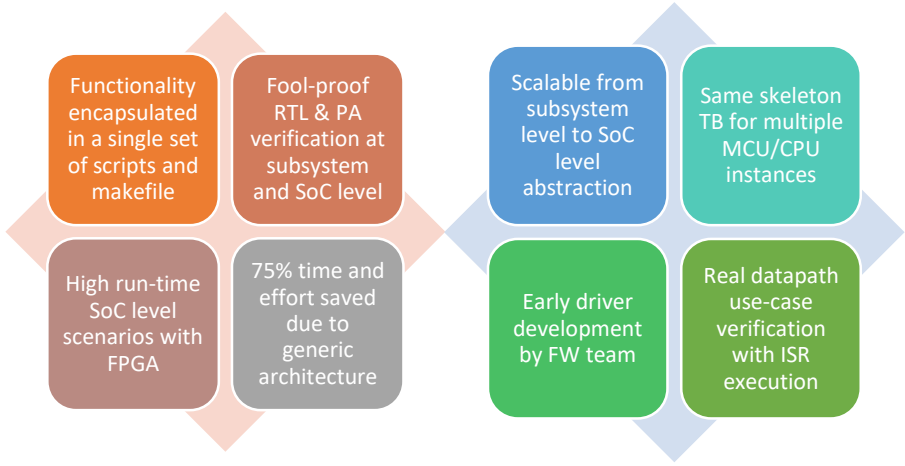
Objective

Figure 2. MCU and IPC DV Verification attributes

Implementation



MRMT Features: Resourcefulness and Reusability



IPC Features & Verification

- Inter processor communication ensued via 2 main components:
  - Mutex for resource sharing
  - Doorbell for inter processor communication via interrupts
- RoleID based security implementation.
- Firewall access in fabric verified over AxUSER fields

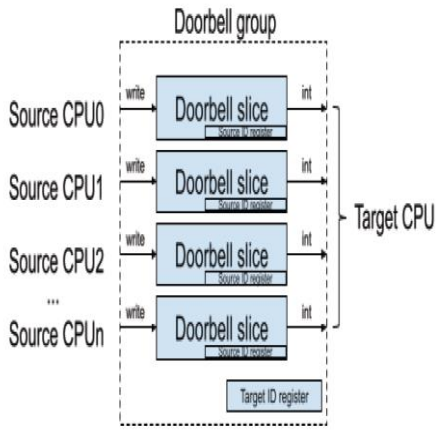


Figure 3. IPC components

Results

Created an innovative methodology to scale the verification for multiple MCU instances in an SoC while facilitating robust inter-processor communication amongst them using MRMT.
Actualized with 3 different classes of MCU in 2 XR SoCs with 16+ instances.
Tremendous 41% save in development time and manual effort.
75% save in terms of simulation time using Dynamic Save and Restart and Capture and Replay mechanisms.
Modular testbench able to detect ~10 critical Silicon breaking issues at subsystem level and ~15 bugs at SoC integration level.

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