2022 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

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A NOVEL APPROACH TO HARDWARE CONTROLLED POWER AWARE VERIFICATION WITH OPTIMISED POWER CONSUMPTION TECHNIQUES AT SOC

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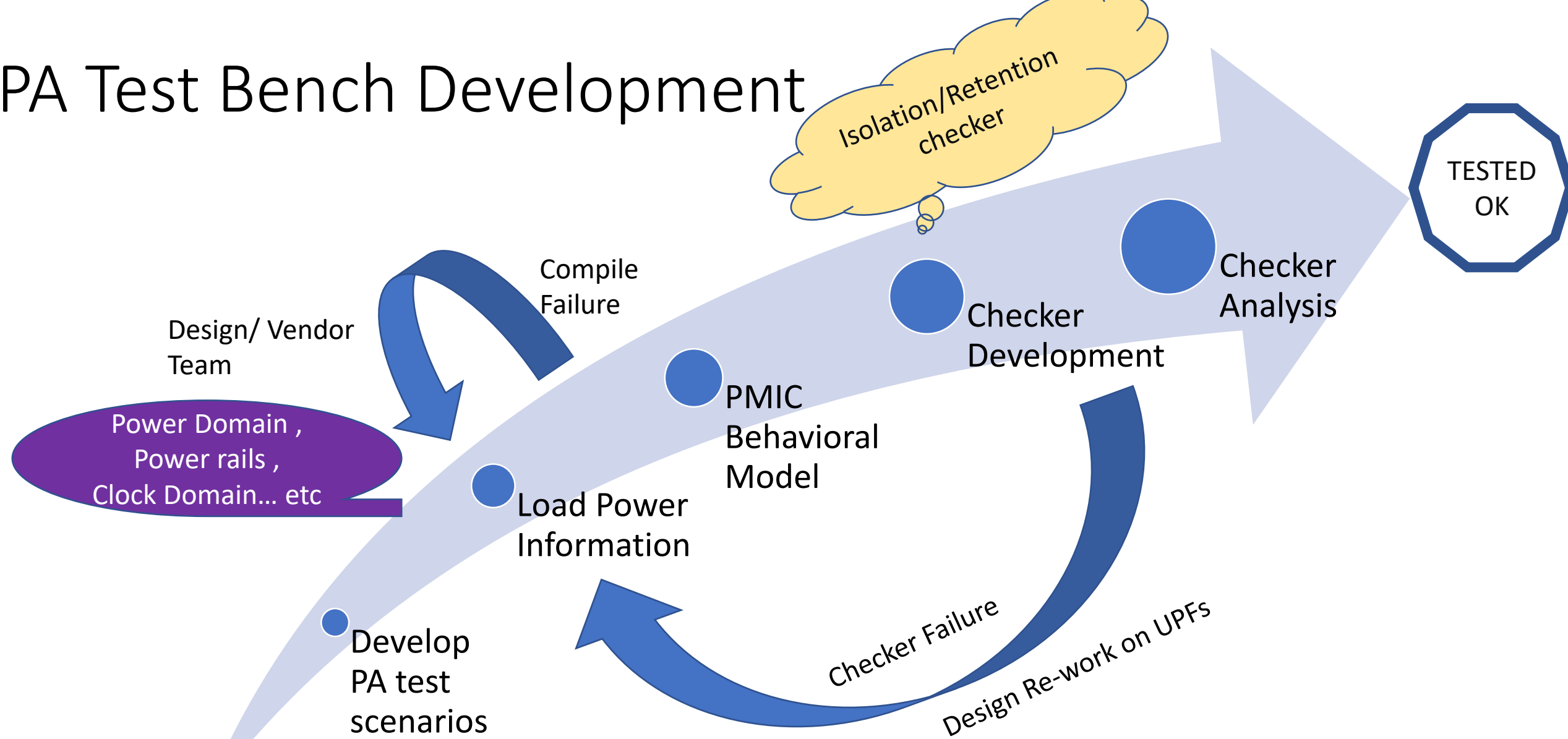
SYSTEMS INITIATIVE

Agenda

- PA test bench development
- PA test bench components
- Power saving techniques
- PMIC model
- SoC boot & power up
- Master slave architecture
- Power transition FSM
- Verification flow
- Power estimation process
- Results
- Conclusion

PA Test Bench Development



PA Test Bench Components

01 RTL

02 UPF

03 Driver

04 VIPs

PMIC Behavioral Model 05

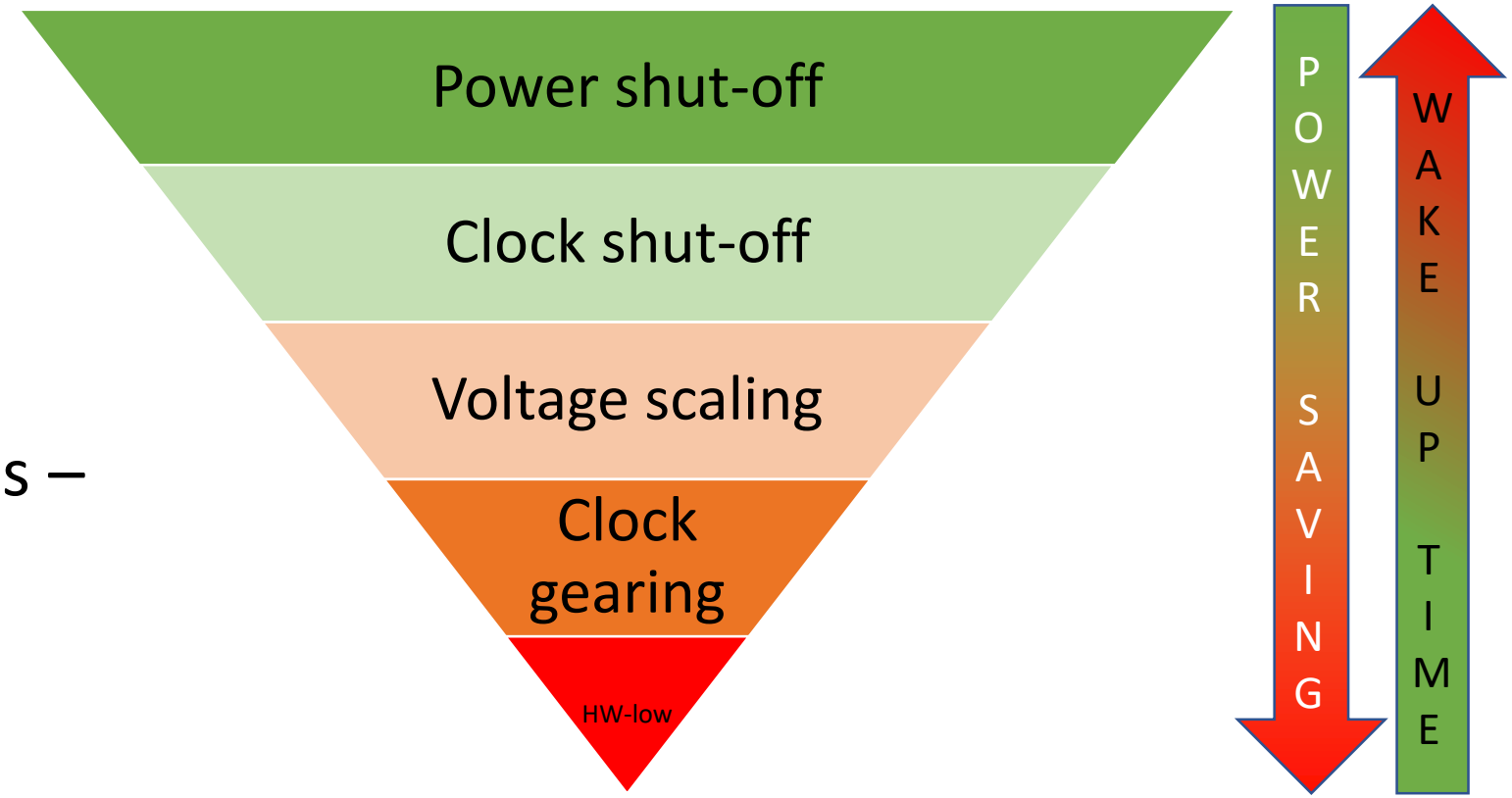
Isolation & Retention Checker 06

Coverage Model For Low Power 07

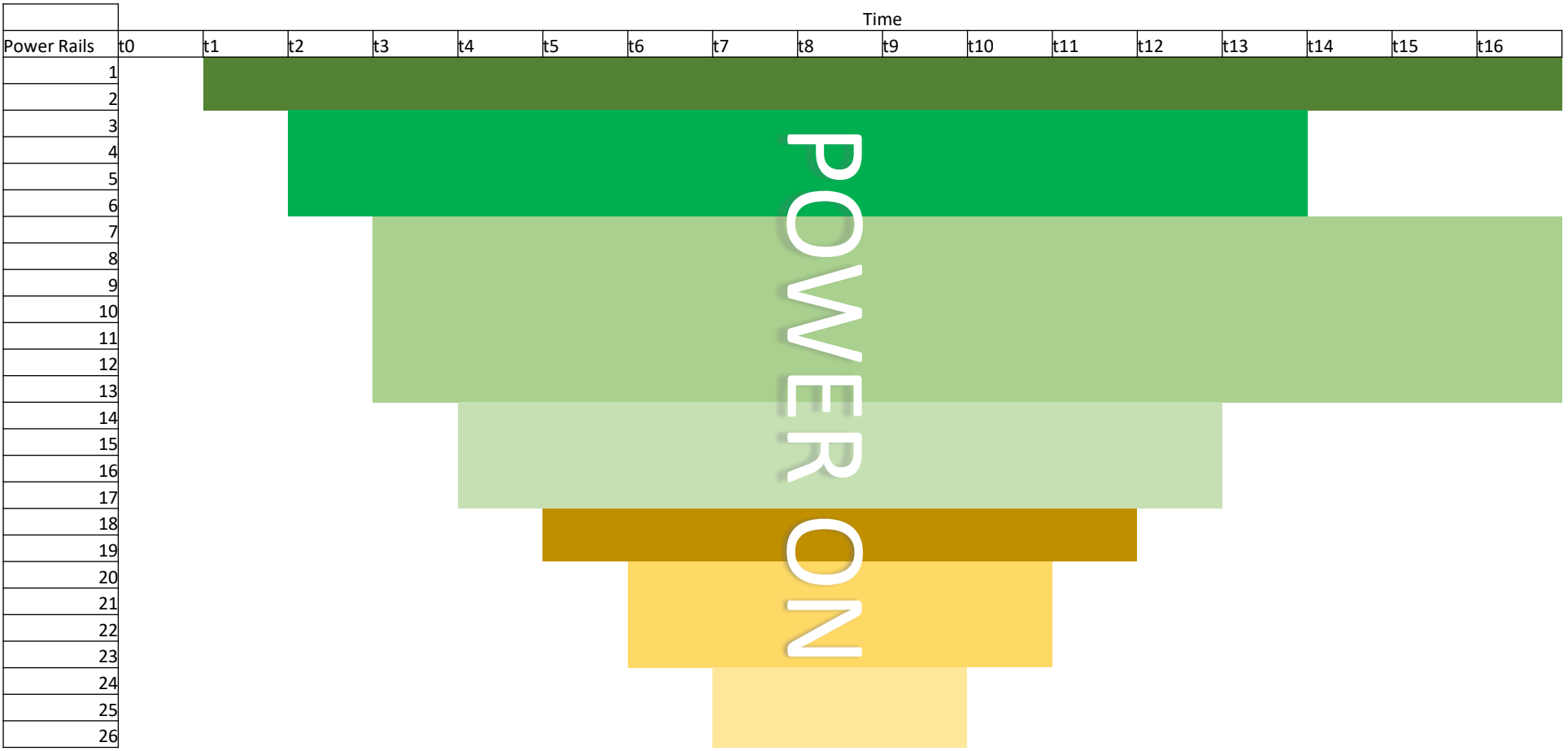
SW and HW Triggered Sequences 08

Power Saving Techniques

- Power shut off
- Clock shut off
- Voltage scaling
- Clock gearing
- Additional techniques –
  - Level shifter
  - Retention
  - Isolation



PMIC Model



STANDBY STATE

Lowest Power State of the chip

SW + HW Programing Required

SoC Boot & Power up

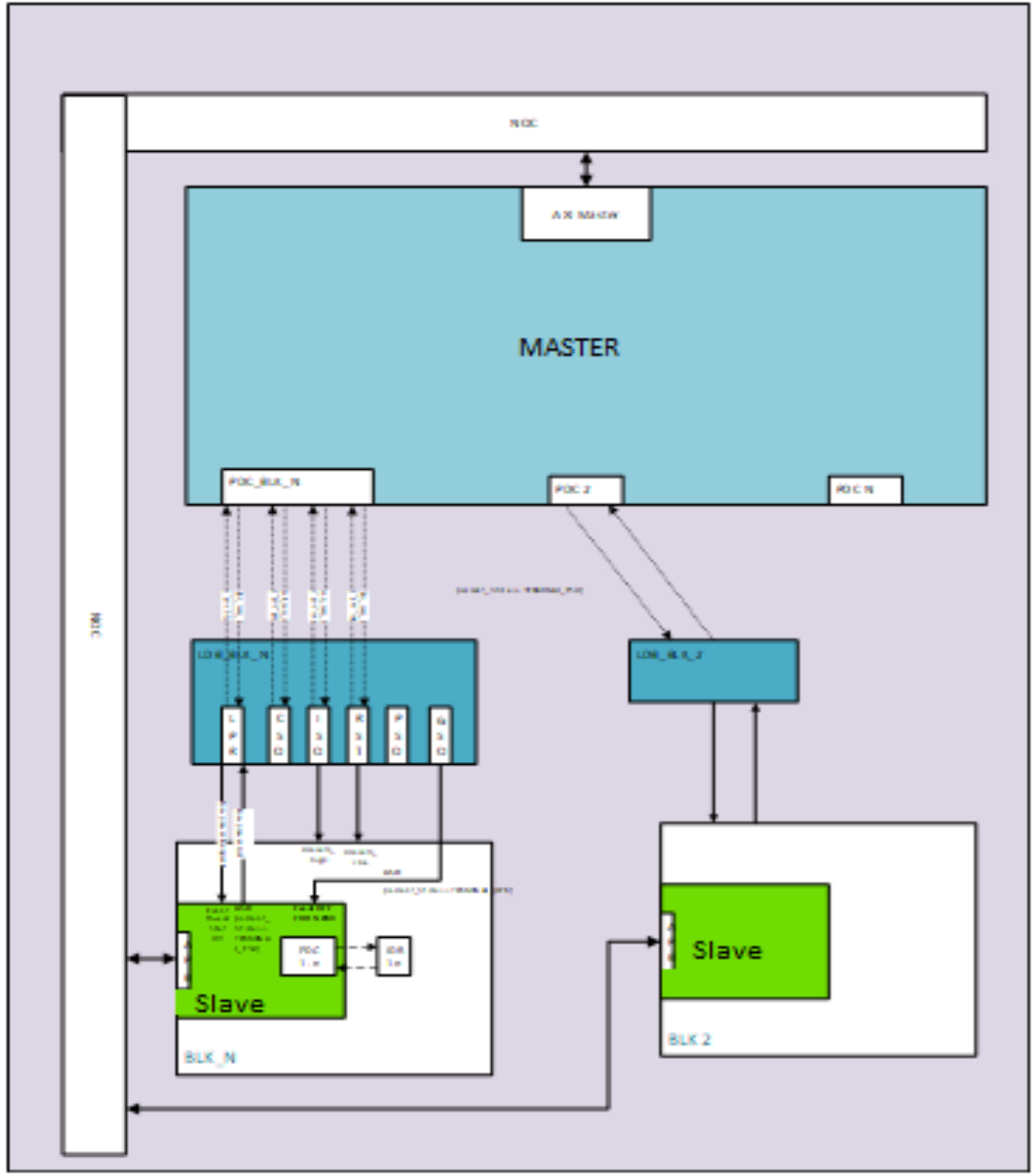
BOOT via ROM

Master Controller Power up

Master Controlled SOC PDs power up

Slave Controller Power up

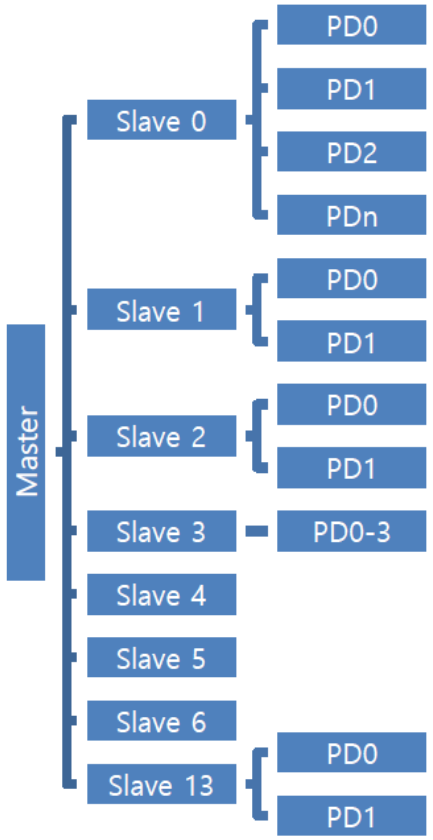
Slave PDs Power up (BLK level)



Master Slave Architecture

14 Blocks

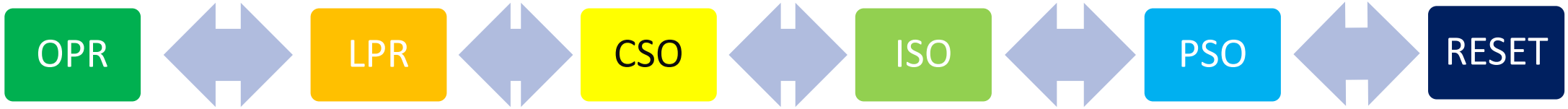
75+ Power domains



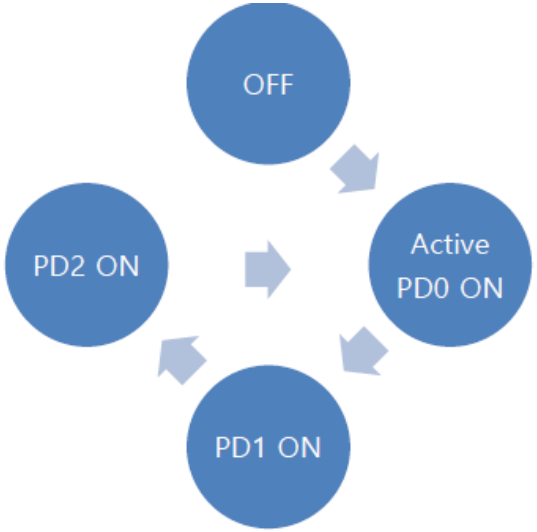
79 Clock Domains

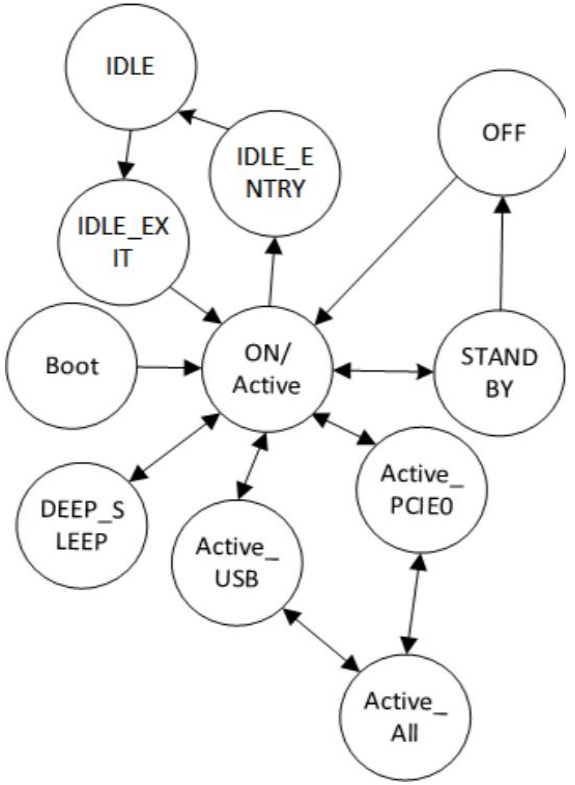
37 Voltage Rails

Power Transition FSM

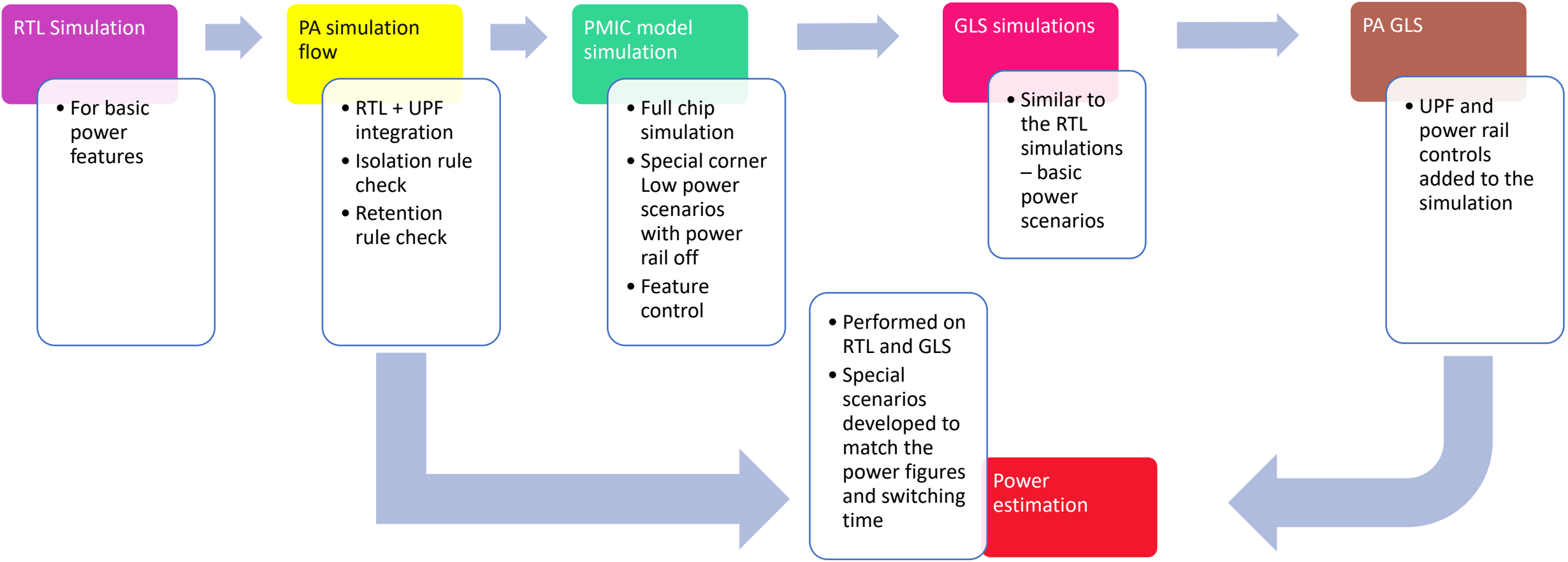


- Slave Power states and Power transitions

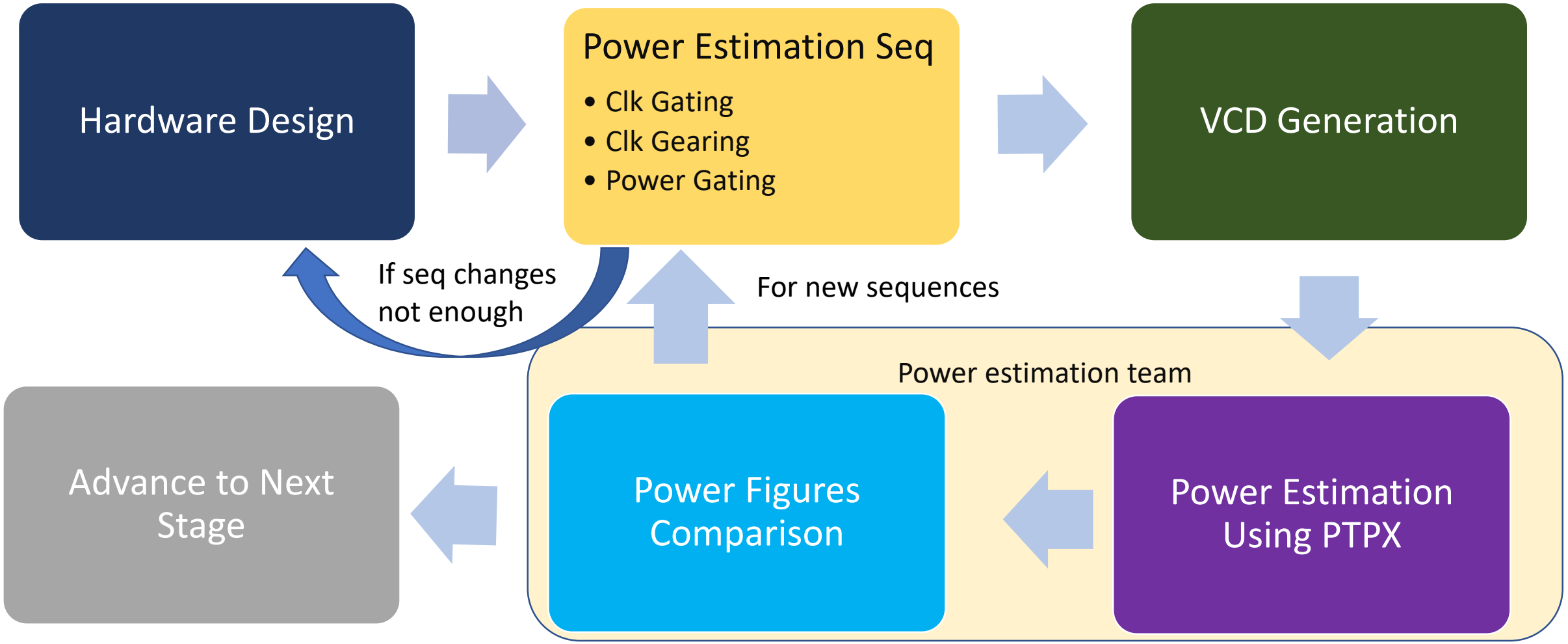




Verification flow



Power estimation process



Results

Chip Level Analysis					
	HW controlled	Software Controlled			
Scenario	Master Level Power gating	BLK level power gating	Master Level Clock gating	IP level Clock gating	Power Saving
A					0%
B				Yes	42%
C		Yes			68%
D			Yes		52%
E	Yes	Yes			83%

LEAK POWER	IDLE POWER	POWER GATED IDLE
40MW	5.99MW	0.58MW

	Block Level Analysis						
	System Register, NOC	MCU	Camera controller	Image Processor	Display controller	DMA	Power Saving
A	FC, NOP (100Mhz)	FC,NOP (800Mhz)	FC,NOP (800 Mhz)	FC,NOP (800Mhz)	FC,NOP (800Mhz)	FC,NOP (800Mhz)	0%
B	FC, NOP (100Mhz)	FC,NOP (800Mhz)	Clock gearing (100Mhz)	Clock gearing (100Mhz)	Clock gearing (100Mhz)	Clock gearing (100Mhz)	10%
C	FC, NOP (100Mhz)	FC,NOP (800Mhz)	FC,NOP (800Mhz)	FC,NOP (800Mhz)	Clock Gating	FC,NOP (800Mhz)	25%
D	FC, NOP (100Mhz)	FC,NOP (800Mhz)	Clock Gating	Clock gating	Clock Gating	Clock Gating	40%
E	FC, NOP (100Mhz)	Clock Gearing (100Mhz)	Clock Gating	Clock gating	Power Gating	Clock Gating	58%
F	FC, NOP (100Mhz)	FC,NOP (800Mhz)	Power Gating	Power Gating	Power Gating	Power Gating	68%
G	FC, NOP (100Mhz)	Clock Gated	Power Gating	Power Gating	Power Gating	Power Gating	79%
H	Clock Gated	Power Gated	Power Gating	Power Gating	Power Gating	Power Gating	91%

Conclusion

- HW triggered Power down – 40cycles
- SW Triggered Power down – 200 cycles
- Aggressive power saving techniques -> time penalty -> selection based on the real time scenario
- Master slave power controller architecture – 40% improvement
- The power estimation - RTL and GLS – meet low power req in real silicon
- DV sequences –
  - Lowest power state determination
  - Programing Sequences
  - Faster turn around time

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QUESTIONS?

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