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Reset Your Reset Domain Crossing (RDC) Verification with Machine Learning

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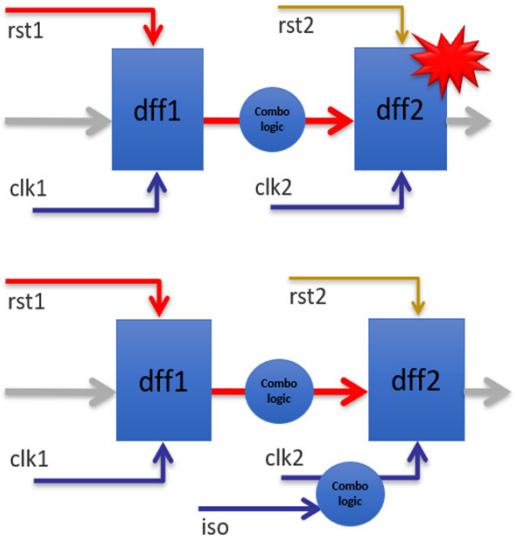
The RDC Setup and Noise Reduction Challenge



- CDC predicates RDC
- RDC constraints can be challenging
  - Ordering, Clock ISO, Data ISO
- RDC challenges include:
  - Quickly setting up a baseline of RDC analysis
  - Refining the setup to get more accurate results
  - Understanding related violations to create minimal, accurate constraints
- These challenges are well suited to automated assistance from Machine Learning (ML)

Machine Learning For RDC

Help with early setup issues

- Identify resets, gated resets
- Identify clocking schemes
- Suggest constraints to improve results

Enable a methodology which focusses on large problems more quickly to remove low level noise, resulting in greater time to review potential design bugs

Study

Purpose : To examine the benefits of applying machine learning assistance in RDC Verification, to a real world design

- Can ML for RDC perform as well as a user in generating a set of suggested constraints?
- Study looked at performance, noise and RDC results to determine effectiveness and accuracy of ML vs hand generated constraints
- Reference design
  - 10 Million state bits, 3 clock groups, 8 reset groups
  - 90K RDC paths utilise reset gating, ordering and isolation
- Design chosen as it had already undergone RDC verification, so valid constraints already existed.

Approach

Siemens EDA Questa RDC with ML

- Suggests constraints based on mining results database

To generate the ML constraints required a baseline design

- Reference design run with zero RDC constraints
  - Removed the reset ordering constraints
  - Removed the isolation constraints
  - Removed all waivers.
- Questa RDC analysis reported 10000+ RDC violations

RDC ML Assist Output

Questa RDC ML Assist flow generates suggestions for RDC constraints

- Different constraints suggestions
- Example RDC paths which are impacted
- Total number of RDC paths affected

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Section 1 : Possible reset order
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1. fifo_1_d.u_rafifo.u1.rst0
   u_csr_interface_apb.u_samplefifo.rp_gray.rst_gbl
     Affected crossings (150)
        rdc_areset_209679,  rdc_areset_217871,  rdc_areset_193295,  rdc_areset_201487...(146 more)

     Constraint :
        resetcheck order assert -from {fifo_1_d.u_rafifo.u1.rst0} -to {u_csr_interface_apb.u_samplefifo.rp_gray.rst_gbl}

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Section 2 : Possible resets with same domain
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1. u_csr_interface_apb.u_samplefifo.rp_gray.rst_gbl
   u_master_interface.u_apb_master_mc.rst_m
     Affected crossings (100)
        rdc_areset_10027,  rdc_areset_1515,  rdc_areset_1522859,  rdc_areset_1531115...(96 more)

     Constraint :
        netlist reset {u_csr_interface_apb.u_samplefifo.rp_gray.rst_gbl} -group <group name>
        netlist reset {u_master_interface.u_apb_master_mc.rst_m} -group <group name>
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ML results for baseline design

- 9 Reset ordering constraints
- 14 clock isolation constraints
- 1 reset grouping constraint

RDC ML Assist Results

RDC Results after applying Reset ordering constraint suggestions

- Baseline : 10000+ RDC violations
- Baseline + ML constraints : 440 RDC violations

Applying clock Isolation constraints

- Hand-crafted Clock isolation constraints
  - RDC crossings affected : 4446
- RDC ML Assist Clock isolation constraints
  - RDC crossings affected by : 4436

Mixing Constraints

- User reset ordering constraints + RDC ML Assist clock isolation constraints
- 221 RDC violations (Baseline 10000+ Violations)

Conclusions

- RDC ML Assist generated constraints correlate very well to user generated constraints
  - Highly similar constraints affecting similar number of RDC paths
- Combined User constraints + ML constraints yield very good results
  - RDC paths from 1000’s to hundreds with minimal effort
- RDC ML performance
  - No noticeable runtime or memory impact