

INTRODUCTION (or REQUIREMENTS)

The RDC Setup and Noise Challenge

CDC verification/setup needs to come first

RDC constraints can be challenging

- Reset ordering, clock & data isolation

RDC challenges include:

- Quickly setting up a baseline of RDC analysis with minimal noise
- Refining the setup to get more accurate results
- Understanding related violations to create minimal, accurate constraints

These challenges are well suited to automated assistance from machine Learning (ML)



OBJECTIVES

Can Machine Learning for RDC perform as well as a user in generating a set of suggested constraints?

Study looked at performance, noise and RDC results to determine effectiveness and accuracy of ML versus hand generated constraints

Reference design :

- 10 million state bits, 3 clock groups, 8 reset groups
- 90K RDC paths, utilizing various RDC mitigation strategies

Design chosen had already undergone RDC verification, so valid user-constraints already existed

RESULTS

Questa RDC ML flow generates suggestions for RDC constraints

- Various constraint types
- Example RDC paths
- Total affected RDC paths
- Constraint syntax

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Decision 1 - Possible reset order
Decision 2 - Possible reset order
Decision 3 - Possible reset order
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Decision 100 - Possible reset order
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Baseline design created by removing all RDC constraints and running analysis in Questa RDC

- 10000+ RDC Violations

ML constraint suggestions for baseline design:

- 9 reset ordering constraints
- 1 reset grouping constraint
- 14 clock isolation constraints

RESULTS

RDC ML Results

Applying ML reset ordering constraints to design:

- 440 RDC violations compared to 10000 from baseline

Applying clock isolation constraints:

- 4436 crossings affected compared to 4446 with hand-generated constraints

Applying a mix of user reset ordering constraints and ML clock isolation constraints:

- 221 RDC violations compared to 10000 from baseline

CONCLUSIONS

RDC ML Assist generated constraints correlate very well to user generated constraints

- Highly similar constraints affecting similar number of RDC paths

Combined User constraints + ML constraints yield very good results

- RDC paths from 1000's to hundreds with minimal effort

RDC ML performance

- No noticeable runtime or memory impact

REFERENCES

- DVCon Europe, Oct 2021: Resetting RDC Expectations: A Systematic Approach to Verifying Configurable Designs, and Detection of glitch-prone clock and reset propagation with automated formal analysis
- DVCon China, May 2021: Build Reliable and Efficient Networks with a Comprehensive Reset Domain Crossing Verification Solution
- DVCon U.S., March 2021: Handling Reset Domain Crossing for Designs with Set Reset Priority Flops, and Bringing Reset Domains and Power Domains Together – Confronting Issues Due to UPF Instrumentation
- DVCon Europe, October 2020: Build Reliable and Efficient Networks with a Comprehensive Reset Domain Crossing Verification Solution, and Achieving Faster Reset Verification Closure with Intelligent Reset Domain Crossings Detection