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A Generic Configurable Error Injection Agent for All On-Chip Memories

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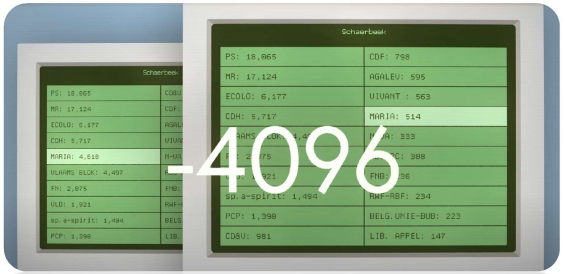
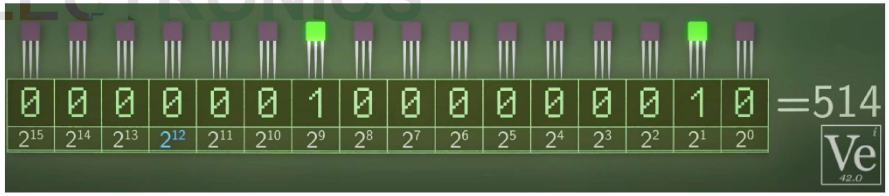
accellera
SYSTEMS INITIATIVE

AGENDA

- Memories exist everywhere
- High Probability of Bit Flips
- Need for Error Correction and Detection
- Agnostic verification of ECC Algorithm

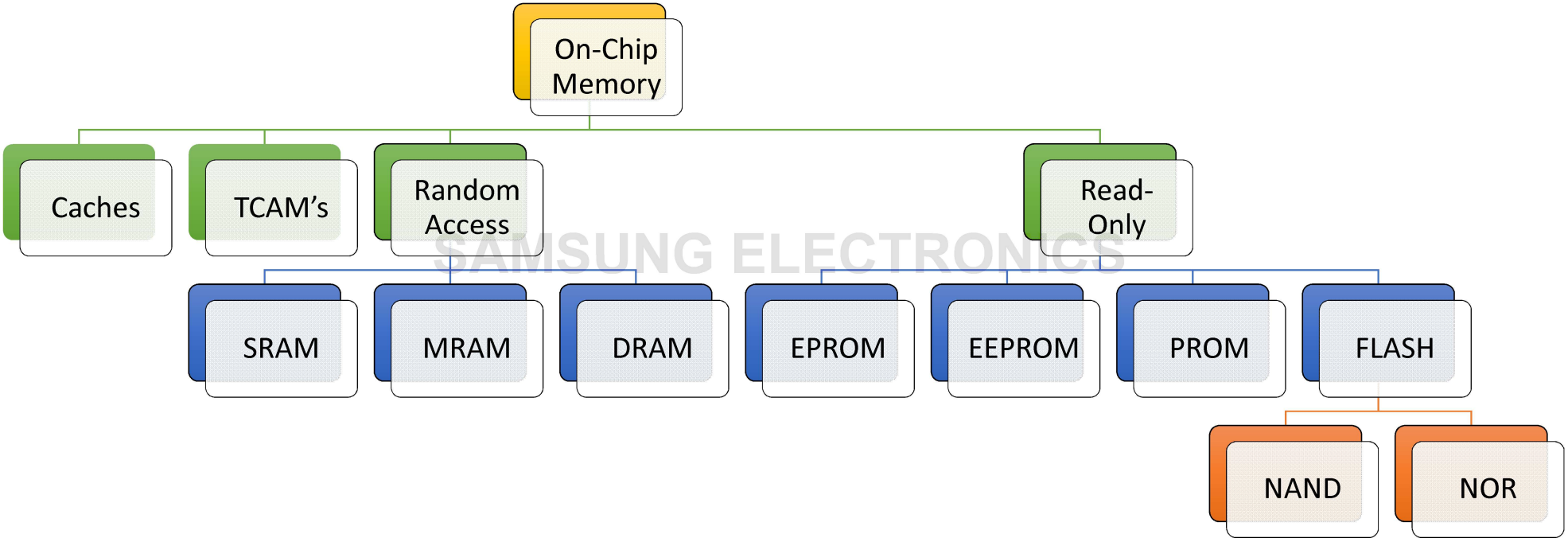
Federal Voting: 18th May 2003, Belgium



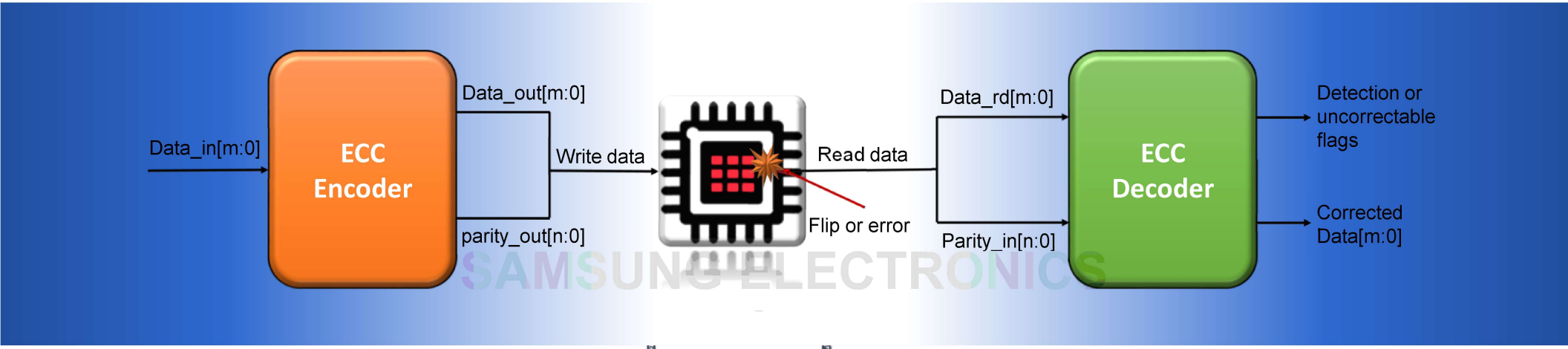


- Memory Errors
  - Soft Errors
  - Hard Errors

Motivation

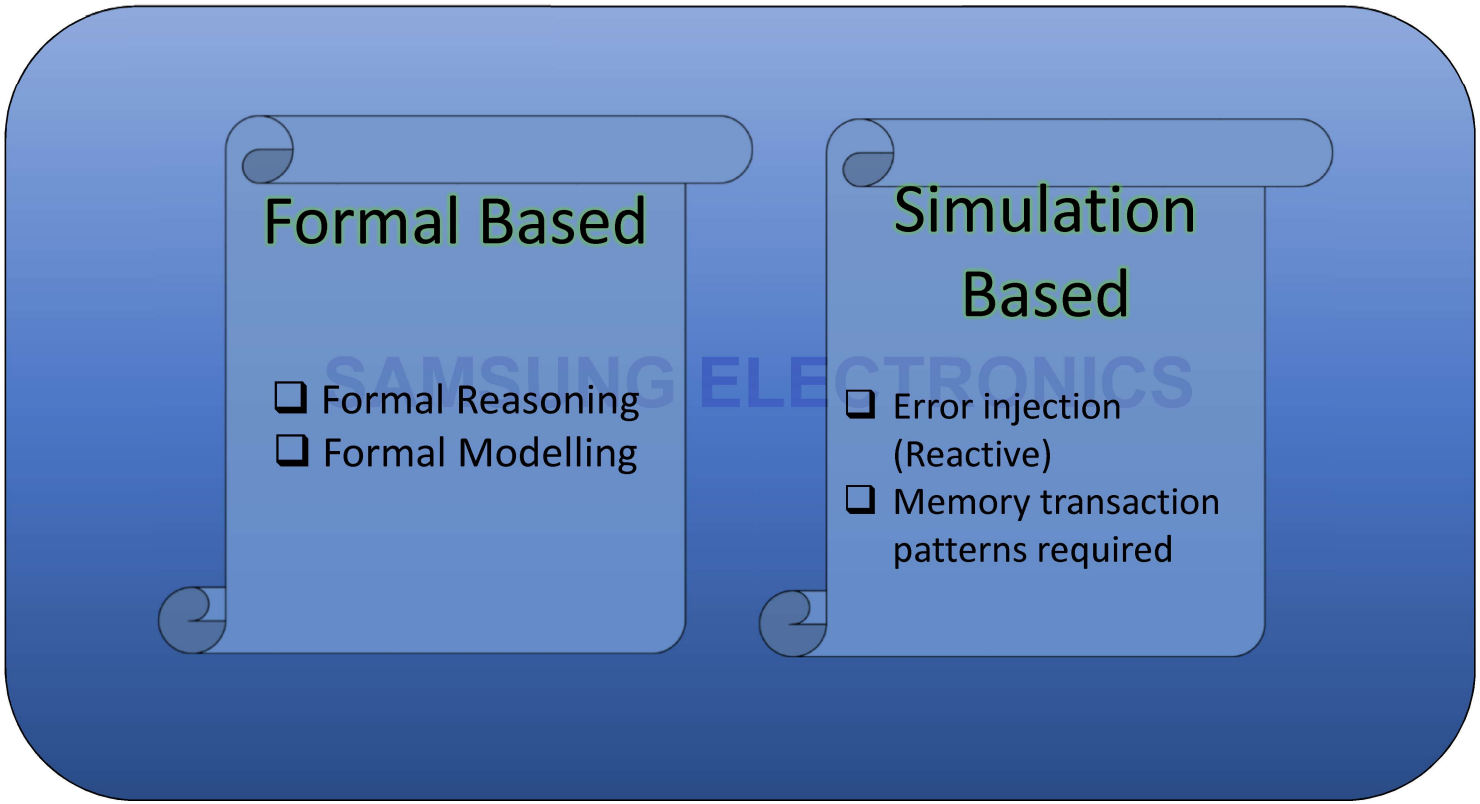


On-Chip Memories

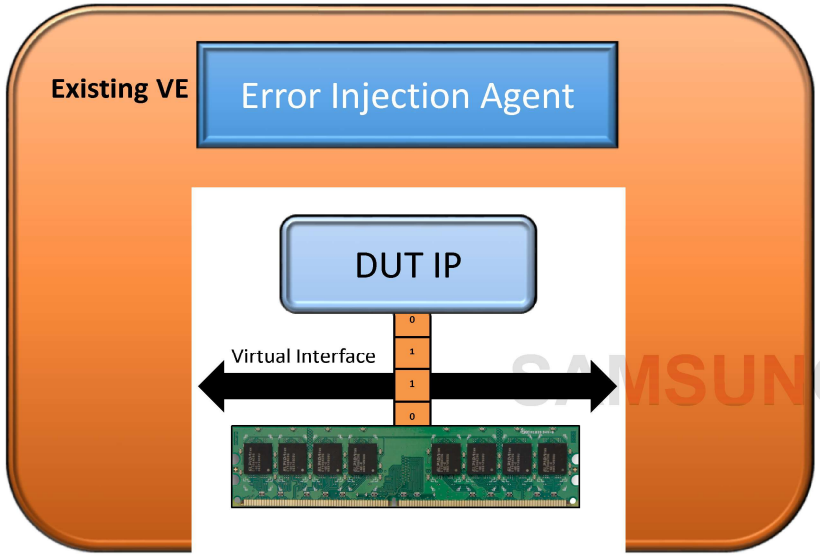


Parity Code | Checksum | Cyclic Redundancy Check | Hamming code | BCH code

Description



Existing Methodologies



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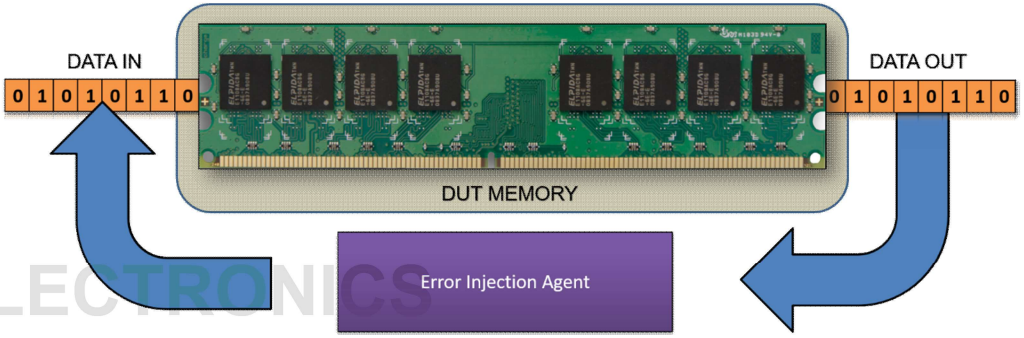

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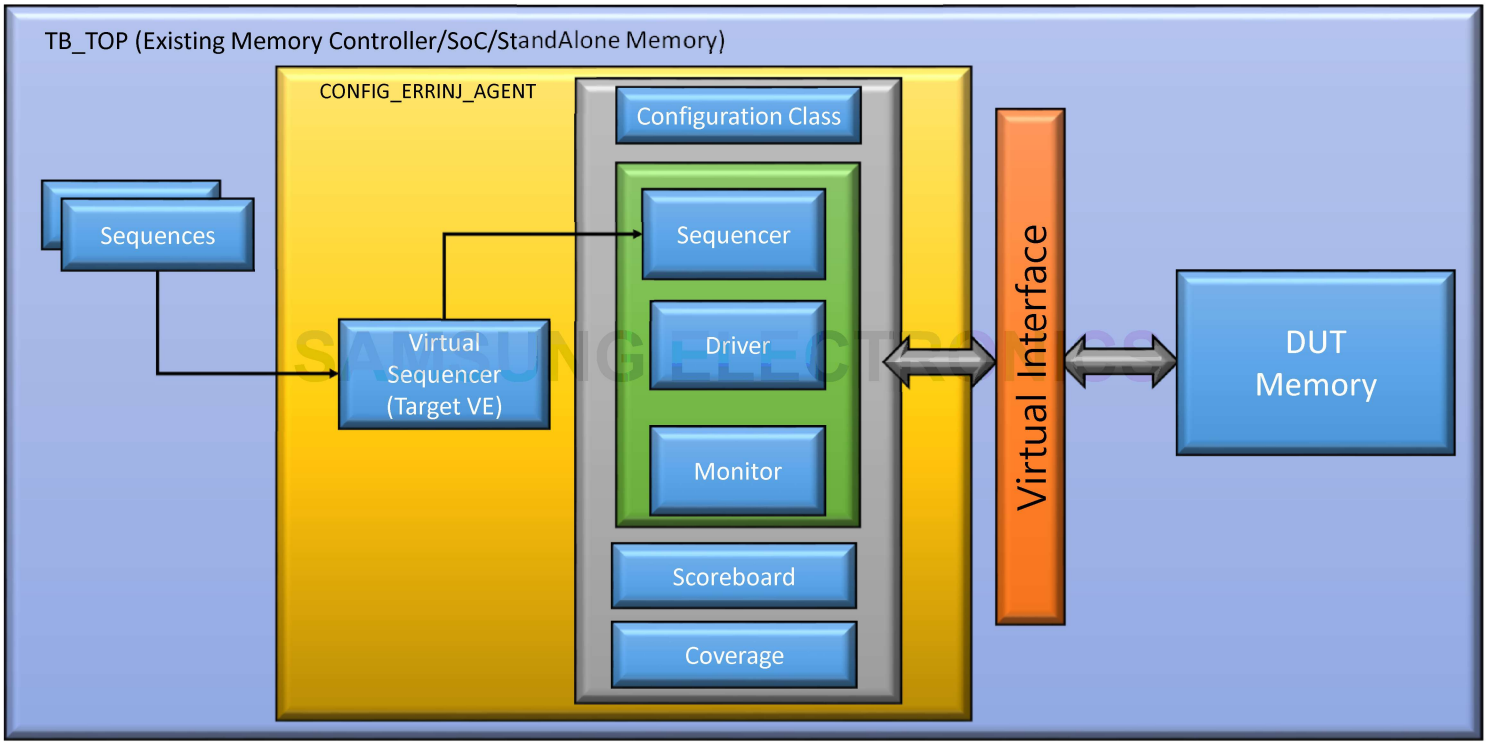
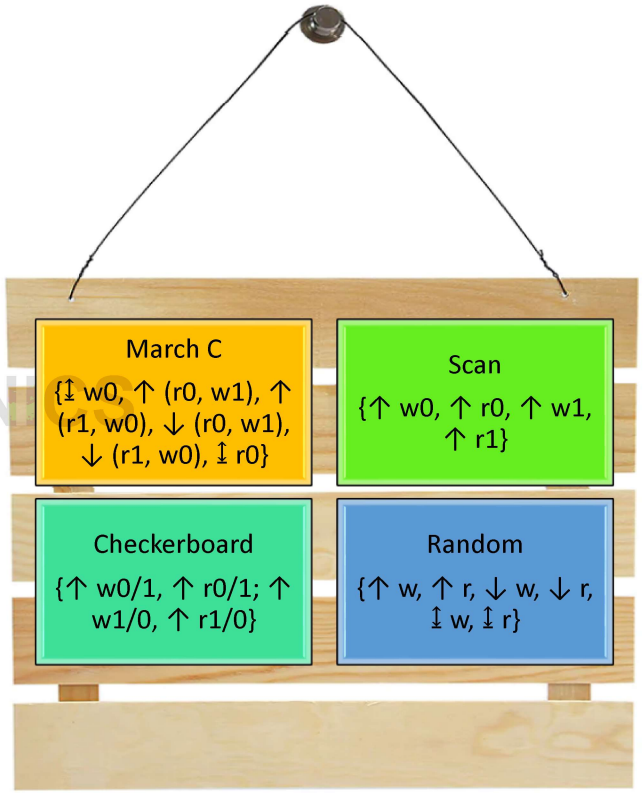
Solution



Solution

Type of Error	• SEI,DEI,TEI,MEI
Error Injection Mode	• Random,Fixed,Incremental address mode
Ratio mode	• MEI in ratios
Non stop mode	• Continuously Error injection
Fixed Error Position	• Used to create Stuck at faults
Address and Position range	• Error to be injected on a selected range of Address
Error Count	• In incremental mode, user can configure number of errors injected.
Number of ECC's	• Parallel testing for those blocks whose data width is covered by different ECC modules
Use Reference Memory	• To enable or disable checks for Memory DATA IN and DATA OUT

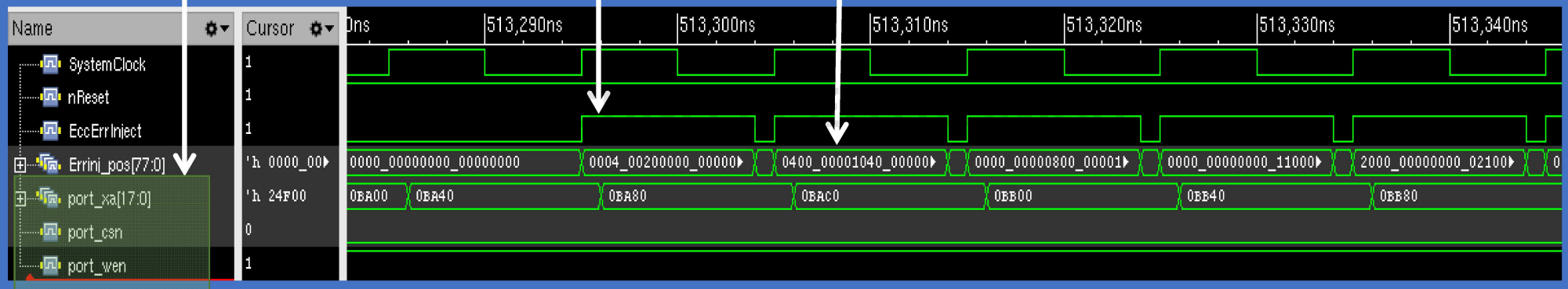


Configuration Parameters

SRAM Memory Signals:
Indicates Read Operation on XA address

EccErrInject:
Tells if Error was injected

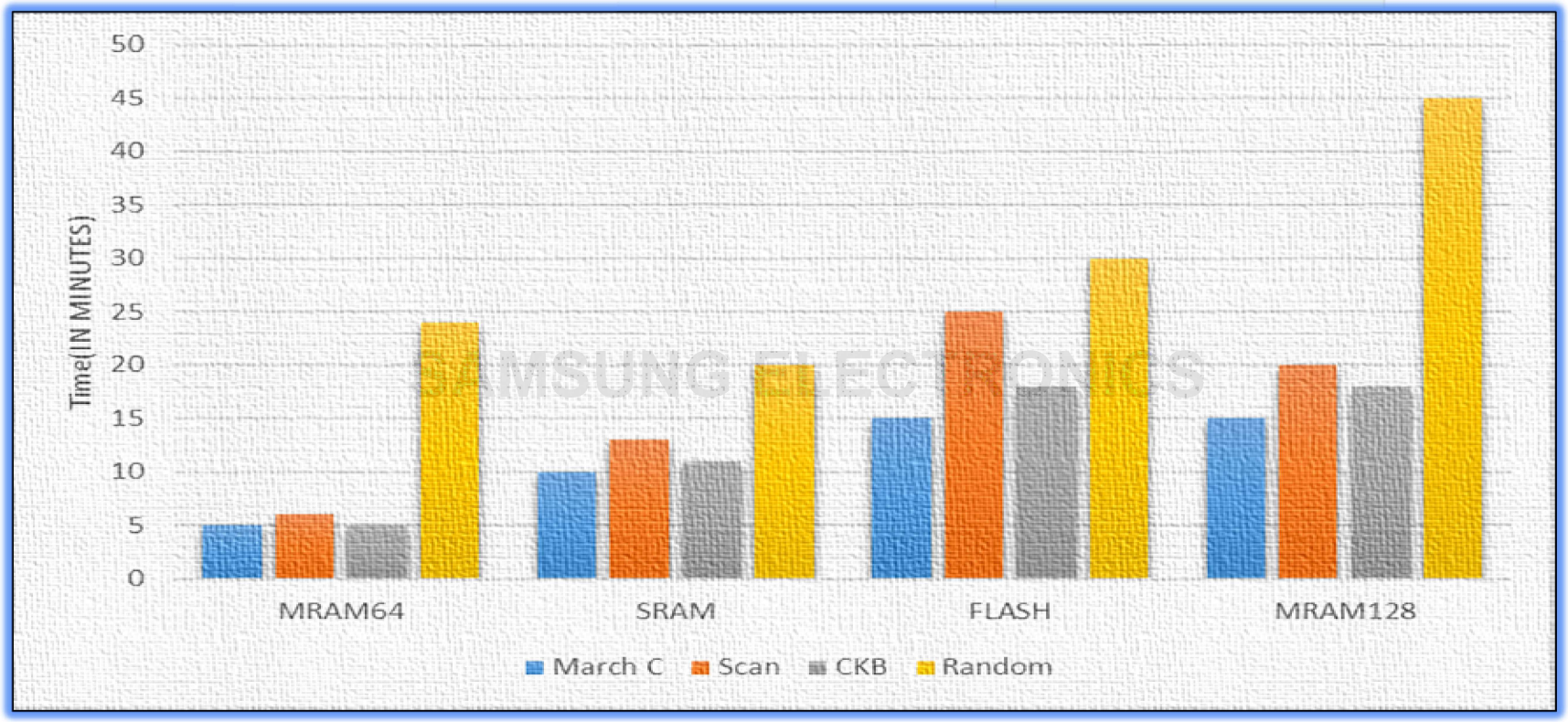
ErrinjPos:
Tells which bit position was flipped



Simulation

Memory Type	Data width	No of ECC Blocks	Number of coverage bins (RTL design code)	Simulation time saved to achieve 100% coverage	Test Bench development time saved
MRAM	64 data bits + parity bits	1	7100	**25%**	**40%**
MRAM	2*(128 data bits + parity bits)	2	18400*2	**35%**	**45%**
SRAM	32 bits + parity bits	1	400	**20%**	**50%**
FLASH	32 bits + parity bits	1	1589	**25%**	**35%**

On an average 0.5x time saved for a single instance of Memory with ECC



Results

- Early detection of bugs in embedded ECC logic
- Comprehensive and early coverage closure for ECC circuit logic
- No overhead in simulation time
- Easy to integrate with any UVM environment
- Optimizing on memory test patterns to close verification faster
- Extension on actual memory netlists (non-behavioral model) and then compare the performance metrics.

Thanks !!!