Next-Gen Verification Technologies for Processor-Based Systems

Ravindra Aneja, Synopsys
Xiaolin Chen, Synopsys
Aimee Sutton, Synopsys
Nilabja Chattopadhyay, Amazon.com LLC
Jevin Saju John, Synopsys
Bjoern Hartmann, Synopsys

RISC-V Verification Tutorial Agenda

- Introduction to RISC-V, Verification Challenges and Methodology
- Formal Verification Methodology for Single Core
- RISC-V CPU Verification Using ImperasDV and Related Technologies
- User Experience Using Dynamic Verification Methodology
- RISC-V CPU Test Generation Using STING
- Case Study Applying Formal and Dynamic Verification Technologies to an ASIP Core