Signal Integrity Challenges in rail-to-rail Parallel Interfaces designed for MEMS, Automotive & Infotainment Applications

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Abstract- **Signal integrity is a critical parameter for Qualification of new age ICs & it affects functionality as well as reliability of the system. With the new trends, increased data processing in SOC and complex handshaking with peripherals, leads to higher bandwidth, which requires an increase in the number of output buffers. Electromagnetic Compatibility (EMC), Simultaneous switching Noise (SSN), Crosstalk & transmission line play significant role for ensuring signal integrity of IOs. System level overshoots & undershoots concerns circuit reliability, mutual coupling between elements at printed circuit board (PCB) indicates risk of electromagnetic interference. The industry faces significant constraints in ensuring the design performance in diverse real-world environments. Despite its importance, the challenges of interpreting silicon and CAD design concepts into real-world applications remain underdiscussed. This paper explores how ensuring signal integrity is challenging for IO interfaces & mapping of signal integrity concepts with CAD & Silicon is done in subsequent sections. Eldo simulator has been used to analyze signal integrity & for reflecting silicon observations on CAD.**

I. Introduction

One of the hot topics in circuit design is Signal Integrity. Seamless transmission of data is of utmost importance to ensure accurate and reliable communication. Study and analysis of various factors such as crosstalk, transmission line characteristics, SSO is crucial in CMOS circuits from the perspective of signal integrity because it dictates the qualities of a signal. In a chip IOs are placed at periphery & it can work as a Transmitter or a Receiver, so when an IO is working as a transmitter it drives off chip environment. In current scenario a General-Purpose-Input/output (GPIO) circuit works at few hundreds of MHz (in time scale few tens of nanosecond) for driving external loads. When an IO is configured as a transmitter SSO comes into picture. Simultaneous switching outputs (SSO) expresses the number of IOs which can switch per supply/ground pair meeting all dynamic requirements & SSO number is a strong function of SSN. Transmission lines are interconnect traces that carry the signal from driver to receiver. It may happen that the signal transmitted from driver gets distorted due to various transmission line effects before reaching the receiver. Similarly, the presence of parasitics between adjacent lines can result in coupling leading to crosstalk. Understanding and minimizing the effects of these factors is pivotal to preserve signal fidelity and minimize errors. Signal Integrity has been studied and demonstrated vividly in all available literature. This paper is inspired from the learnings captured in Ye and C. Ye, "Transmission Lines and Basic Signal Integrity," *2018 IEEE Symposium on Electromagnetic Compatibility*, *Signal Integrity and Power Integrity (EMC, SI & PI)*, Long Beach, CA, USA, 2018. Mentioned paper studied importance of signal integrity, issues contributing to signal integrity & possible mitigations, but it didn't deal with signal integrity issues in SOC with real time application of IPs. However, in our work we demonstrated concepts of signal integrity, mapping signal integrity with IO ring which eventually allowed us to enter into system level study of signal integrity challenges for IOs. This Paper is organized as follows. In Section II, Signal integrity challenges such as Electromagnetic compatibility, Crosstalk, Transmission line effects, Simultaneous switching noise are discussed in detail. In Section III CAD analysis & its silicon correlation are provided, Section IV has conclusion of the paper followed by references.

II. SIGNAL INTEGRITY CONSTRAINTS IN INTERFACES

A. Electromagnetic Compatibility (EMC)

It is the ability of a system to function satisfactorily in its electromagnetic environment without any electromagnetic disturbances to nearby environment and this depends on materials, size, geometries, PCB technologies, electrical operating conditions (i.e., clock frequencies, dynamic currents). To catch potential issues and cut the cost of the fixes, the modern trend is to measure and assess the EMC performances at every development step i.e., at component, module & system levels. The IEC Normative 61967 (Emissions) and 62132 (Immunity) define a reference test condition for the integrated circuits [1].

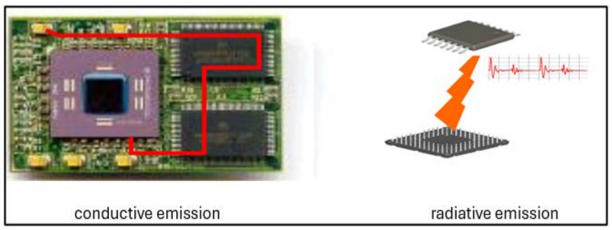

Figure 1(a).

Meeting EMC requirements is critical to bring the value in market for the products being used in RF applications. Interference of RF energy with the device may cause unwanted behavior. In IO it may cause disturbance in the noise rejection ability of receiver (hysteresis) which is a very critical parameter for the design. This issue can be minimized by anticipating the EMC behavior of circuit by testing it when exposed to RF environment.

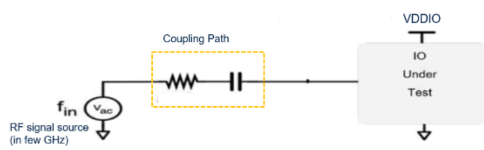

Figure 1(b). EMC testing simulation setup

Above figure illustrates how we can anticipate the impact of harmonic distortion through simulation. RF signal gets coupled to IO pad through coupling path. Critical specs of receiver such as input thresholds, hysteresis etc. can be measured after coupling. Secondly, steps should be taken to minimize the interference and protect the design . For protection against strong external electro-magnetic fields on-chip filtering can be done by implementing passive filters preceeding IOs receiver block. Shielding can also be done to avoid coupling between source and victim devices.

B. Crosstalk

Process-technology scaling results in adjacent interconnects shrinkage, leading to increased coupling capacitance. The presence of parasitic capacitances, inductances, and resistances in adjacent transmission wires can lead to unintended coupling [4]. The crosstalk in ICs can be between the interconnects, bonding wires, power pins or signal pins. In perspective of rail-to-rail signals, these unwanted fluctuations (due to crosstalk) in data lines lead to timing errors, increased noise profile, poor signal quality & excessive overshooting/ undershooting. Crosstalk will ultimately affect both signal integrity & circuit reliability.

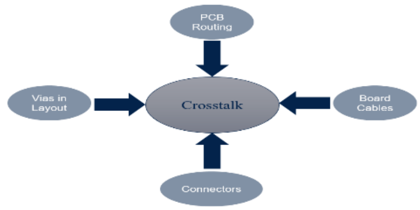

Figure 2: Sources of crosstalk in an IC [5]

Increasing spacing between adjacent lines is the best way to mitigate the problem but can end up eating wider area on boards. Another alternate way is Shielding [5] which decreases the shared inductance present between the path of interconnecting lines. Some other techniques to minimize the effects of crosstalk are to take care if high frequency signals can travel far from other traces carrying signal, also optimized routing, placement in layout design to keep the spacing of wires or traces of a circuit in a way can reduce the crosstalk. In IOs capacitive coupling in Ball Grid Array (BGA) could occur due to lead-to-lead and lead to ground capacitance in the package frame or substrate. More than one coupling path remains active at the same time, Capacitive and Inductive paths are often both present. One is usually dominant, however in the substrate noise transmission, capacitive and conductive coupling works together.

C. Transmission Line Effects

Transmission lines are an essential component in carrying signals between integrated circuits (ICs) & these lines act as a bridge for inter-system & intra-system communication. When the transition time of the interface signals are comparable to the delay of the interconnect traces, then interconnect acts as transmission line having certain delay and characteristics impedance. In reference to IOs it is observed that when there is a mismatch between the impedance offered by IO driver & transmission line, discontinuity is created & this is very common at IO pins. Due to this, the signal travelling through these lines loses the portion of energy which gets reflected back. These reflections distort the waveform. Reflections at driver can be minimized through series termination on board or we can deploy internal resistance stage after IO driver thus matching the impedance between driver stage & interconnect trace. Reflection coefficient can be described as,

$$Reflection\ Coeffiecnt = \frac{Z_L - Z_o}{Z_L + Zo}, \quad \begin{array}{l} Z_L = Termination\ Imdedance\ of\ Transmission\ line \\ Z_o = Characteristic\ impedance\ of\ Transmission\ line \end{array}$$

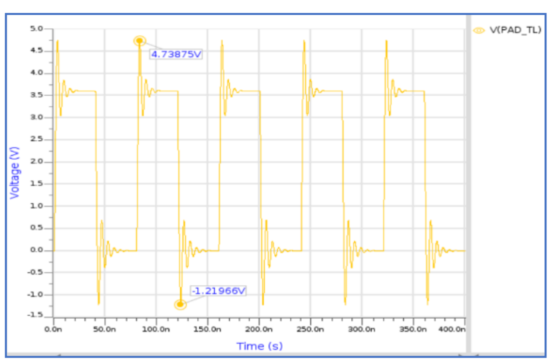

Figure 3: Output of IO transmitter with Transmission line (higher overshoot/undershoot could lead to reliability concerns.)

D. Simultaneous Switching Noise

It has been discussed continuously that there is a need for high-speed circuits to ensure faster data rate so a large number of output buffers with higher driving strength are required. In an IC IOs placed at chip periphery are connected to the pad (Pad is a physical place in an IC which receives/transfer signals from/to external world) through bond wire & bond wire possess an inherent inductance. To provide power connectivity, supply/ground pads are inserted in the IO ring. But due to this inherent inductance supply/ground signals experience shift in their actual DC levels. Equation governing drop in supply levels are as follow:

$$V_{drop=} L * \frac{di}{dt}$$

di/dt: Slew introduced due to driver switching.
L = Inductance of bond wire

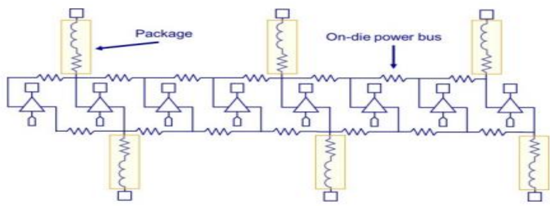

Figure 4(a) Multiple IOs sharing same supply/ground connected through bond wires [2].

Now to maintain higher data rate we intend to switch number of parallel buffers thus the non-linear noise on supply due to simultaneous switching increases (because of the effective inductance of bond wires & di/dt of switched drivers). Excessive voltage drop can raise challenges such as decreased drive capability that can lead to various timing errors like slower rise/fall transitions at output. With the reduced voltages, threshold voltage decreases leading to insufficient noise margin and making the circuit more prone to external noise. Not only this, even the excessive surge in voltages can lead to dielectric damage causing transistor gate oxide reliability issues.
SSN can be mitigated through packages having lesser inductance [3] also by limited drive capability of transmitter we can control 'di/dt' which will improve SSN. The output slew rate can affect the shoots in a critical manner. The slower the output slew, lesser will be the bounce and this leads to an important trade-off between performance and signal integrity.

$$VGND = – Lg * di/dt$$
$$i(t) = Cload* dVo/dt$$

Lg = bond wire inductance of ground terminal, di/dt= rate of change of transient current driving the capacitive load, dVo/dt- change of output voltage in time. VGND = Ground bounce

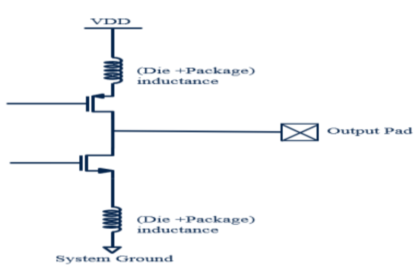

Figure 4(b): IO driver with lumped inductance on supply/ground rails.

Keeping the constraints of simultaneous switching IO buffers is important to ensure the proper functionality. The duty cycle being the critical output parameter needs to be ensured in the range of (40-60) %. From the reliability perspective overshoot and undershoot should be below exceeding limit (typically ~500mV). Emphasis should be there to analyze the worst case which will be the fastest PVT condition.

III. SIMULATION RESULTS

A. Simultaneous Switching Noise

SSO evaluated on IO transmitter designed for Analog & MEMS application in 130nm node. This transmitter supports wide range of supply voltage (1v2/1v8/3v3) +/-10% so managing slew ‘di/dt’ at higher supply voltage was major challenge. In 130nm node device size is small which leads to smaller package. Miniaturization of package improves overall cost, but it also leads to increase in chip density which imposes some drawbacks such as coupling, leakages etc.

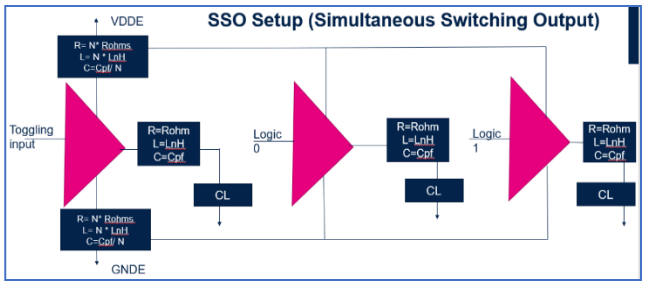

Figure 5: CAD setup of SSO analysis

R, L, C = Modelling of package parasitics as lumped resistor, capacitor & inductor

N = It represents the SSO number

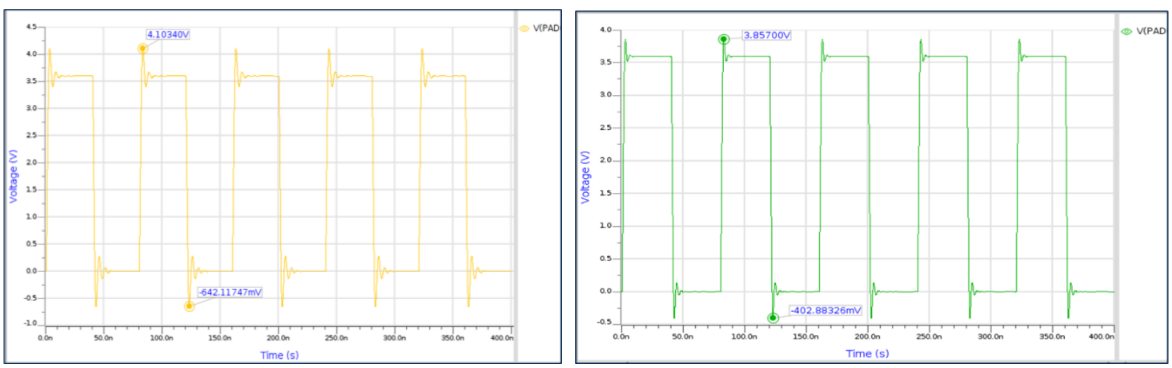

Figure 6. 642mV undershoot observed in IO driver (left) Vs reduced (less than 500mV) undershoot in its lower drive configuration(right).

B. Modelling of Pad noise & ground bounce at SOC, impacting IO Receiver designed for Automotive Product:

Circuit reliability is one of the major challenges for automotive products & each product needs to comply with the given product mission profile. System level Noise, heat-induced electromigration failures, Hot carrier ageing of ICs, Electrical Overstress (EOS) are major concerns seen in automotive chips. In a SOC (system on chip) ICs are prone to noise from various paths. IO receivers are designed to block external noise components which may couple either from pad or through supply/ground pair & DC thresholds i.e., VIH/VIL & hysteresis defines how much noise an IO circuit can block. In 28nm technology it was observed that when we provide toggling input to receiver, falling edge becomes sensitive to noise. On further investigation it was found that this noise generates on board & couples through ground, false triggering at receiver output is observed in presence of pad noise with ground bounce. To model the behavior on CAD lumped parasitics (R=2ohms, L=4nH, C=2pF) were connected at ground terminal & noise is provided in the form of a glitch, on falling edge of receiver input.

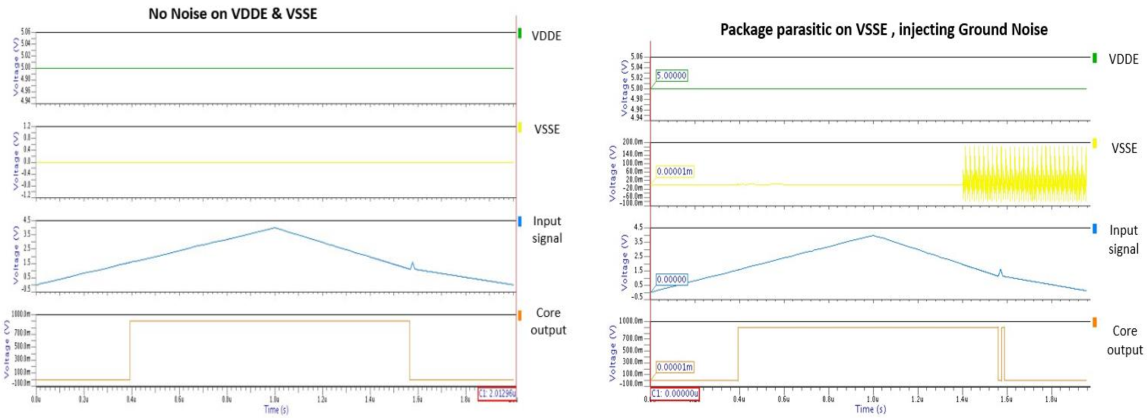

Figure 7. Correct IO receiver toggling when no noise at ground level Vs multiple edge detection due to ground bounce generated at board.

To eliminate this problem from customers SOC it was advised to suppress noise generated at system level, which gets coupled in ground pad resulting in false triggering.

C. Crosstalk behavior of IOs designed for Microcontrollers & Infotainment:

Single ended IOs designed in 28nm technology underwent EMI testing & it was found that crosstalk on adjacent static pin was out of specification. To reflect the behavior on CAD & to propose mitigation of the issue, a setup has been proposed which was closely matching with real testing environment [Fig 9].We observed peaks in the frequency domain plot when two IO transmitters having 0.1pF coupling capacitance in between, interacts with each other (provided one is driving static logic while other is toggling), harmonics seen on CAD were matching with Silicon results. Possible reasons to have peaks in frequency spectrum could be either toggling IO, coupling capacitor or mutual inductance between PAD_PJ0 & PAD_PA15.To identify the root cause following trials have been done. we reflected silicon behavior on CAD using FFT plot feature given inside ezwave (Eldo).

1. Coupling capacitor between toggling pad (PAD_PA15) & static pad (PAD_PJ0) is reduced to 0.05pF from 0.1pF.
2. Drive Configuration of PAD_PA15 has been reduced to slow from very fast mode, using drive control pins.

In both cases spectrum is plotted on PAD_PJ0_1 & there is no change in amplitude of harmonics. It has been observed that IOs were toggling as per expectation in given environment & there was no abnormality in transient toggling which could lead to unwanted peaks in frequency plot i.e., standalone IOs were not contributing to generate harmonics. Same as coupling cap were also not responsible for peaks. From the analysis it was evident that crosstalk mechanism is dependent on-board inductances so minimization only at board level could lead toward acceptable frequency domain plot.

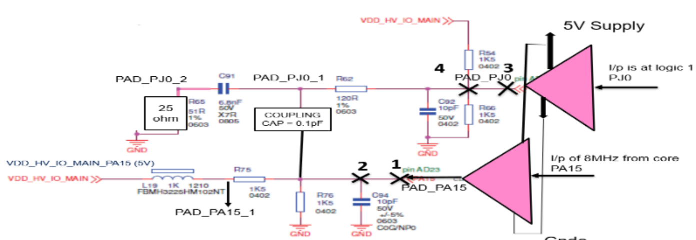

Figure 8: Crosstalk setup

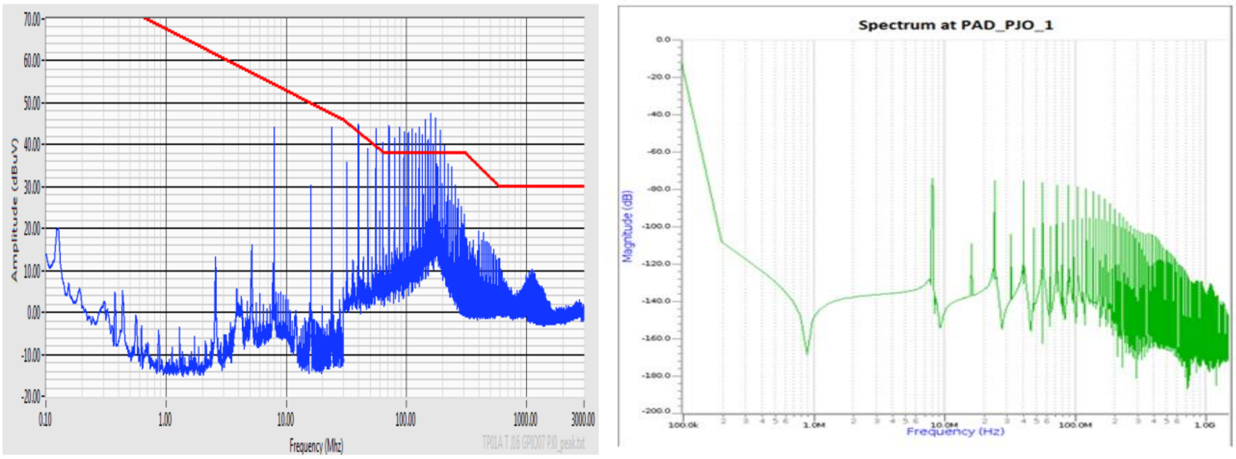

Figure 9. Unwanted peaks observed in silicon testing (left) Vs replication of peak harmonics on CAD (right).

To reduce the amplitude of peaks observed on silicon improved packages with lesser inductive coupling were proposed.

D. Analysis of IO Driver with interconnect traces:

As discussed under Transmission Line Effects in section II we know that Reflection occurs due to mismatch in impedance of IO driver with respect to transmission line. This mismatch causes communication signals of poor quality. Fig 10 shows the setup used for analysis of transmission line with IO transmitter designed in 65nm technology. At far end significant overshoot and undershoot were observed on PAD_FE but when we inserted series impedance of 33ohms on board, signals reflections were attenuated that results in clean output.

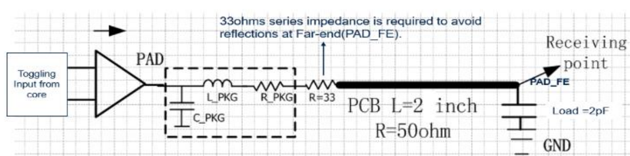

Figure 10: IO transmitter with package parasitics & transmission line, here R_{series}=33ohms inserted at board to avoid reflections.

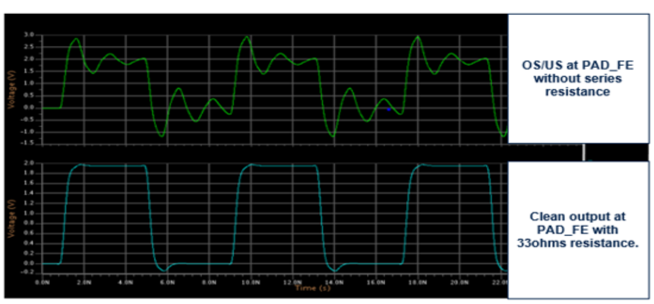

Figure11: Waveform corresponding to setup depicted in Figure 10.

IV. CONCLUSION

In this paper, IPs designed for Automotive/Analog & MEMS /Imaging/Infotainment applications are analyzed against Signal Integrity. The impact of signal integrity on IOs has been demonstrated and apparently the presence of triggering factors like SSN, Crosstalk, Transmission Line Effects & EMI is shown. The causes and mitigation of mentioned factors have been thoroughly explained with the correlation of CAD and real silicon behavior. The risks associated with the measures are also explained. For example, introducing series resistance on board to manage the effect of Transmission Line can lead to increased board cost, which indicates the tradeoff required for final qualification. This paper also illustrates how packages become evidently small in applications such as MEMS, which critically impacts the signal quality. Industrial challenges of signal integrity in different techno's like 130nm, 28nm were presented. The work thus contributes profound comprehension of signal integrity and the exploration of groundwork challenges in real implementation.

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