DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA
Architecture to Analytics A2A
DVCON 2024
September 18-19, 2024 | Radisson Blu, Marathahalli, Bengaluru

Harnessing AI for Enhanced Verification Efficiency

Anika Sunda

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Bio

Anika Sunda is a senior product marketing manager in the Cadence System Verification Group. She has more than 15 years of semiconductor industry experience spanning product management, research development, and verification from prior roles at Synopsys and Agilent Technologies. Sunda is a gold medalist and holds a master's from IIIT Bangalore, India.

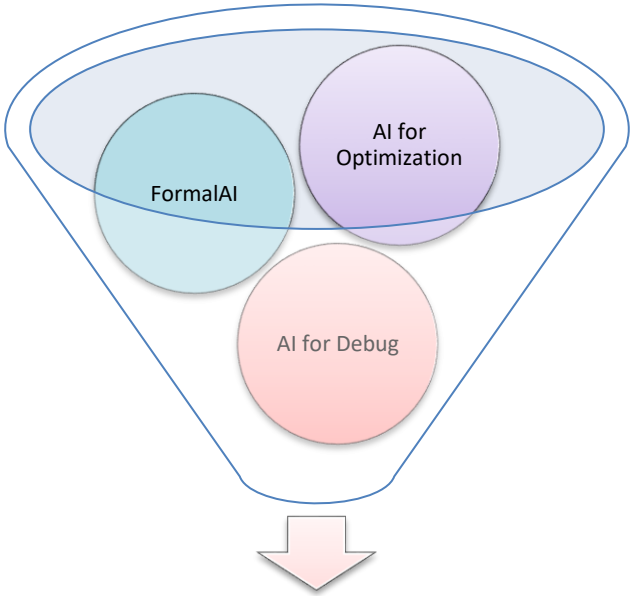
Sundararajan Ananthakrishnan

Application Engineer Architect

Cadence

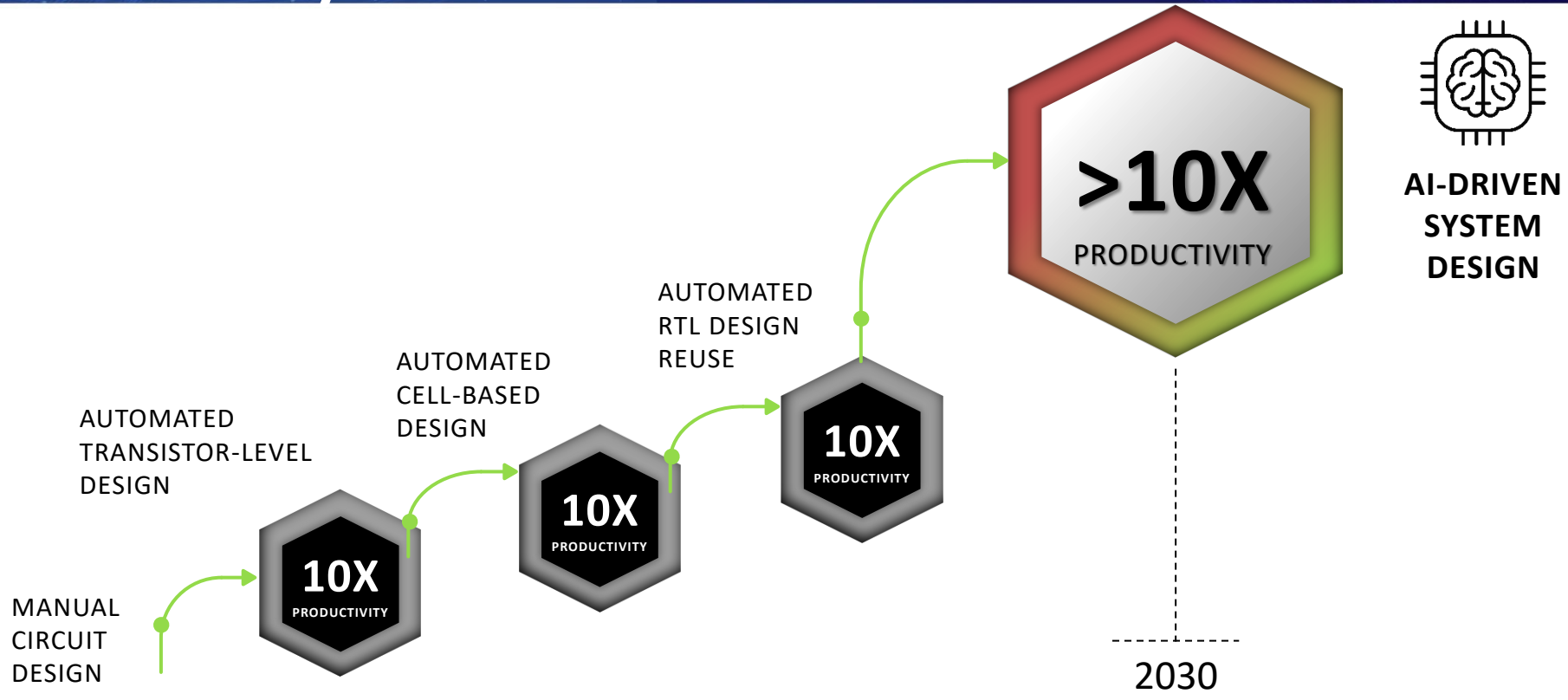
Sundar has been at Cadence for 14+ years, with an overall Experience of 24+ years in the field of SoC & IP Verification. Sundar leads the Cadence Advance Verification Systems field team for India region and drives the Advanced ML/AI and Verification Solutions in the region.

Accelerated Verification Efficiency

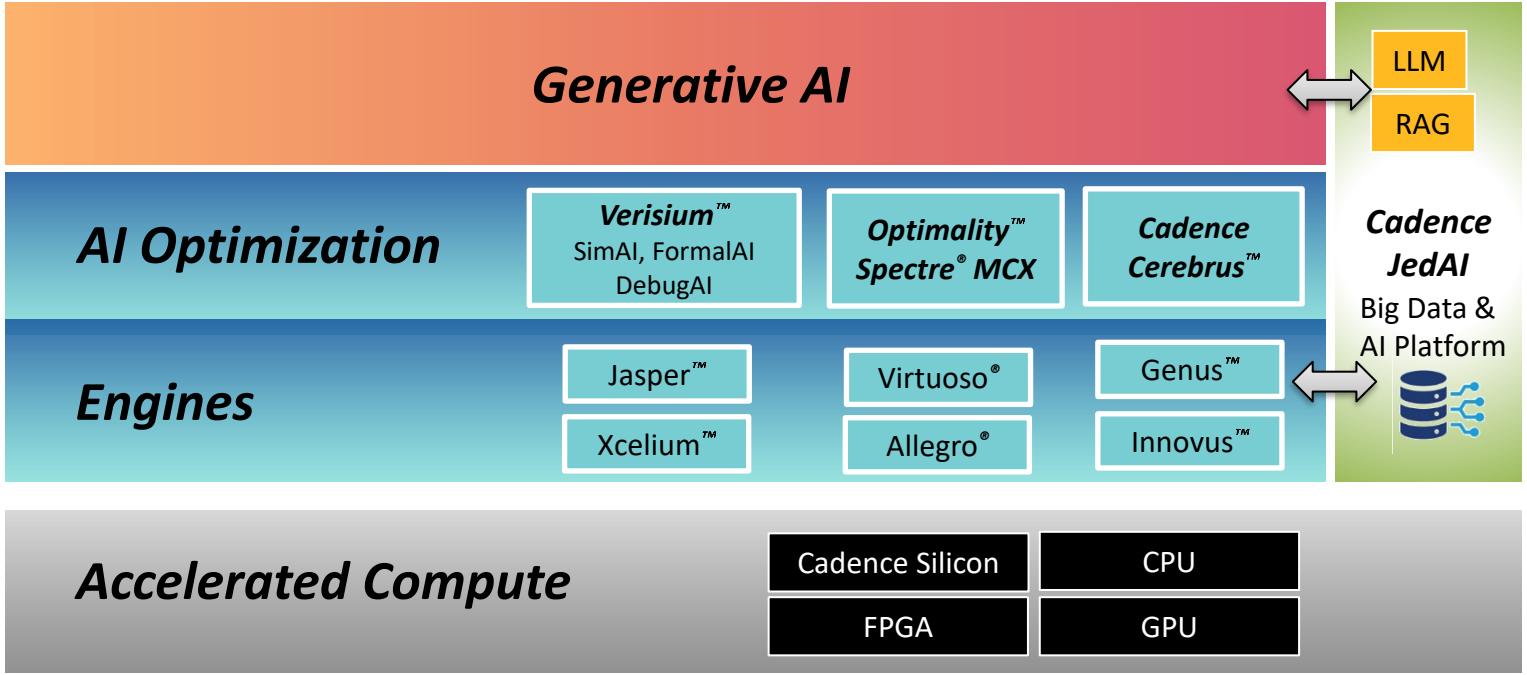


10X Verification Throughput

AI – Accelerating System Design Productivity

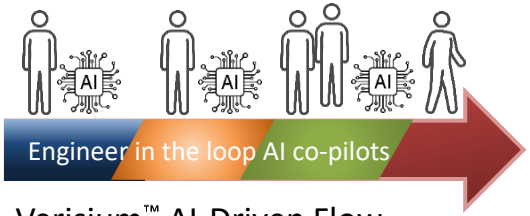


Cadence AI Strategy



Regression Efficiency with Verisium Platform

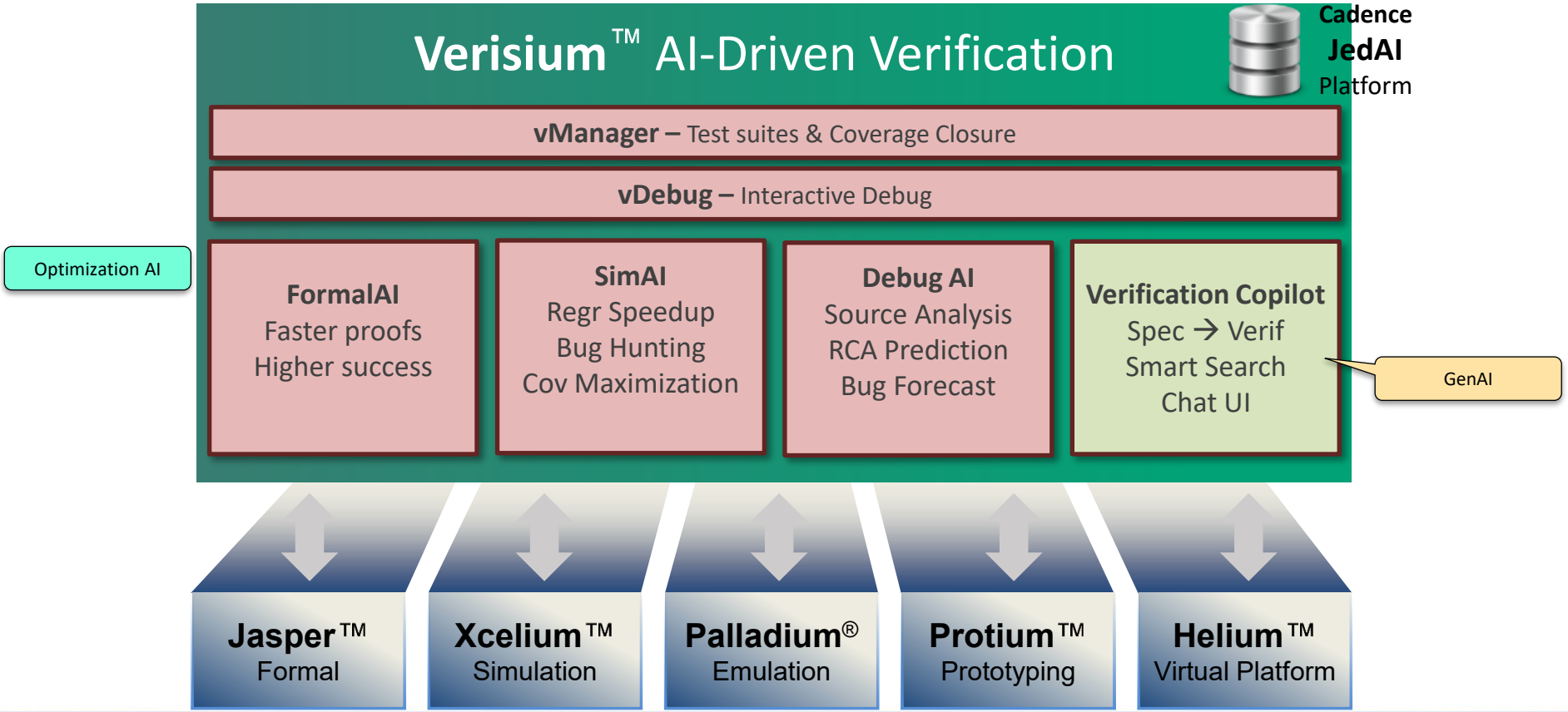
Manual Flow



Verisium™ AI-Driven Flow

Potential for 20X+ improvement in verification productivity

Verisium AI-Driven Verification Platform



Major AI FLOWS FOR VERIFICATION

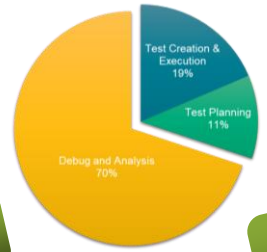
Verisium AI-Driven Debug Apps

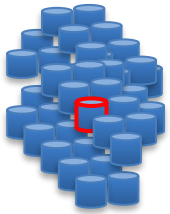
3x reduction post-regression failure triage

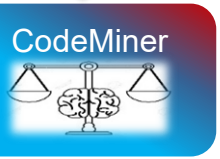
ML-Assisted Failure Triage

6h vs. 1 week to debug 95 failures

ML Bug Prediction



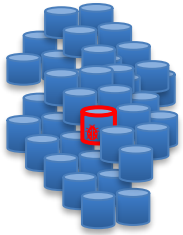




AI source code hot spot analysis

30x faster root cause

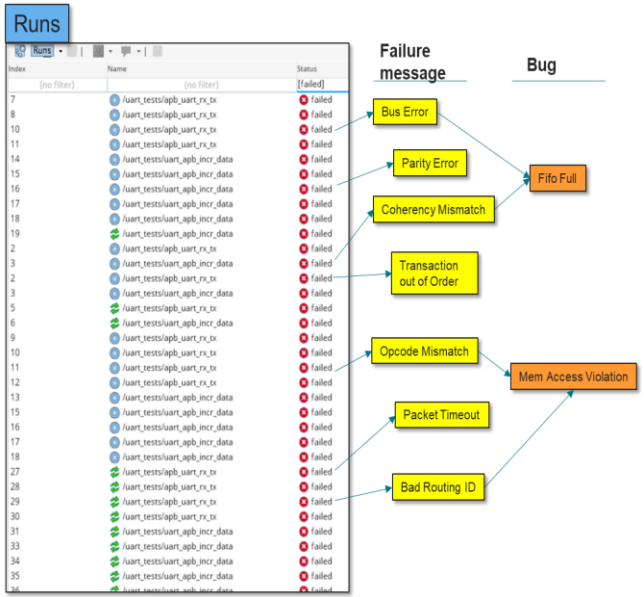
AI Waveform and Root Cause Analysis



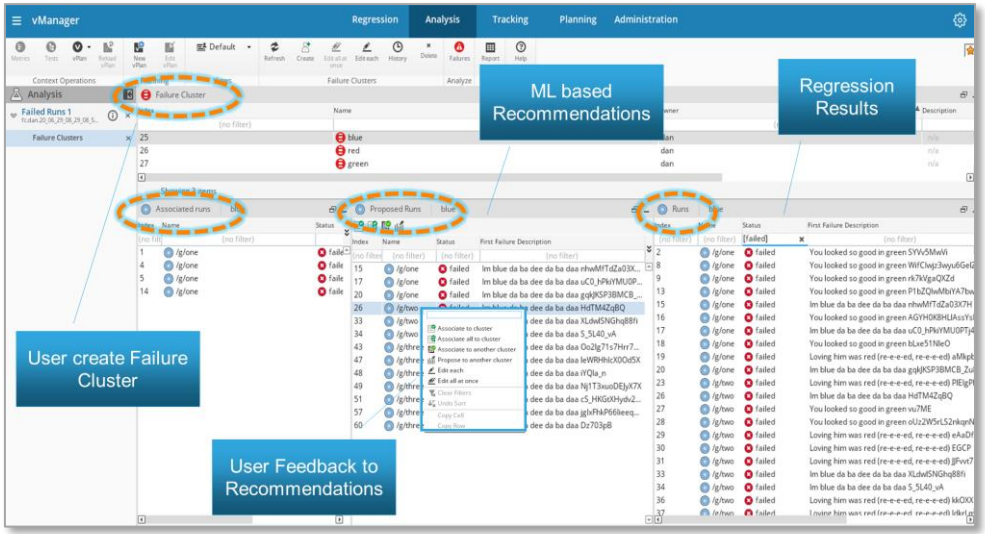
```
signal rst @ T=4324ns
```

AutoTriage – Automated ML Bucketing of Regression Failures

Manual failure analysis of regression is very costly and inefficient.

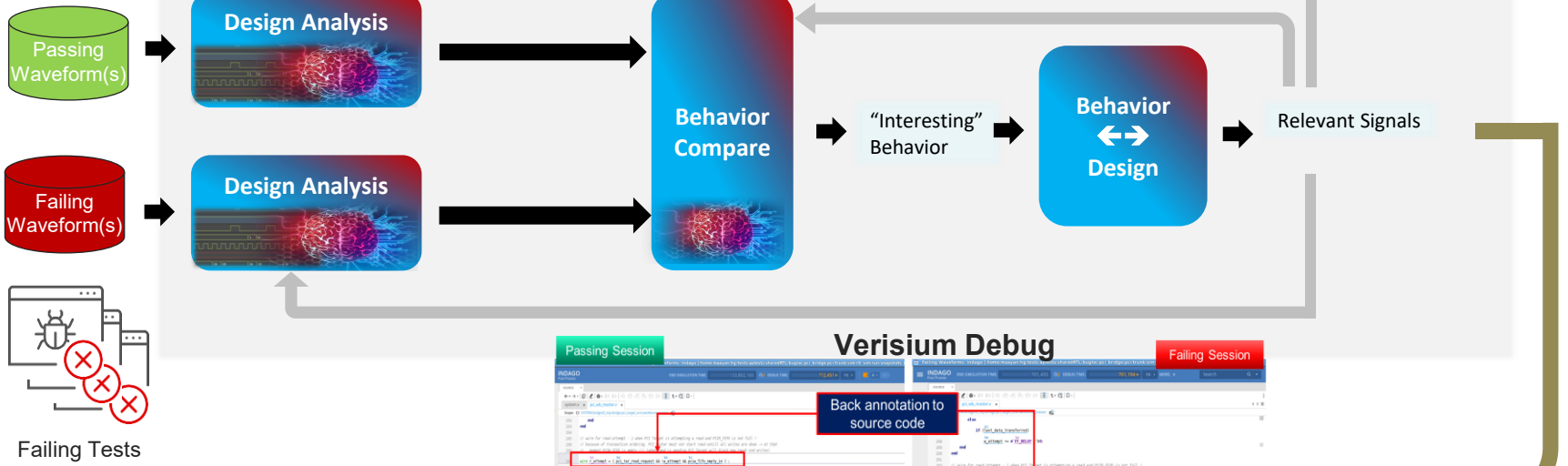


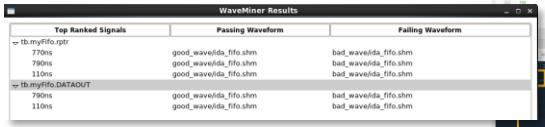
- AutoTriage
  - Automate failure classification using Machine Learning
  - Recognize patterns in any run-based attributes

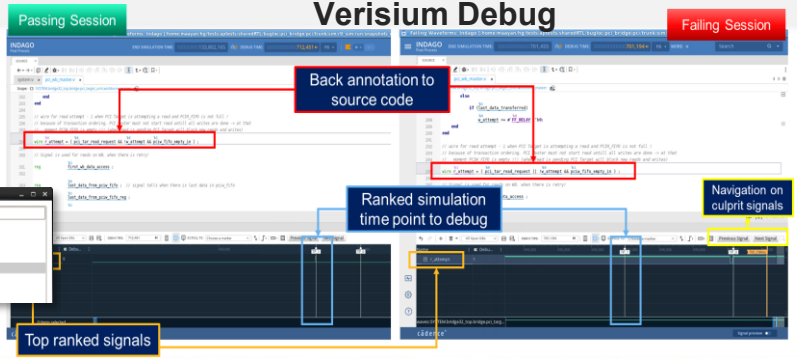


WaveMiner: Smart Waveform Analysis

WaveMiner : Applies powerful AI engines to analyze waveforms from multiple runs and determine which signals, at which times, are most likely to represent the root cause of a test failure.

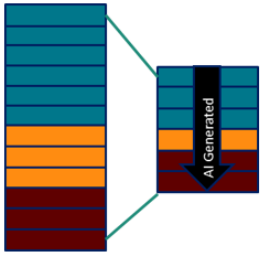






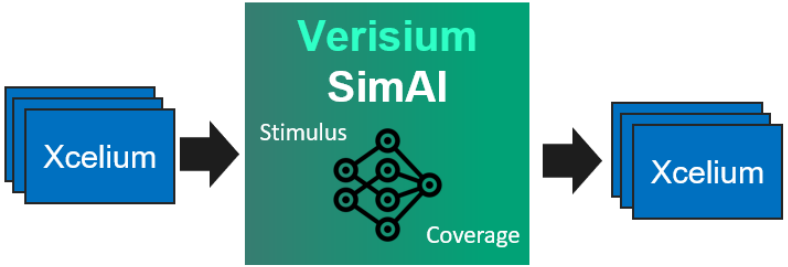
Verisium SimAI

Regression Performance

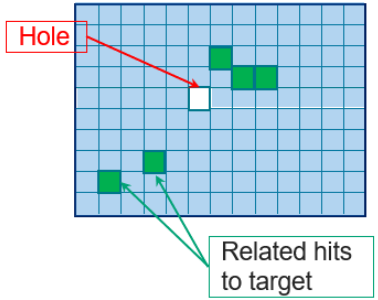


2-6x speed up

AI Optimized Randomization



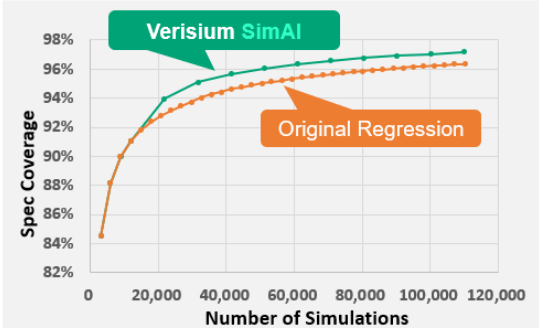
Coverage Maximization



New bins covered 2x fewer sims

Simulation CPU hours	Baseline	Verisium SimAI	Speed-up
IP 1	19	1	19x
IP 2	3,588	597	6.0x
IP 3	12,807	4,396	2.9x
IP 4	26	2	13x
IP 5	3,810	536	7.1x

Qualcomm – “We observe as much as 20x reduction in CPU cycles and find SimAI very useful for hard-to-hit cross coverage bins.”
CadenceLive Silicon Valley 2024



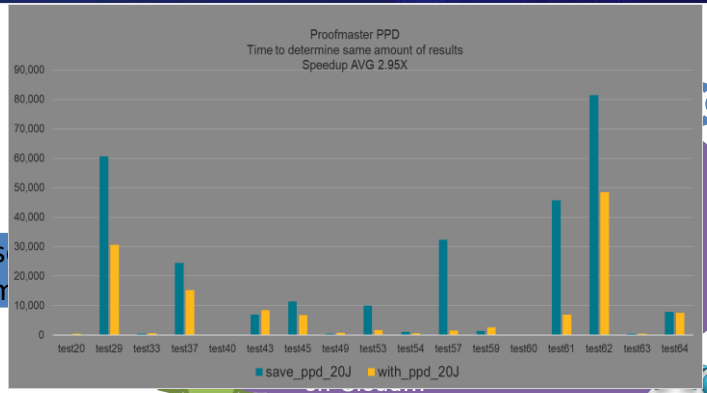
Jasper FormalAI: Robust, Scalable Proof Solutions

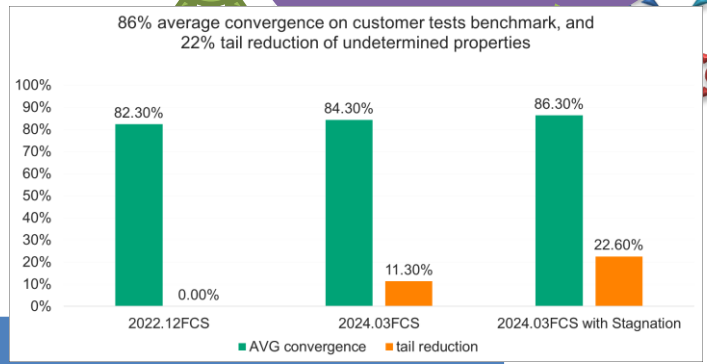
Use cases
- Design bring-up
- Proof/bounds signoff
- Bug hunt/bug fix
- Regression

ML-based use case optimization

ML-based Orchestration
- Stagnation detection
- Prove/hunt integration
- Target bounds learning
- Bounds signoff

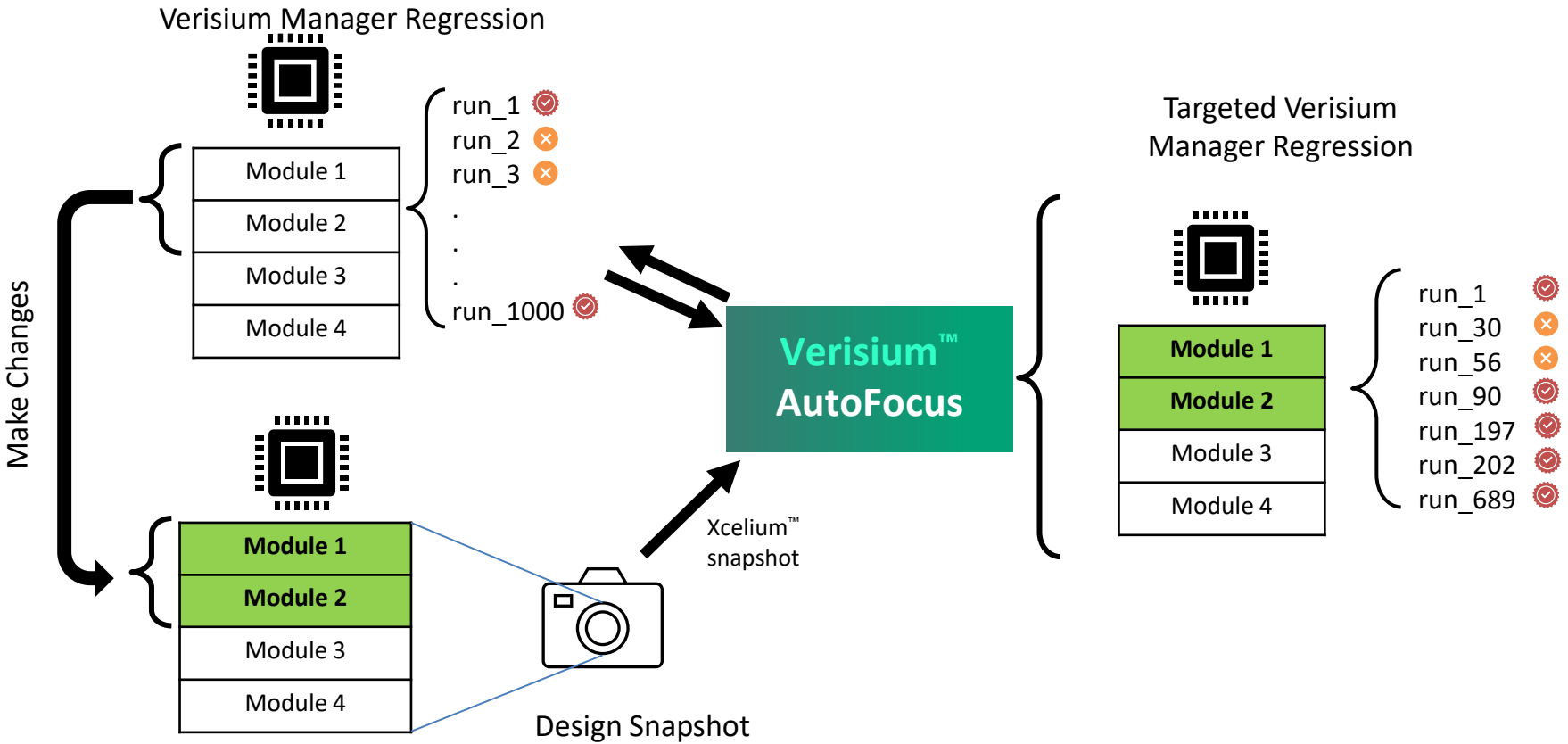
Smart Proof DB





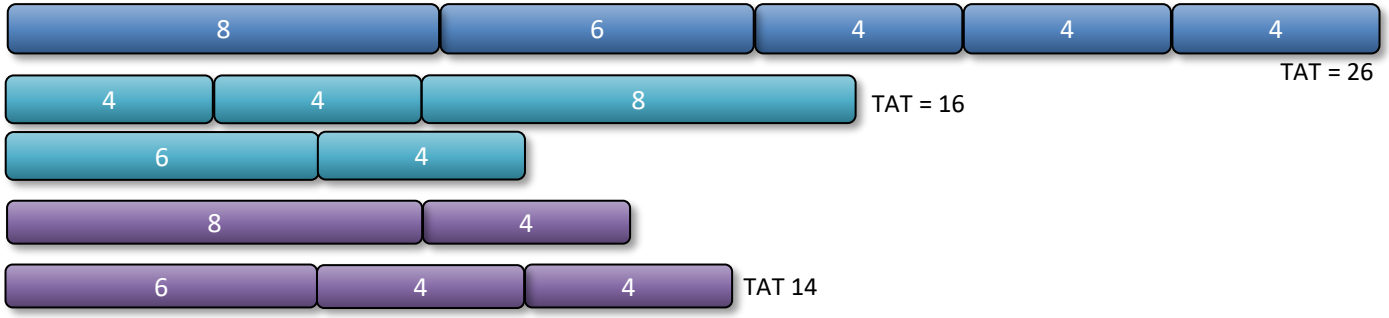
RESOURCE OPTIMIZATION

Verisium AutoFocus - AI Optimized Regression



Verisium SmartRun

- The goal of **Smart Run** is to provide the fastest turnaround time for regression and improve verification throughput
- Flow
  - **Learning** the typical run durations for tests
  - **Reports** that allow the user to decide what queuing policy and farm resources to apply to optimize the regression throughput.
  - **Reshuffle** and launch new regressions using the new queuing policies.



Automotive IP Results
- 40% Faster Total TaT
- 13x smaller farm resource allocation

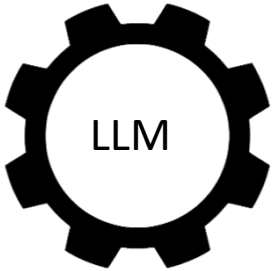
Generative AI for verification

LLM Expectations and Reality

Oh!

Now the magic happens…

Write formal properties for my 3 channel round robin arbiter



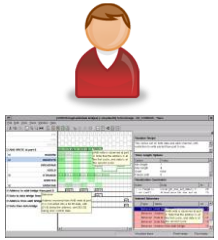
Bot: How can I help you today?

User: Write formal properties for my 3 channel round robin arbiter

Bot: Sure, here's your formal property:

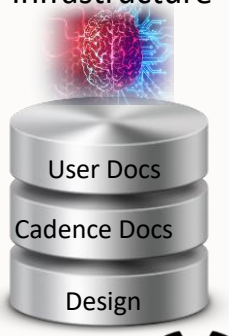
```
// Assert that the arbiter
always grants access to the
next requester in round robin
order
assert property (@(posedge
clk) disable iff (!rstn)
(req0.granted &&
 req1.granted &&
 req2.granted) |=>
req0.granted ##1
req1.granted ##1
req2.granted);
```

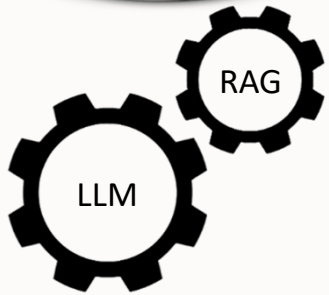
Verisium Copilot Potential



Integrated User Chat

Cadence® JedAI Infrastructure





Follow-up Questions

SpecMiner

'done' must be asserted in the next clock tick of 'clk' after signal 'sent' has asserted

```
assert property
(@(posedge clk)
   $rose(sent) |-> ##1
done));
```

Add to vPlan

Scripting

Create Jasper TCL setup for ['arbiter.v']

```
analyze -sva arbiter.v
elaborate -top arb
clock clk
reset rst
assume ~scan_en
```

Docs search

What is monitor mode in the LPDDR5 VIP?

Monitor mode is…

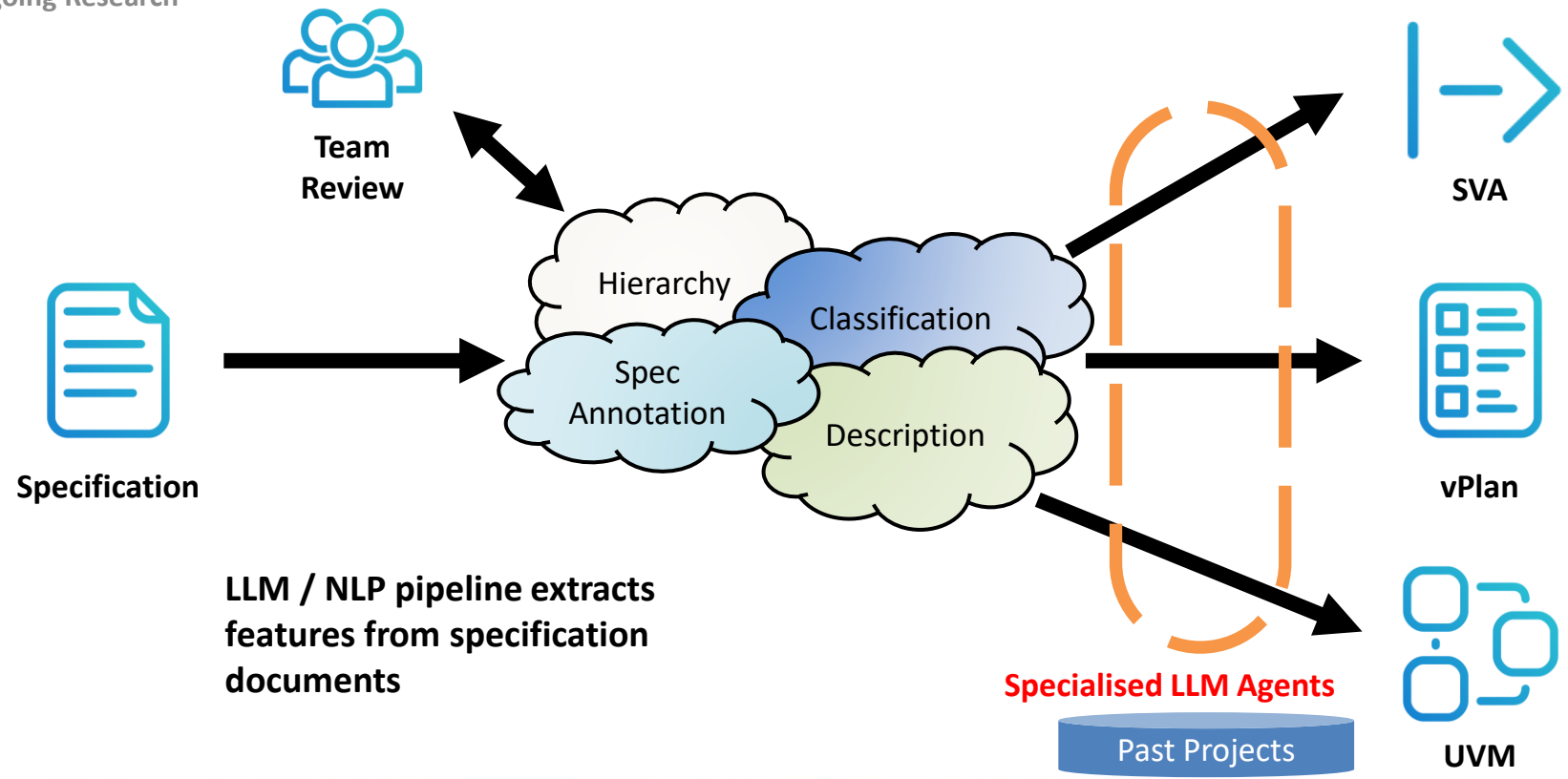
Debug

Find all instances of signal_1 and signal_2 having value 0x10 at the same time.

Activates Verisium Debug and highlight times at which signal_1 and signal_2 have value 0x10.

Verification Co-Pilot - Verisium SpecMiner

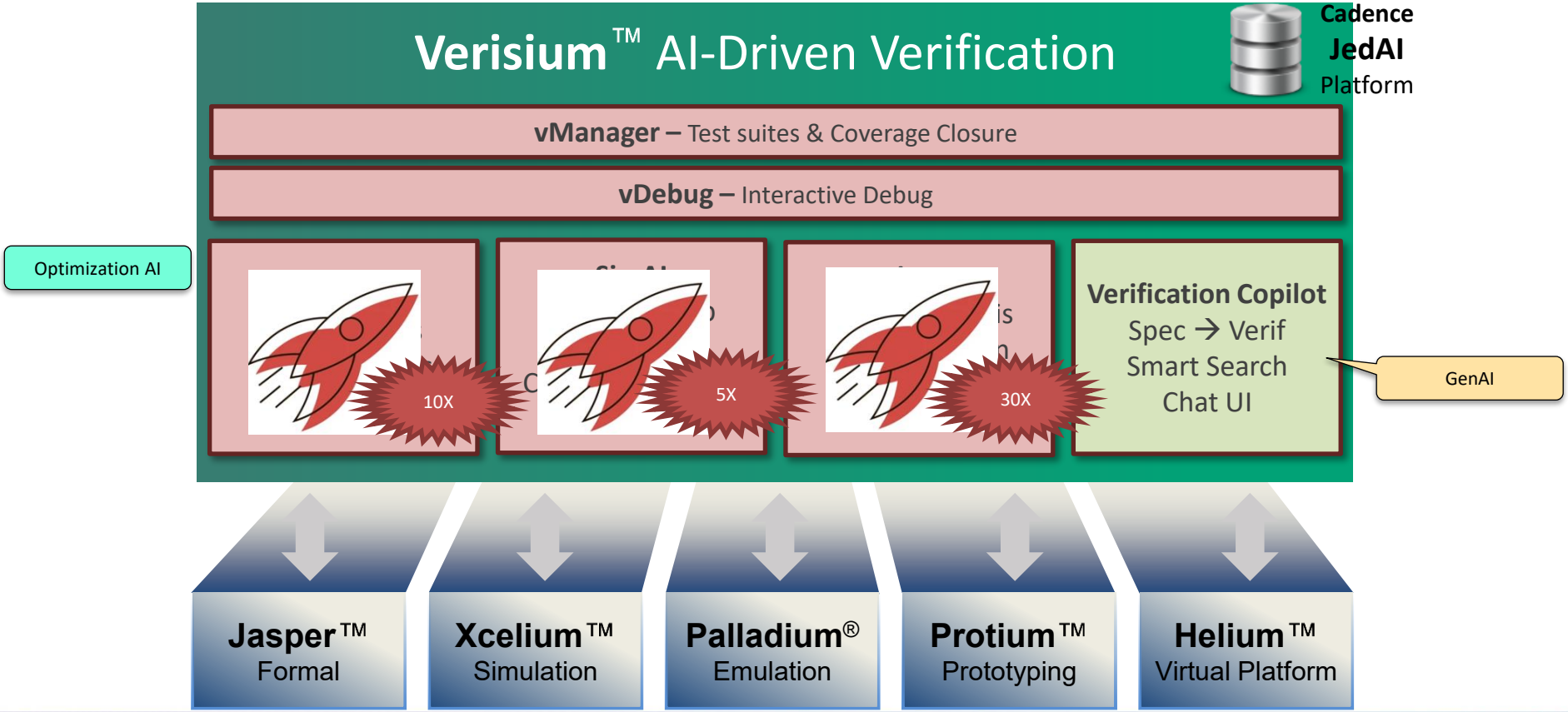
Ongoing Research



LLM / NLP pipeline extracts features from specification documents

SUMMARY

Verisium AI-Driven Verification Platform



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Maximizing Verification Efficiency Using the Synergy of AI & ML

Vivekananda upadyaya P
Sr. Staff enginner/manager
Qualcomm India Private Limited

Verification Challenges

Design Complexity

- Cutting-edge features are being added to improve performance/QoS

Testbench Complexity

- Several Constraint layers with around thousands of random variables
- All operational modes with multiple configuration settings and inherent randomness

Coverage Goals

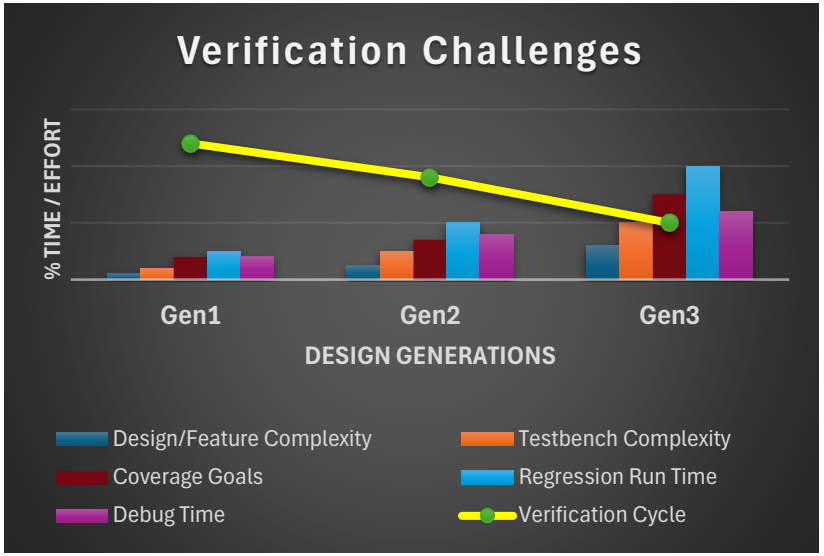
- Millions of coverage bins

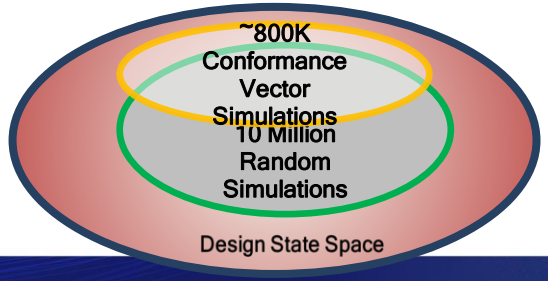
Regression Run & Debug Time

- Millions of random simulations along with 100s of thousands of Conformance suites

Verification Cycle

- Reduction in overall Time-To-Market for VLSI products means similar reduction in overall verification cycle

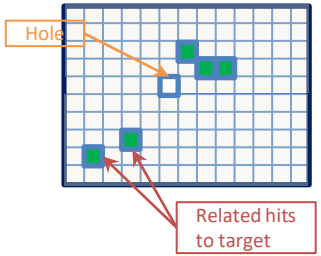




DV Acceleration Using Verisium SimAI Flow

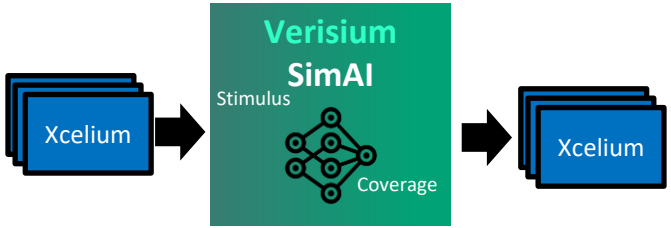
NEW

Coverage Maximization



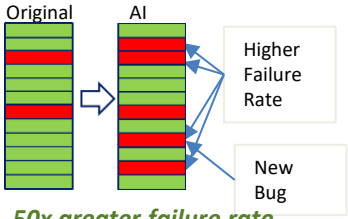
New bins covered
2x fewer sims

AI Randomization Optimization



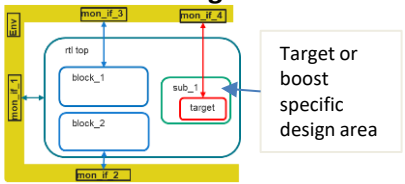
NEW

Cousin Bug Hunting



50x greater failure rate
20% more unique bugs

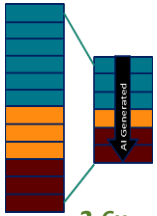
Soak Testing



Target or boost specific design area

5-10x more hits on target vs. random

Regression Compression



2-6x speed up

Regression & Coverage Data using SimAI

Type of Regression	No. of Tests	Bins covered	Total Bins	%Covered	Total CPU(Run) Time
Full Random Regression	950	20139	27439	73.40%	2327.542 hr.
Synthesized regression	288 optimized tests 285/288 passing	19698	27439	71.78%	776.562hr.

CodeMiner Report

Entity Type	Entity Name	Entity golden File/line	Entity new File/line	Mode	Modified lines	Added lines	Deleted lines	Total lines	Diff count	Total count	Rank
Library Item	t1	./pkg.sv(22)	./pkgn.sv(22)	Modified	0	17	0	35	105	500	2
Interface	b	./interface.sv(19)	./interfacen.sv(19)	Modified	0	2	2	18	4	60	4
Module	n	./arb.sv(34)	./arbn.sv(34)	Modified	2	0	0	28	12	110	3
Module	topb	./top.sv(21)	./topn.sv(21)	Modified	3	215	225	316	559	793	1

Conclusion

Simulation Efficiency

- Reduced **randomization time by 15x** & memory consumption by 2x
- Regression runs reduced by **2.5x**
- Compute resources usage reduced by **2x**

Debugging

- Debugging the testbench issues has become very easy and avoids lot of time wastage to check them instead the whole focus is now on RTL debugging and bug hunting

Coverage

- Coverage maximization using SimAI has helped to exercise coverage holes that have never been exercised
- Soak testing feature of SimAI focusing on a portion of the design helps in covering rare scenarios

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