



Harnessing AI for Next-Gen EDA

Trends, Tools, and Technological Advancements

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This presentation contains forward-looking statements based on current expectations or beliefs, as well as a number of preliminary assumptions about future events that are subject to factors and uncertainties that could cause our actual results to differ materially from those expectations or results described in the forward-looking statements. You are cautioned not to put undue reliance on these forward-looking statements, which are not a guarantee of future performance and are subject to a number of risks, uncertainties and other factors, many of which are outside Cadence's control.

Cadence Intelligent System Design



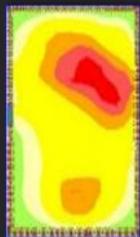
Designing Data Centers with Computational Software

Analyze and Optimize Thermal from Chips to the Data Center

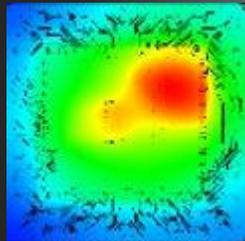
Celsius™ Thermal Solver

Electronics cooling (CFD*)

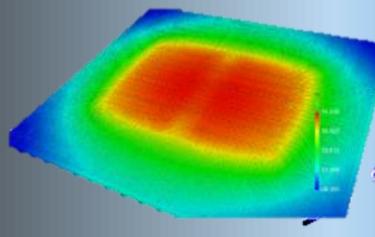
future facilities
6Sigma - Virtualizes the data center and ecosystem as a 3D digital twin



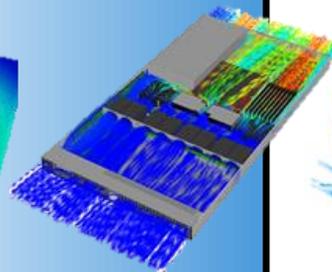
Chip



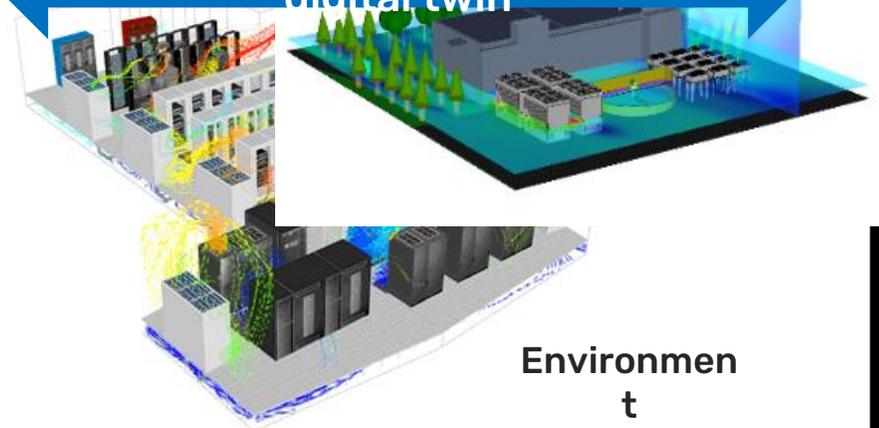
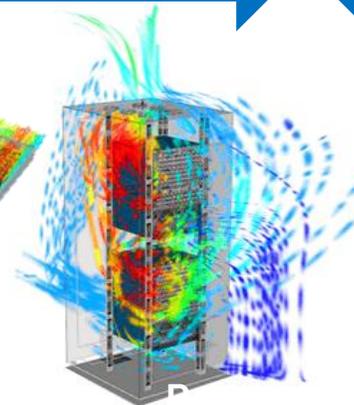
Package



PCB

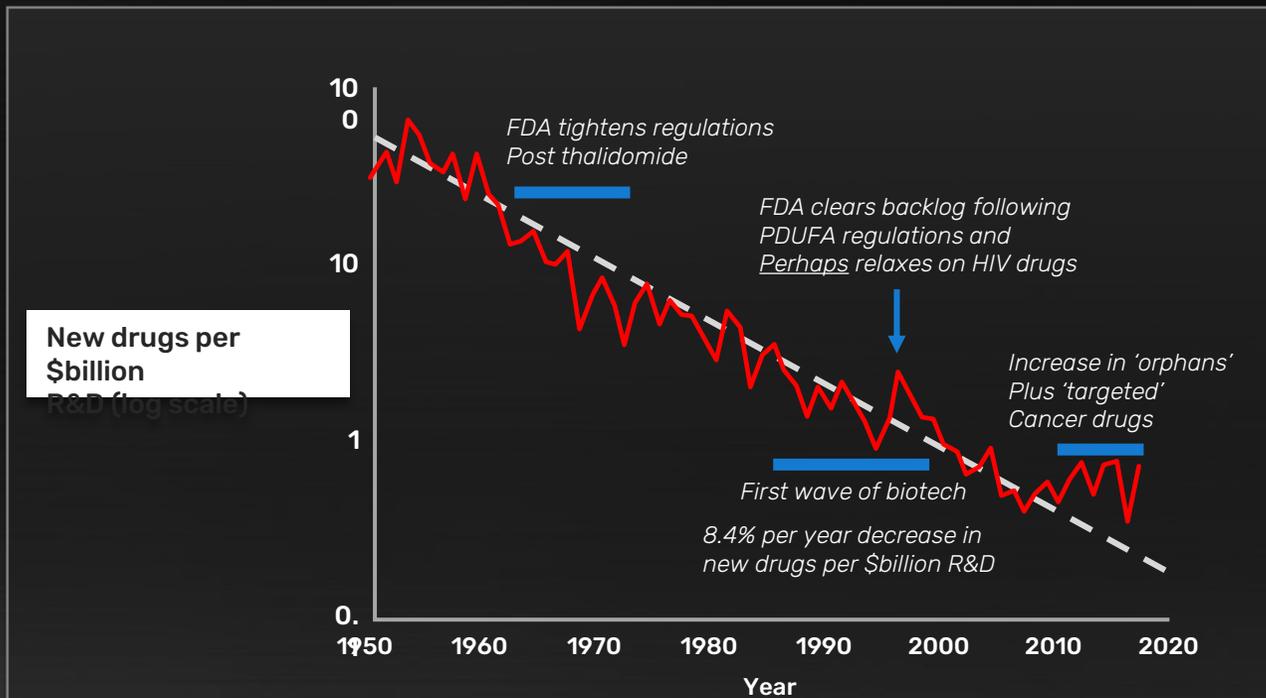


Blade



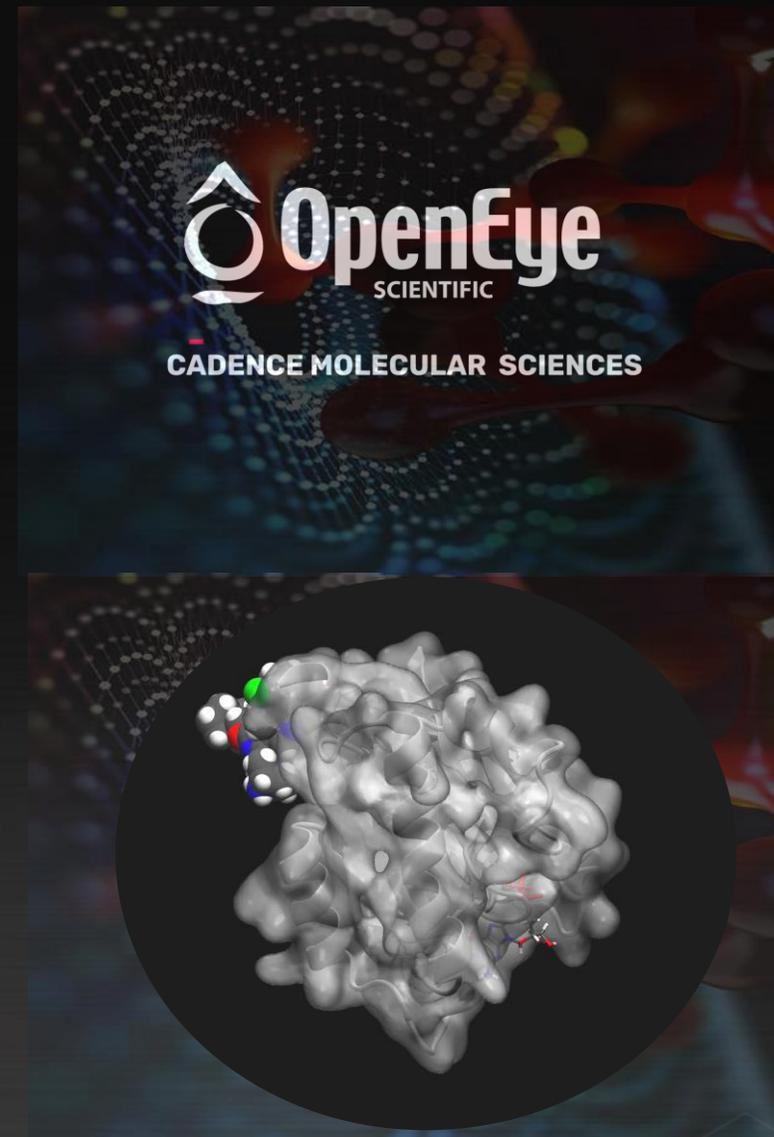
Environment

Drug Discovery with Computation Software



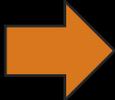
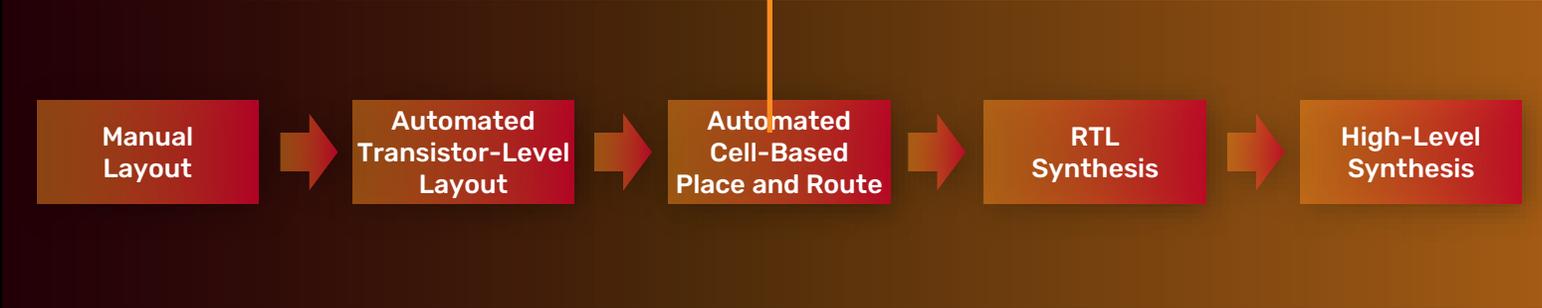
Source: Diagnosing the decline in pharmaceutical R&D efficiency, Nature Reviews Drug Discovery, 2012

Number of FDA approved new molecules per US\$bn global R&D spend has halved every 9 years



AI Opportunity in EDA

40 years of methodology innovations in design abstraction



A new generation of task abstraction tools



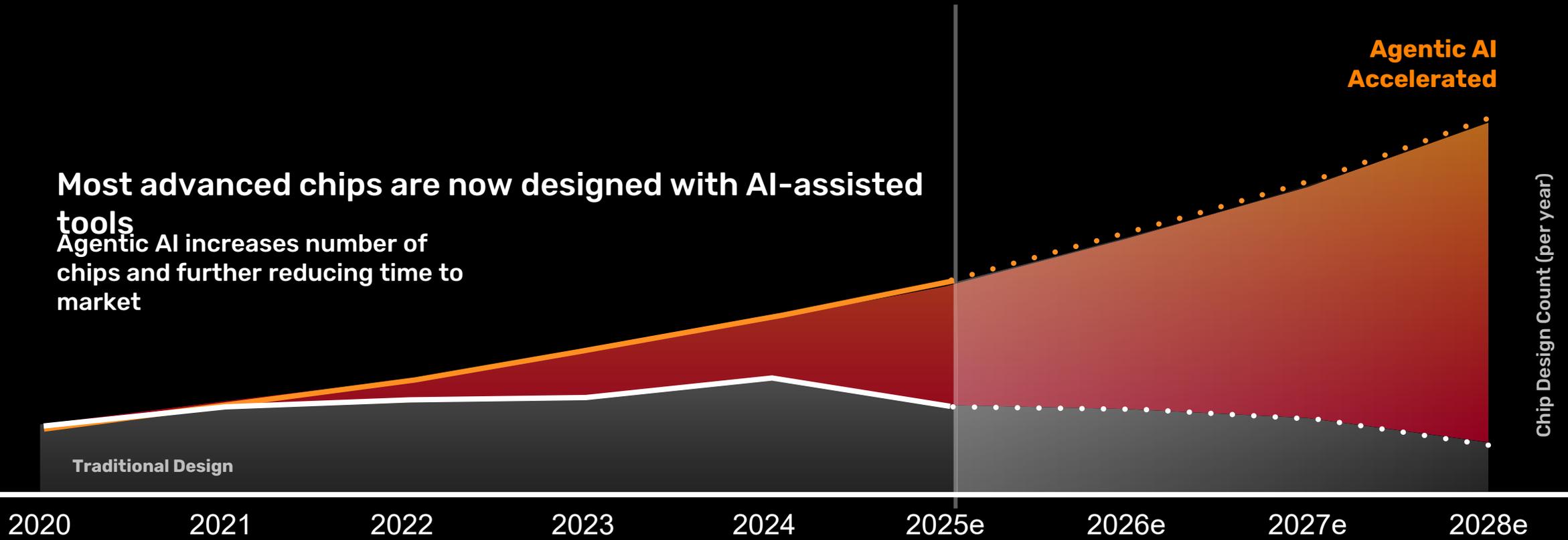
40 years of algorithmic innovations in simulation and optimization



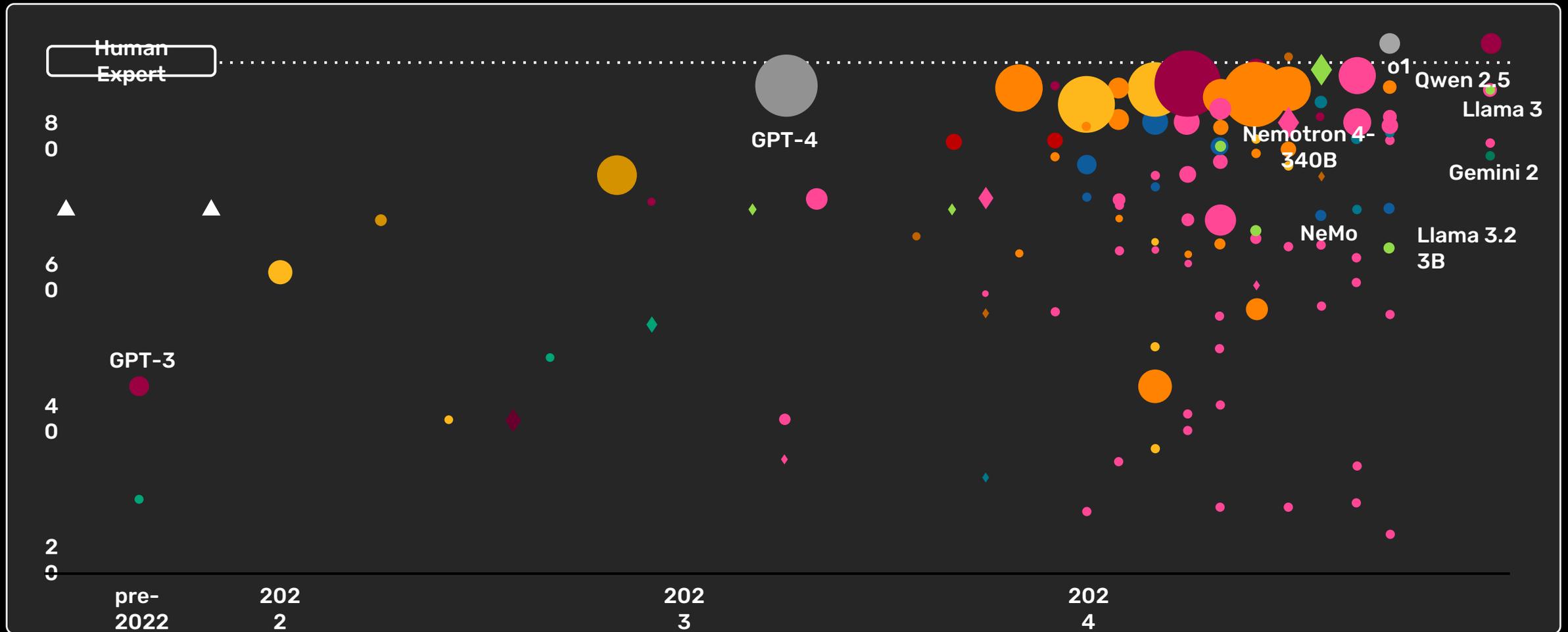
A new leap forward in QOR and performance



AI-Driven Chip Design Inflection Point

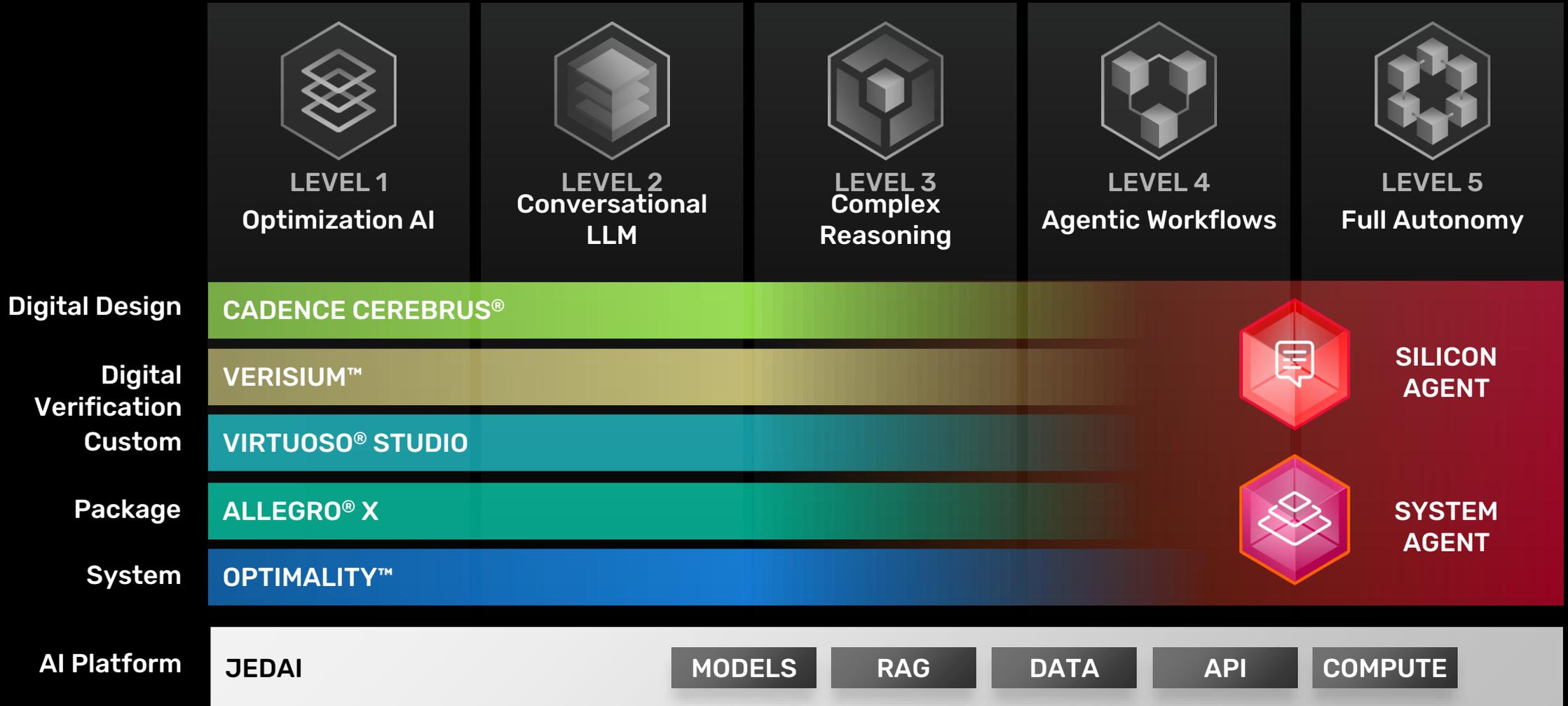


A New Age of Fuel Efficient Models

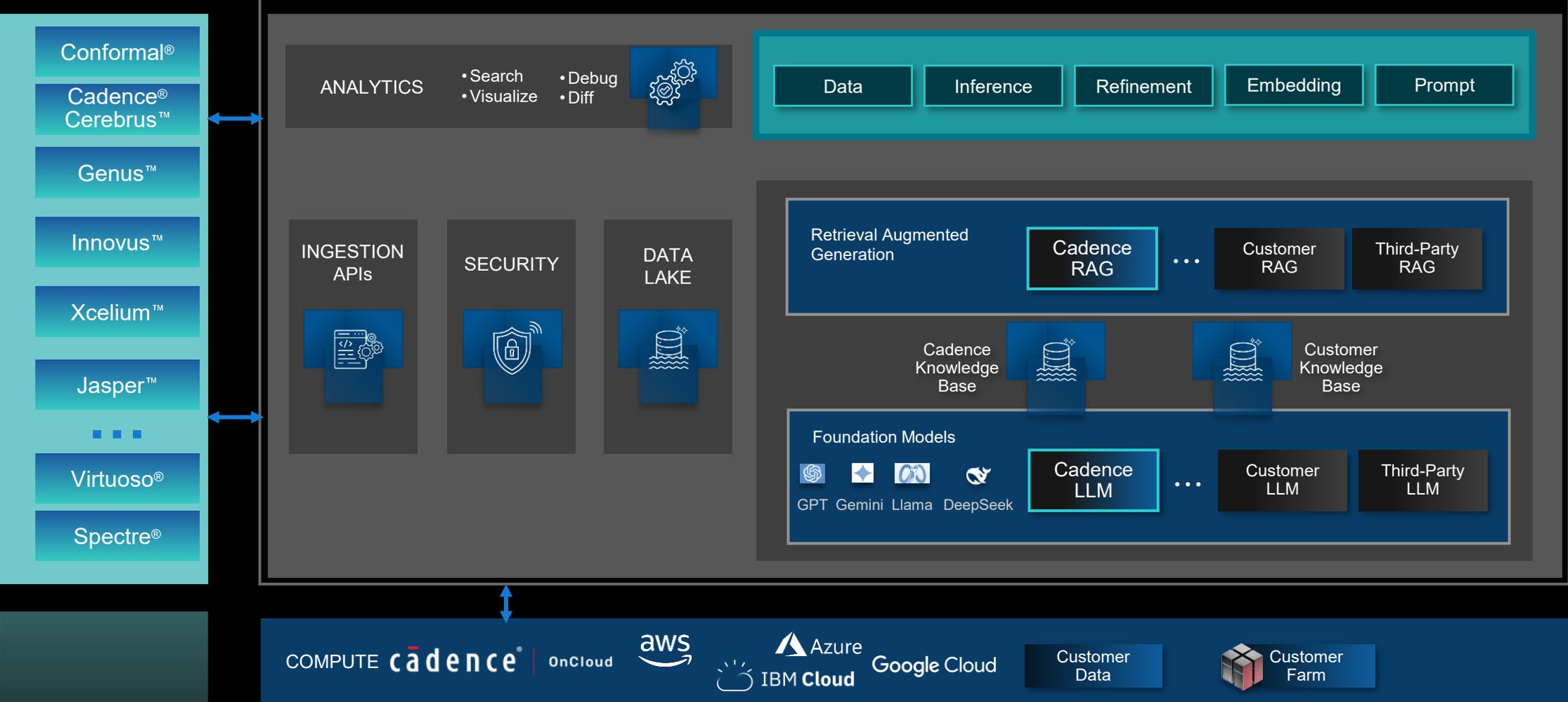


Source: <https://labelyourdata.com/articles/llm-model-size>

The Journey to Autonomous Design



Cadence JedAI Platform



Optimization AI in Digital Implementation with Cadence Cerebrus

cādence.ai

Chips-to-systems intelligent design acceleration

Optimization AI

Cadence®

OPTIMIZATION AGENTS

Cerebrus™

Digital Design

750

Successful design tapeouts

AI-Driven Power, Performance, Area Optimization

AI-ENHANCED DESIGN ENGINES

Genus™

Innovus™

Tempus™

Stratus™ HLS

PPA-optimized chips and chiplets



Customer	Node	Productivity	PPA
Foundry	4nm	5X	8% leakage
Mobile	4nm	5X	10% leakage
HPC	6nm	5X	20% PPA
Foundry	5nm	5X	14% FmaX
Automotive	7nm	5X	8% power
HPC	5nm	5X	15% power
CPU Core	N12	4X	13% PPA
AI	5nm	4X	25% power
Image Sensor	40nm	15X	5% PPA
Mobile	3nm	5X	10% power
Automotive	5nm	5X	6% power
Automotive	28nm	5X	15% leakage

Optimization AI in Digital Verification with Verisium SimAI

cādence.ai

Chips-to-systems intelligent design acceleration

Optimization AI

Cadence®

OPTIMIZATION AGENTS

Verisium™ SimAI

Debug and Verification

10X

Verification productivity

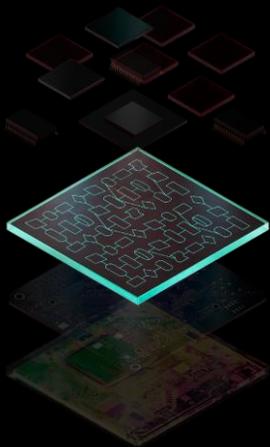
AI-driven automation and analysis for digital chip verification

AI-ENHANCED DESIGN ENGINES

Jasper™

Xcelium™

Bug-free designs



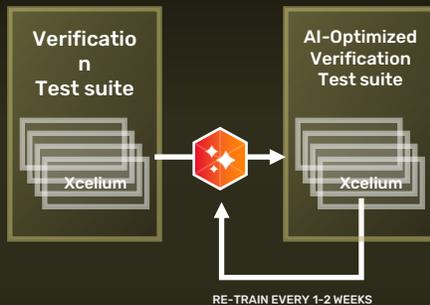
Design Type	Speedup
Modem IP	20X
Mobile SoC	7X
AI IP	8X
AI IP	3X
Memory IP	5X
Base Station	18X
NOC IP	5X
Automotive SoC	5X
CPU IP	3X
Network IP	4X
CPU IP	9X



Verisium™

AI-driven digital verification delivers orders of magnitude speedup

AI-Optimized Simulation



SPEEDUP

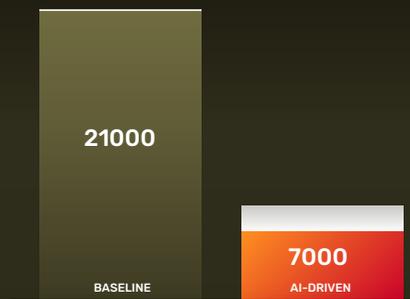
20x
Modem IP

8x
AI IP

9x
CPU IP

AI-Driven Bug Hunting

REGRESSION RUNS



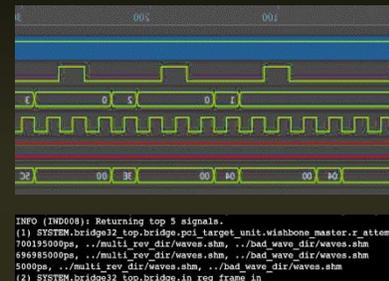
IMPROVEMENT

6x
Faster TAT

40x
Less CPUs

7
New bugs found

AI-Driven Root Cause Analysis



SPEEDUP

30x
Memory Controller IP

6x
Automotive SoC

10x
Mobile SoC

Optimization AI in Jasper

Parallel runs find more bugs and achieve deeper proofs



Jasper Smart Proof AI-Driven Orchestration

Proof Profiling Data

- Keep engine-level settings that worked before

Proof Caching

- Reuse the existing result if the constraints and COI are unchanged

Trace Replay

- Leverage previously found traces

Proof Orchestration

- Use Machine Learning to find the best proof algorithm settings

Multi-run optimization

+AI



Find more bugs



Better convergence



Faster proofs

Qualcomm CPU JUG 2023 Best

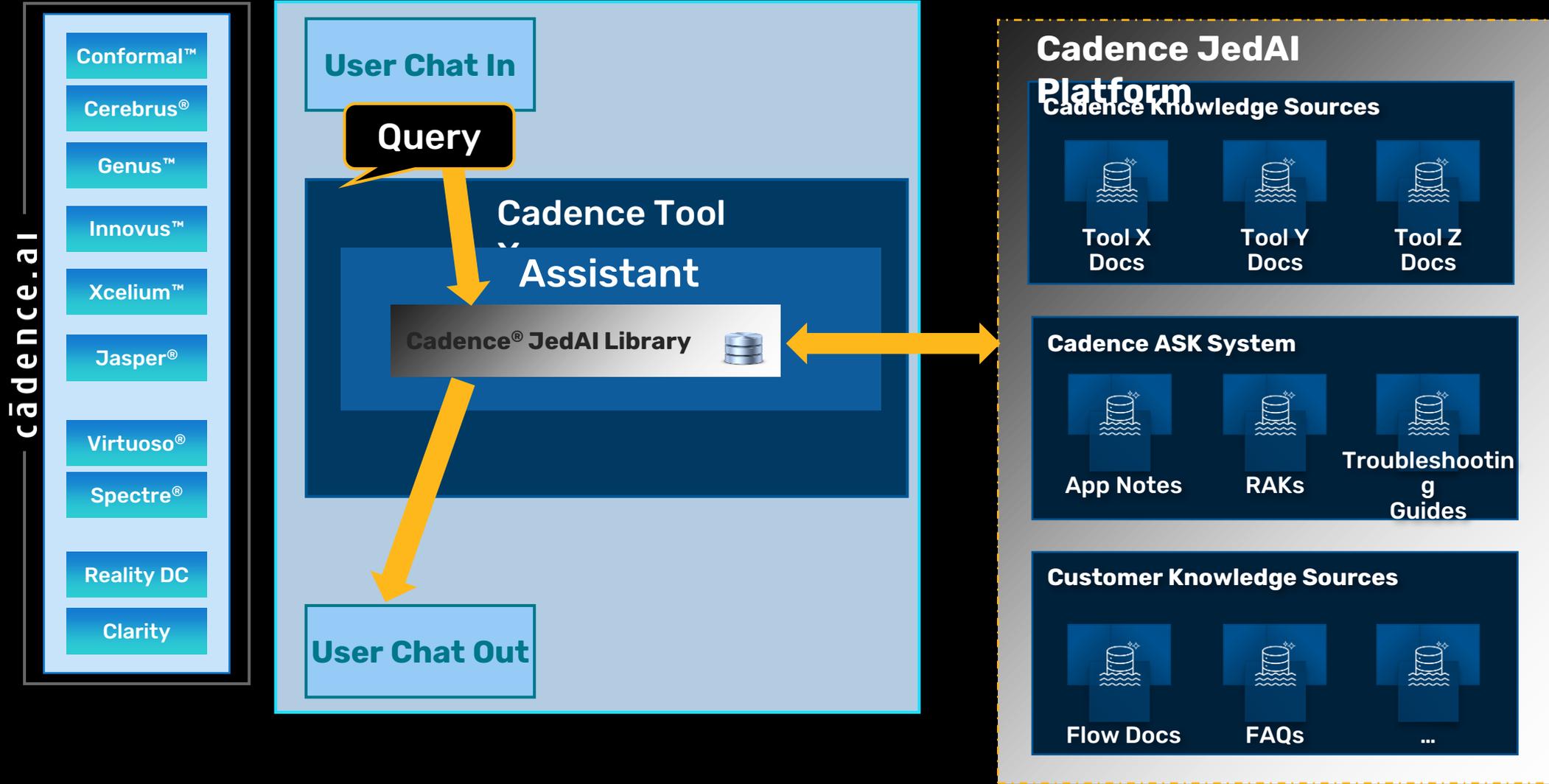


- For fully-converging testcases:
- 5x reduction in runtime
 - 90x reduction in machine slots

Conversational LLM Agents Across the Software Portfolio



LEVEL 2
Conversational LLM



Allegro X Assistant: SKILL Coding Agent



LEVEL 2
Conversational LLM

Allegro Enterprise PCB Designer: Cadence_Demo.brd Project: C:/share/pcb/examples/board_design

File Edit View Add Display Setup Shape Logic Place FlowPlan Route Analyze Manufacture RF-PCB Tools Help

Design Workflow Start Page Cadence_Demo

load('C:/EINROOTDIR/test_skill1')
Function andGetTotalNetLength
redefined
t
andGetTotalNetLength0
19649.87

SKILL >

Allegro SKILL Coding Agent

Enter your query:

Write SKILL code to get the total length of nets in the design?

Progress:

Starting query processing...
Generating draft code (Please wait)...
Draft code generated successfully...
Correcting for API usage: Trial 1...

Final Candidate:

```
***skill  
; Get the total length of nets in the design  
procedure(axiGetTotalNetLength()  
let((totalLength netList)  
; Get the list of nets in the design  
netList = axiGetDesign()->nets  
  
; Initialize total length to 0  
totalLength = 0  
  
; Iterate over each net in the design  
foreach(net netList  
  
; Add the length of this net to the total length  
totalLength = totalLength + axiGetLength(net)  
  
)  
  
; Return the total length of all nets in the design  
totalLength  
  
)  
...  
}
```

Query processing complete!

Jasper Knowledge Agent



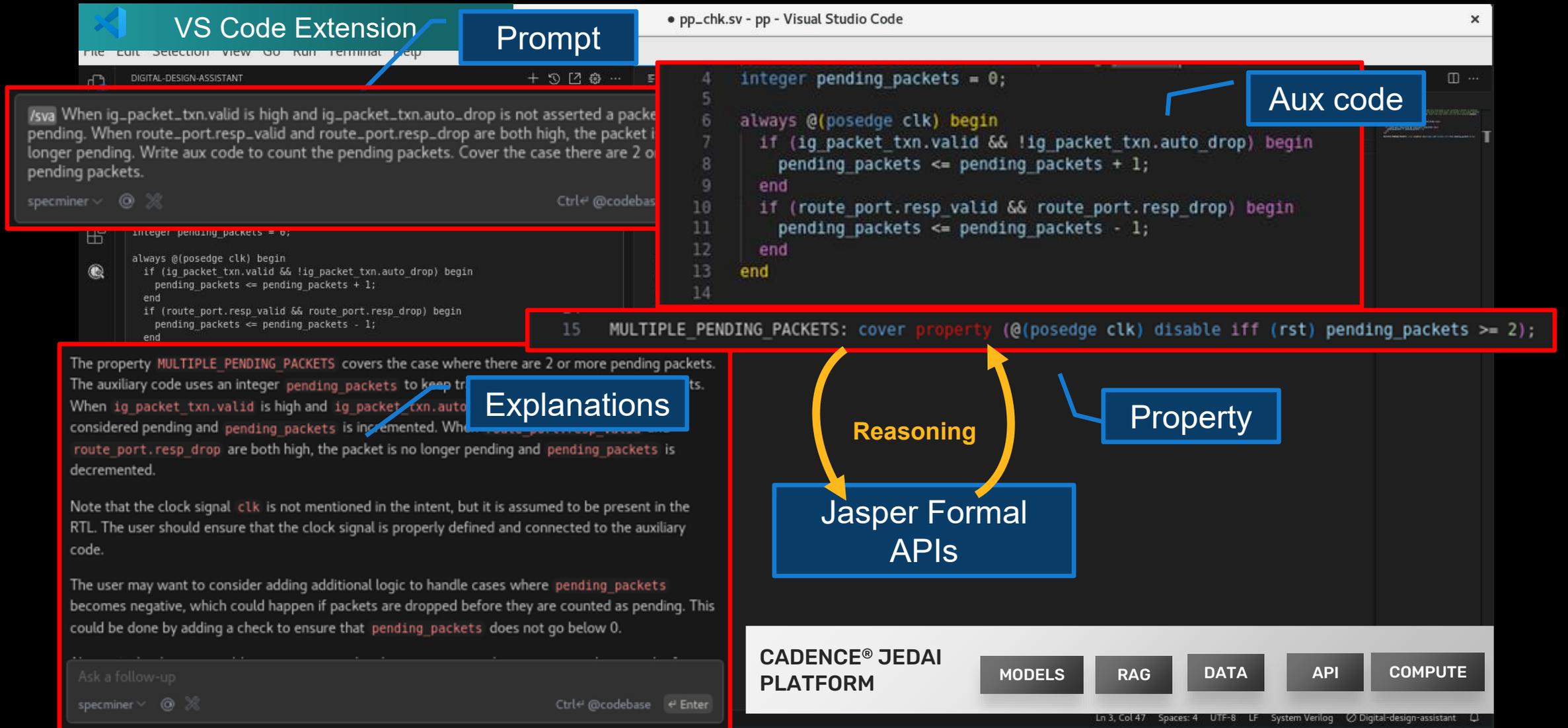
LEVEL 2
Conversational LLM

The screenshot displays the Jasper Knowledge Agent interface within a formal verification tool. The interface is divided into several sections:

- Design Hierarchy:** A tree view showing the structure of the design, including components like `ig_parse`, `route_ctrl`, `payload_mem`, `thr_mem`, `stall`, `drop_ctrl`, `list_ctrl`, and `cfa`.
- Property Table:** A table listing properties with columns for Type, Name, Engine, Bound, Traces, and Time. The table shows several properties related to memory and simultaneous writes.
- Console:** A text area displaying various messages, including warnings (e.g., `[WARN (VDB-1013)]`, `[WARN (VERI-1209)]`) and information (e.g., `INFO (INL208): Elaboration synthesis summary:`).
- Chat Window (JedAI):** A conversational interface where a user asks questions. The chat shows a user asking "What is debug handoff?" and receiving a detailed response. The response explains that Debug Handoff is an extension to Jasper@ Visualize™ that supports sharing debugging sessions across teams. It also lists the Tcl commands for sharing a database for a property: `debug_handoff -config database database_name` and `debug_handoff -save -property property_name`.

- ✓ Basic doc search and straightforward command querying from NL
- ✓ Connection to Cadence or customer-provided LLM via JedAI
- ✓ Open queries to streamline general routines
- ✓ History
- ✓ Future integration with JedAI Library to enable ASK and customer knowledge sources

VS Code Extension: Example SVA and Aux Code Gen



Prompt

```
/sva When ig_packet_txn.valid is high and ig_packet_txn.auto_drop is not asserted, a packet is considered pending. When route_port.resp_valid and route_port.resp_drop are both high, the packet is no longer pending. Write aux code to count the pending packets. Cover the case there are 2 or more pending packets.
```

Aux code

```
integer pending_packets = 0;
always @(posedge clk) begin
  if (ig_packet_txn.valid && !ig_packet_txn.auto_drop) begin
    pending_packets <= pending_packets + 1;
  end
  if (route_port.resp_valid && route_port.resp_drop) begin
    pending_packets <= pending_packets - 1;
  end
end
```

Property

```
15 MULTIPLE_PENDING_PACKETS: cover property (@(posedge clk) disable iff (rst) pending_packets >= 2);
```

Explanations

The property MULTIPLE_PENDING_PACKETS covers the case where there are 2 or more pending packets. The auxiliary code uses an integer pending_packets to keep track of the number of pending packets. When ig_packet_txn.valid is high and ig_packet_txn.auto_drop is not asserted, the packet is considered pending and pending_packets is incremented. When route_port.resp_valid and route_port.resp_drop are both high, the packet is no longer pending and pending_packets is decremented.

Note that the clock signal clk is not mentioned in the intent, but it is assumed to be present in the RTL. The user should ensure that the clock signal is properly defined and connected to the auxiliary code.

The user may want to consider adding additional logic to handle cases where pending_packets becomes negative, which could happen if packets are dropped before they are counted as pending. This could be done by adding a check to ensure that pending_packets does not go below 0.

Reasoning

Jasper Formal APIs

CADENCE® JEDAI PLATFORM

MODELS RAG DATA API COMPUTE

This slide contains forward-looking statements regarding Cadence's business or products. Actual results may differ materially from the information presented here.

Agentic AI in Verisium UI – Verification Plan Gen



LEVEL 3
Complex Reasoning

1
SpecMiner proposes vPlan sections

2
User selects suggestions that are relevant, accepts to vPlan

3
User selections recorded and used to improve future iterations



CADENCE Cerebrus[®] AI Studio

Agentic AI digital design implementation platform

Accelerated Design Closure

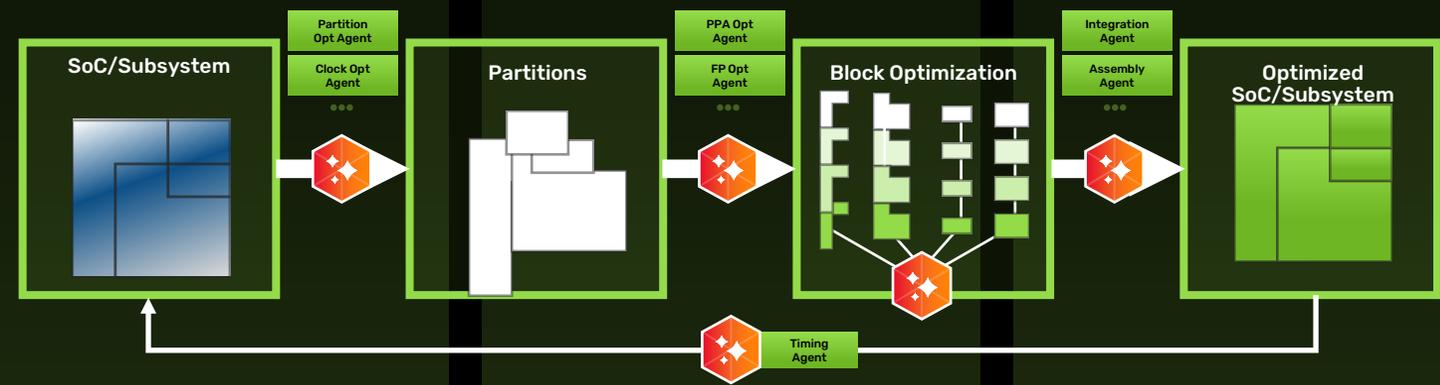
Integrated design platform
Advanced data analytics for faster debug
Smart model selection for faster optimization

Breakthrough Productivity

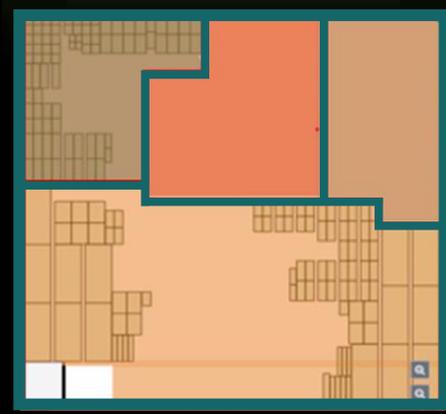
Engineer workload parallelization
Accumulated learning over time
Powerful design dashboard

Unparalleled PPA

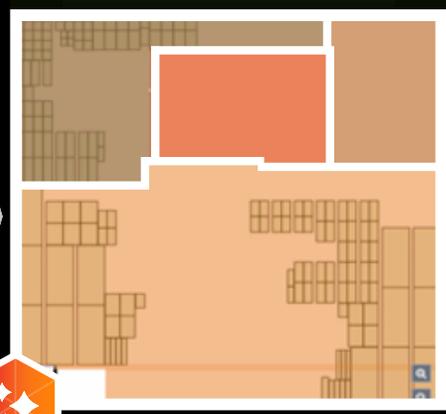
Agentic AI workflows
Top-block co-optimization
Hierarchical design closure



3 Months



1 Month



30%	Improvement in Timing
10%	Improvement in Power
1%	Improvement in Density

Advanced CPU Core 3.3M Instances
5nm



UP TO **70%**
Productivity Improvement

130nm → 55nm
4nm → 3nm

Legacy and Advanced Nodes

Defense HPC AI Power
communications Imaging Aerospace

Broad Production Adoption

Suite of AI Agents

Virtuoso® Studio

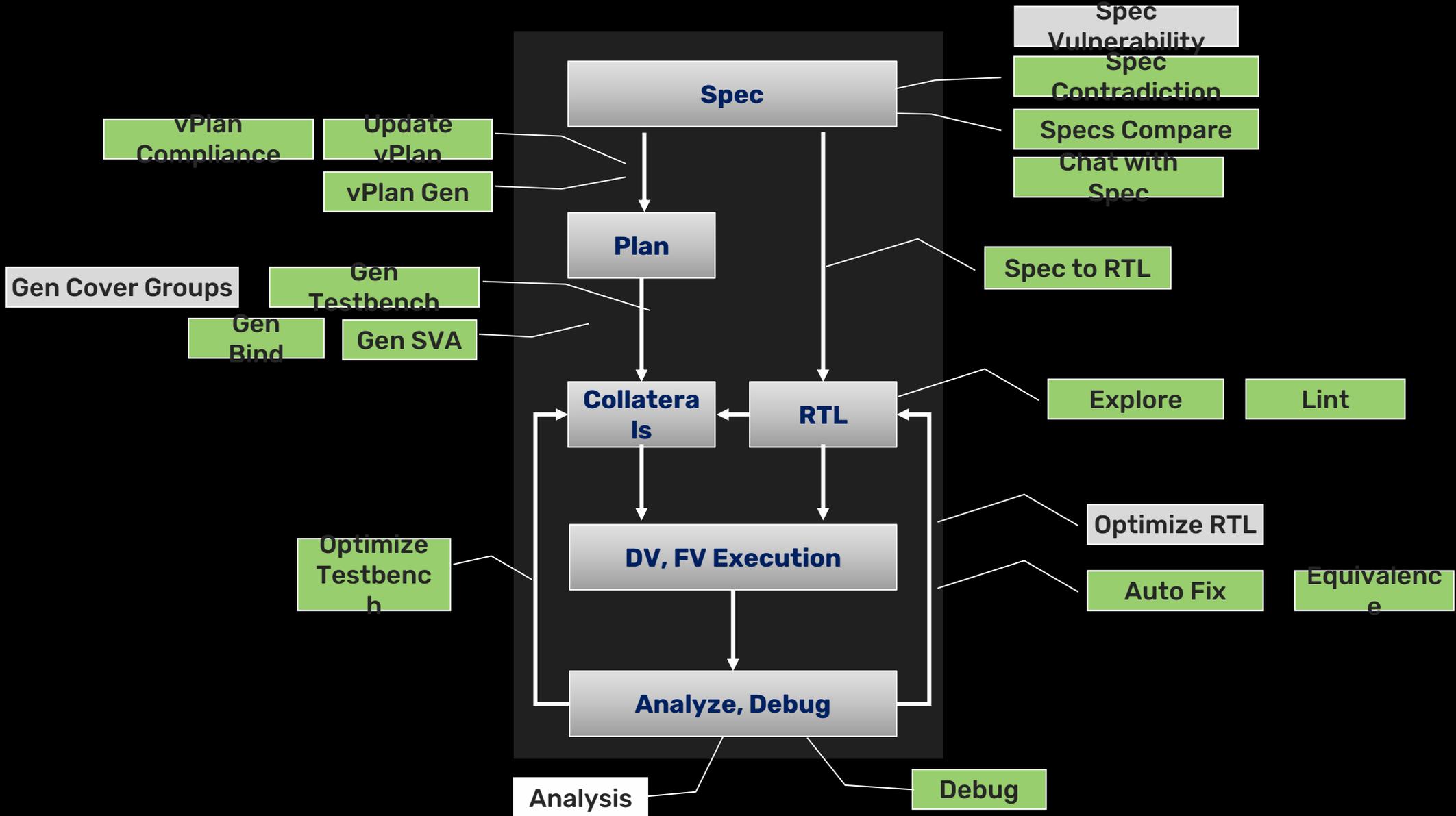
Agentic AI enables custom design migration



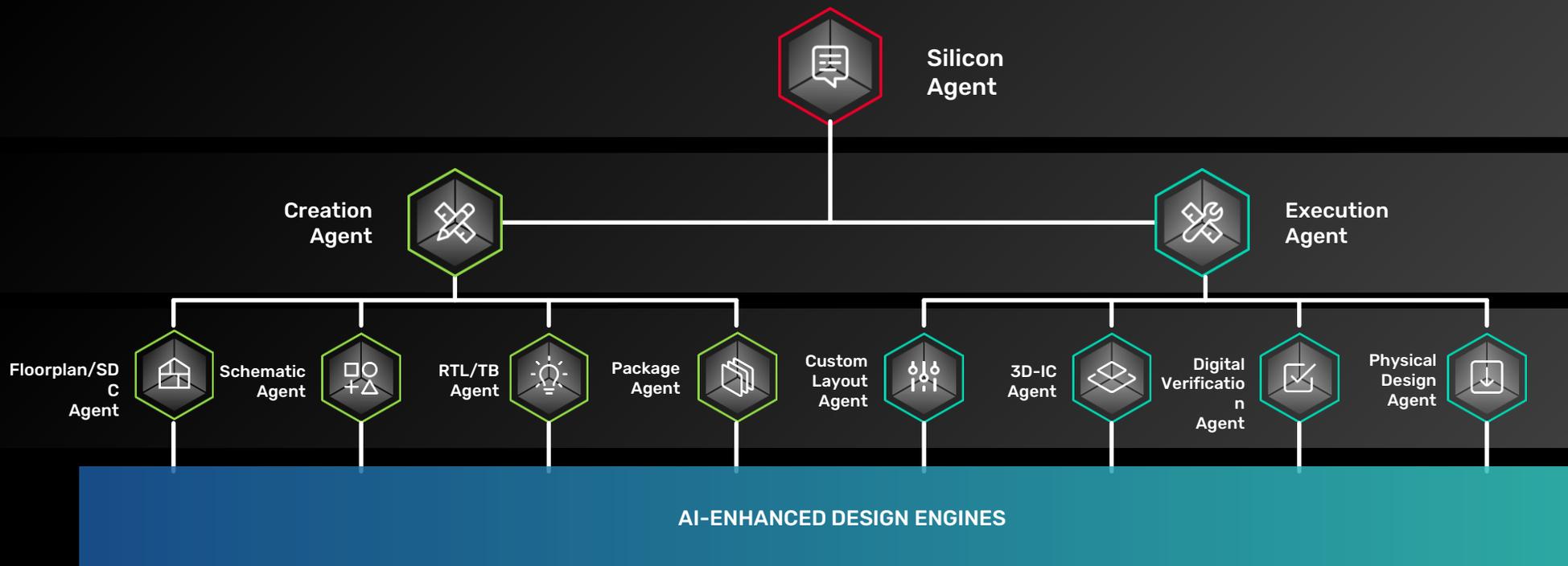
Custom Design Migration



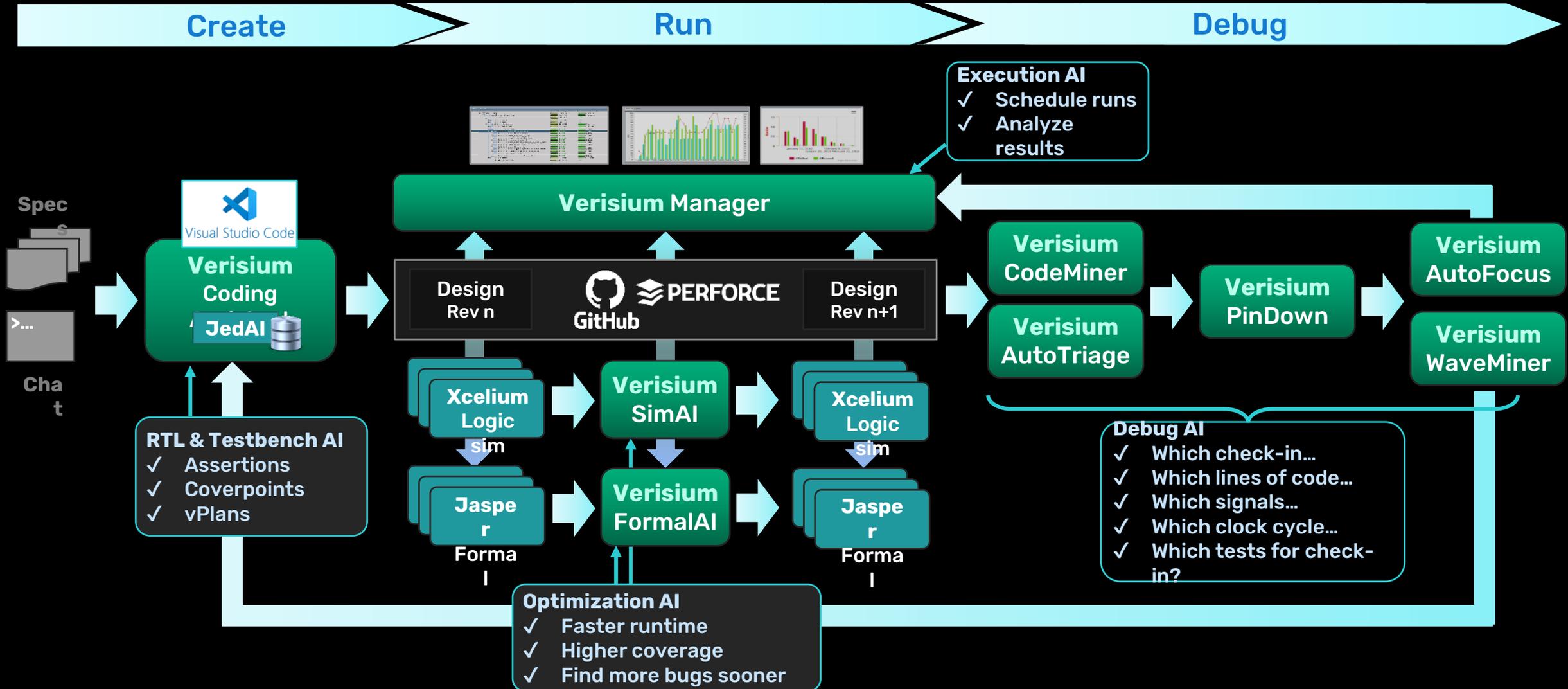
Agentic-AI Spec to Closure



Full Autonomy

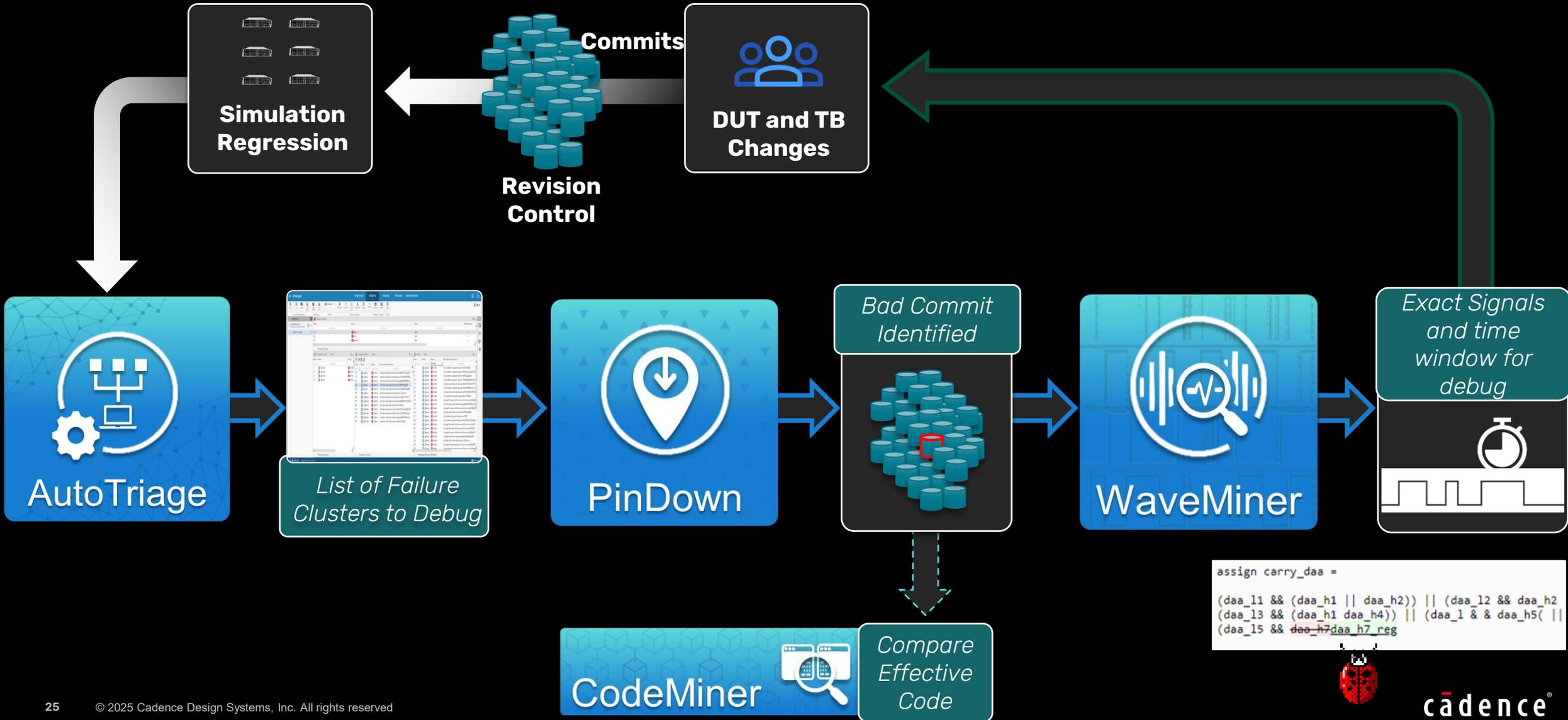


AI-Driven Verification Full Flow with Verisium AI



Verisium Apps – Used Standalone or in a Flow

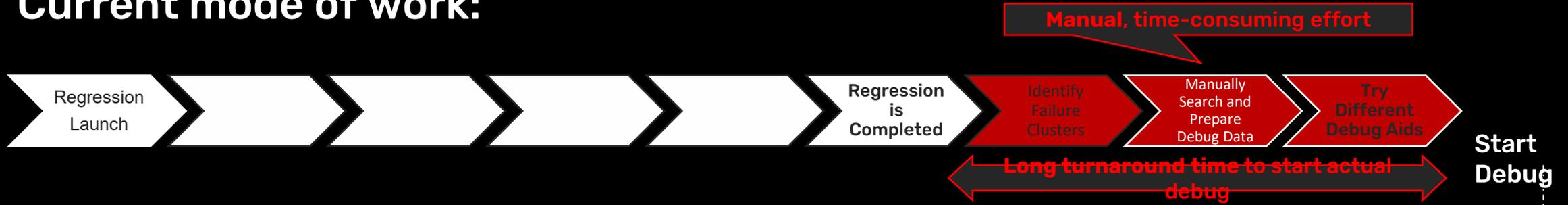
AI-Driven Root Cause for Regression Failures



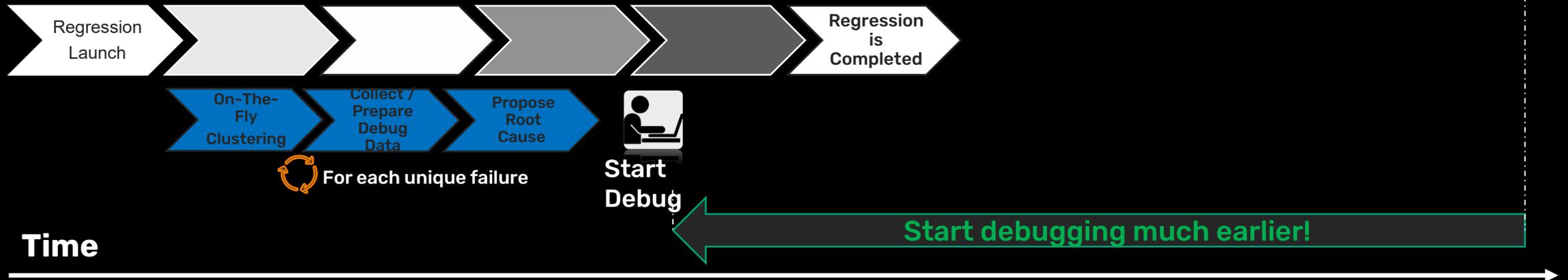
Verisium AI Assistant "Debug Ready"

Start debugging before regression completes, with no prep effort

Current mode of work:

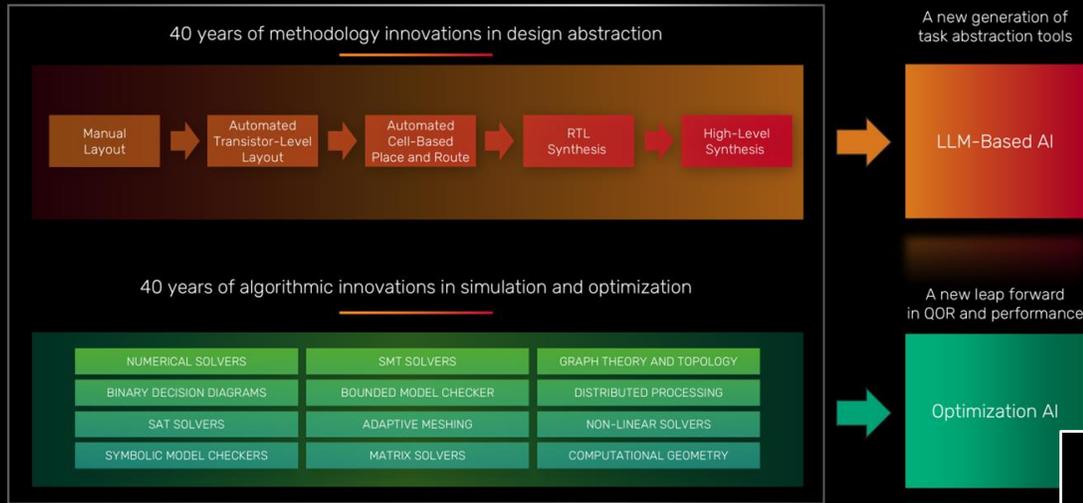


Debug Ready" flow:



Time

AI Opportunity in EDA

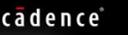


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The Journey to Autonomous Design



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Design for AI and AI for Design