Harnessing AI for Next-Gen EDA

Trends, Tools, and Technological Advancements

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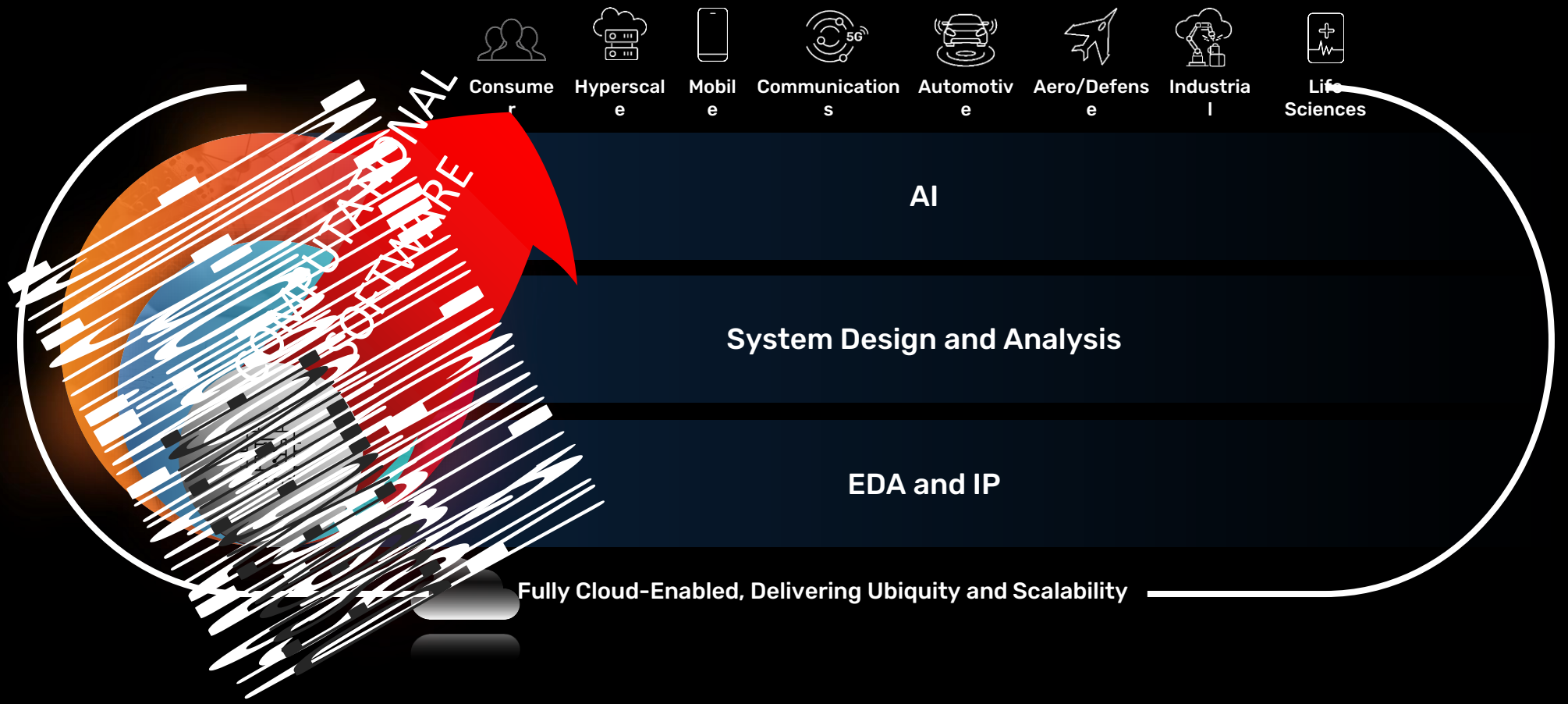
This presentation contains forward-looking statements based on current expectations or beliefs, as well as a number of preliminary assumptions about future events that are subject to factors and uncertainties that could cause our actual results to differ materially from those expectations or results described in the forward-looking statements. You are cautioned not to put undue reliance on these forward-looking statements, which are not a guarantee of future performance and are subject to a number of risks, uncertainties and other factors, many of which are outside Cadence's control.

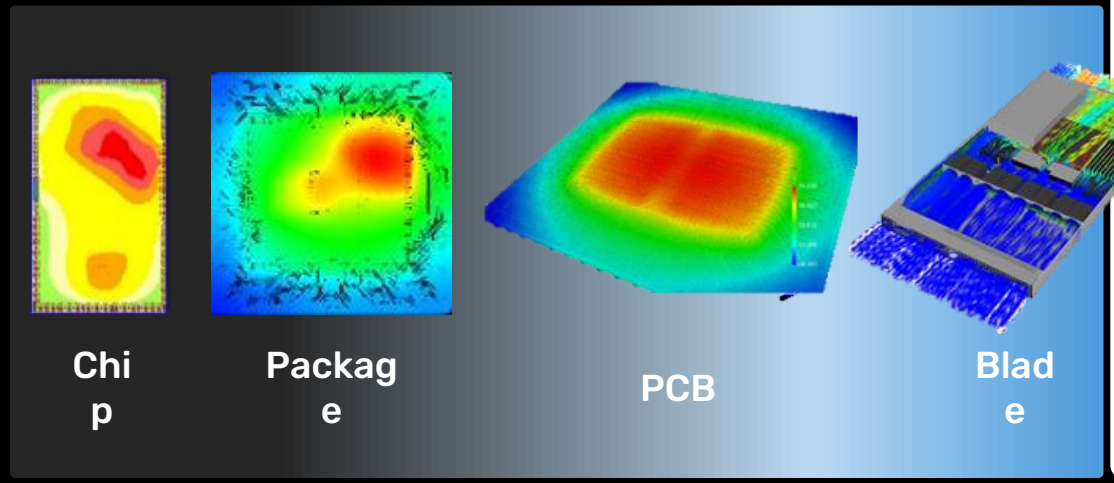
Cadence Intelligent System Design



Designing Data Centers with Computational Software

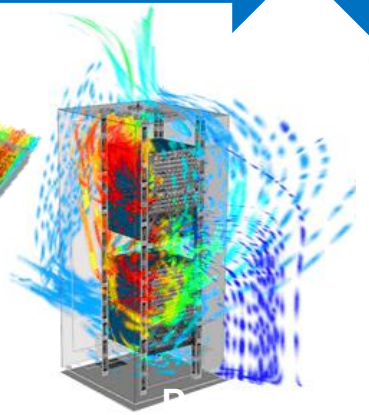
Analyze and Optimize Thermal from Chips to the Data Center

Celsius™ Thermal Solver



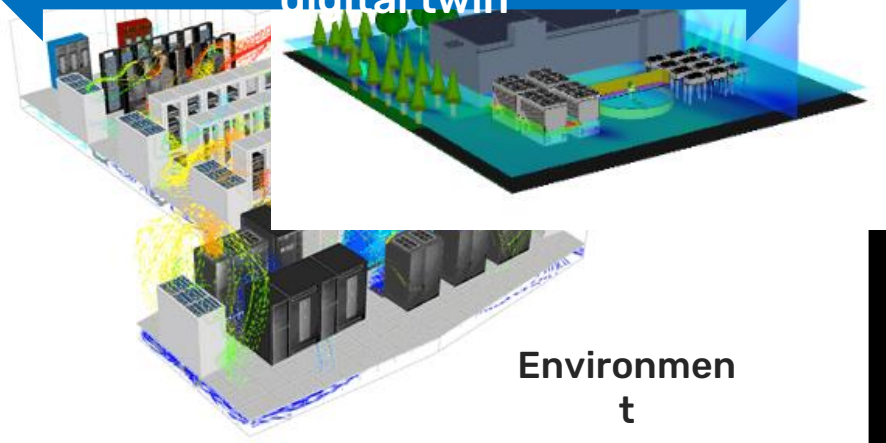
Chip | Package | PCB | Blade

Electronics cooling (CFD*)



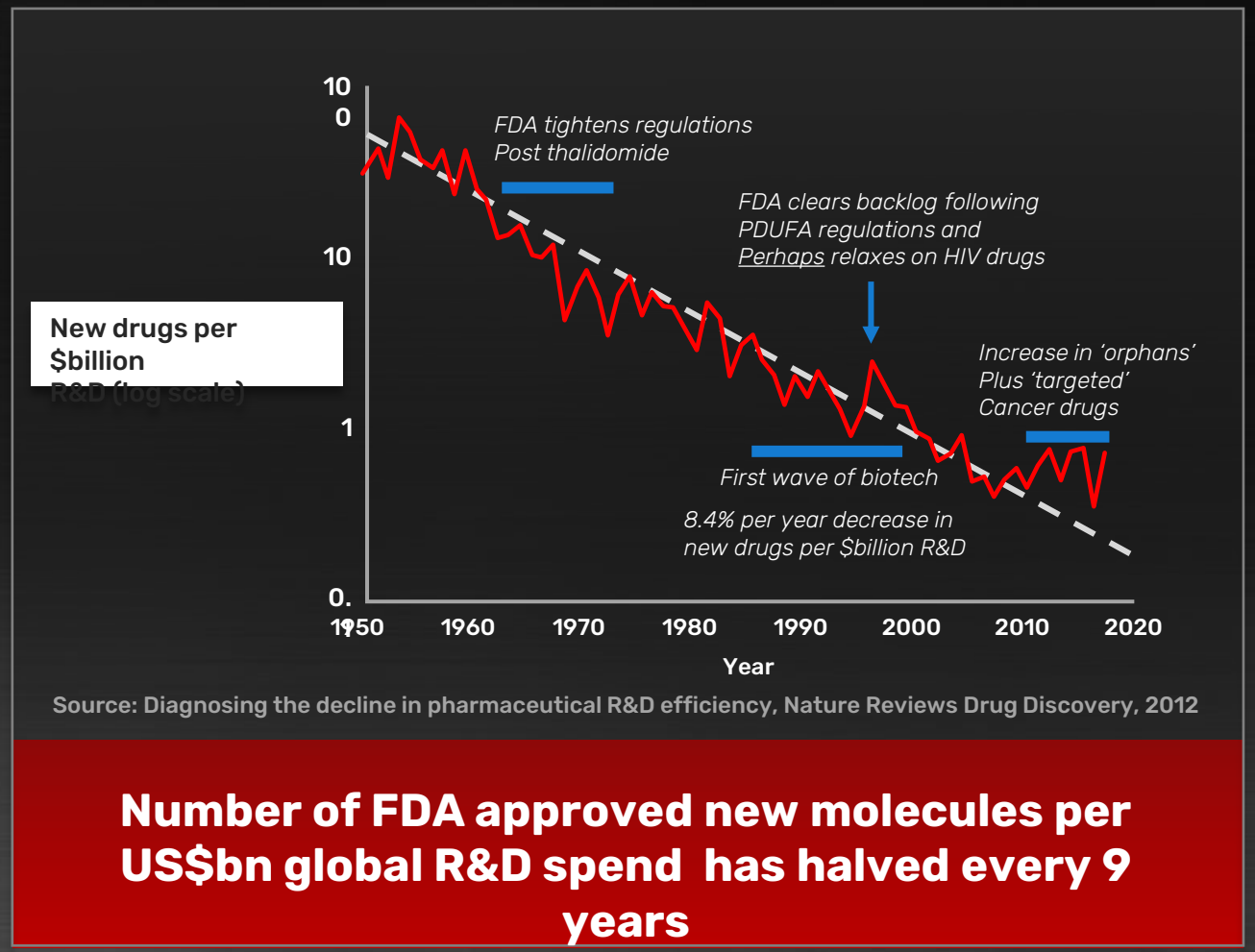
future facilities

6Sigma – Virtualizes the data center and ecosystem as a 3D digital twin



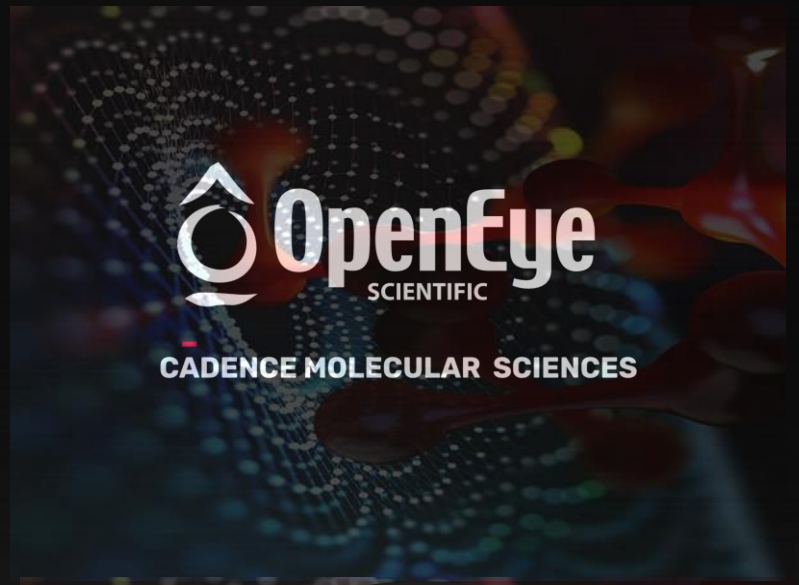
Environment

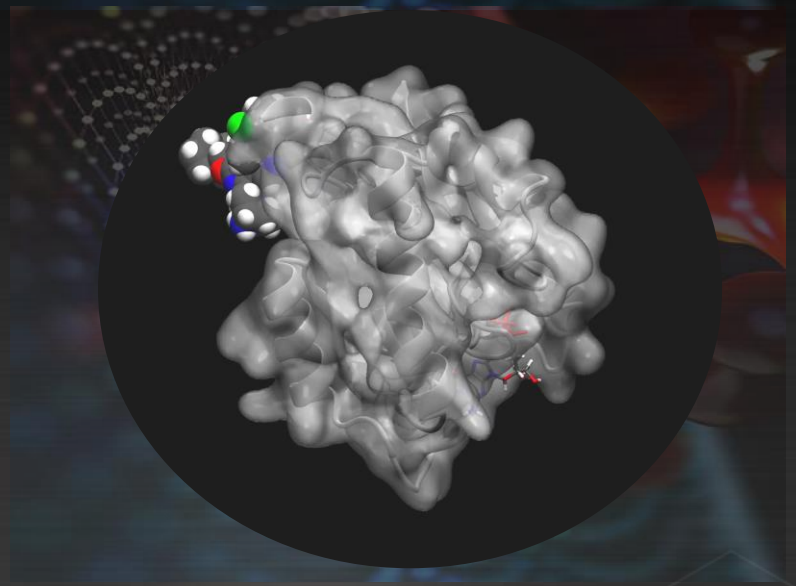
Drug Discovery with Computation Software



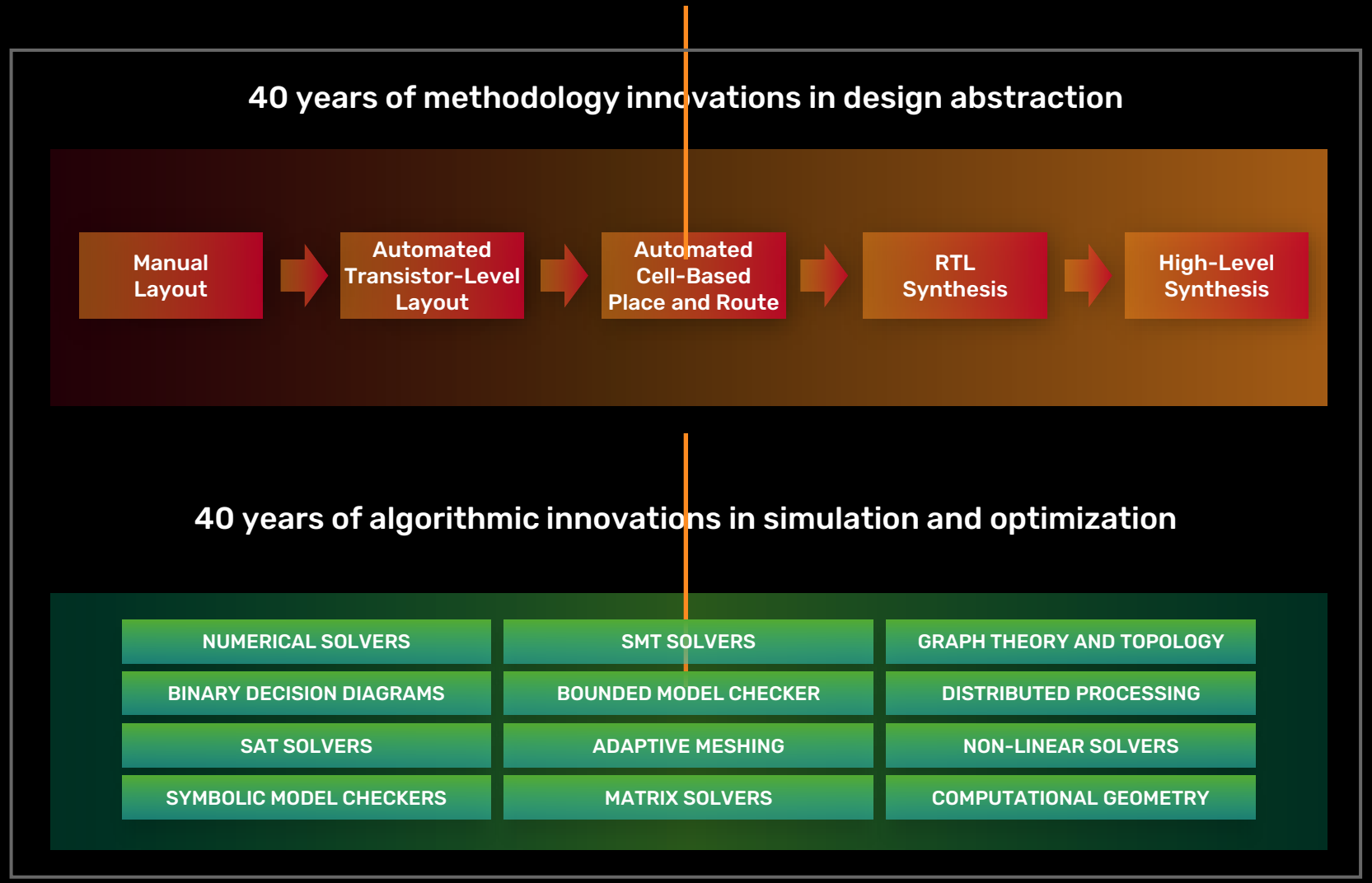
Source: Diagnosing the decline in pharmaceutical R&D efficiency, Nature Reviews Drug Discovery, 2012

Number of FDA approved new molecules per US$bn global R&D spend has halved every 9 years





AI Opportunity in EDA



A new generation of task abstraction tools

LLM-Based AI

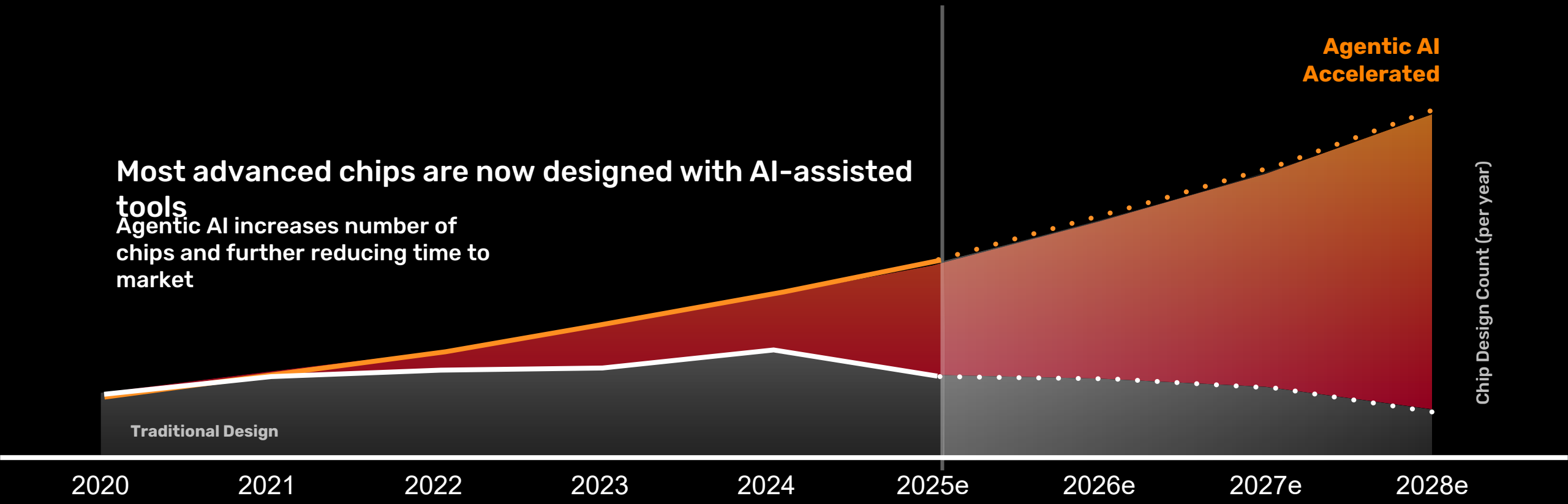
A new leap forward in QOR and performance

Optimization AI

AI-Driven Chip Design Inflection Point

Most advanced chips are now designed with AI-assisted tools

Agentic AI increases number of chips and further reducing time to market



Sources: Industry projections for tape-outs and AI adoption, and Cadence analysis.

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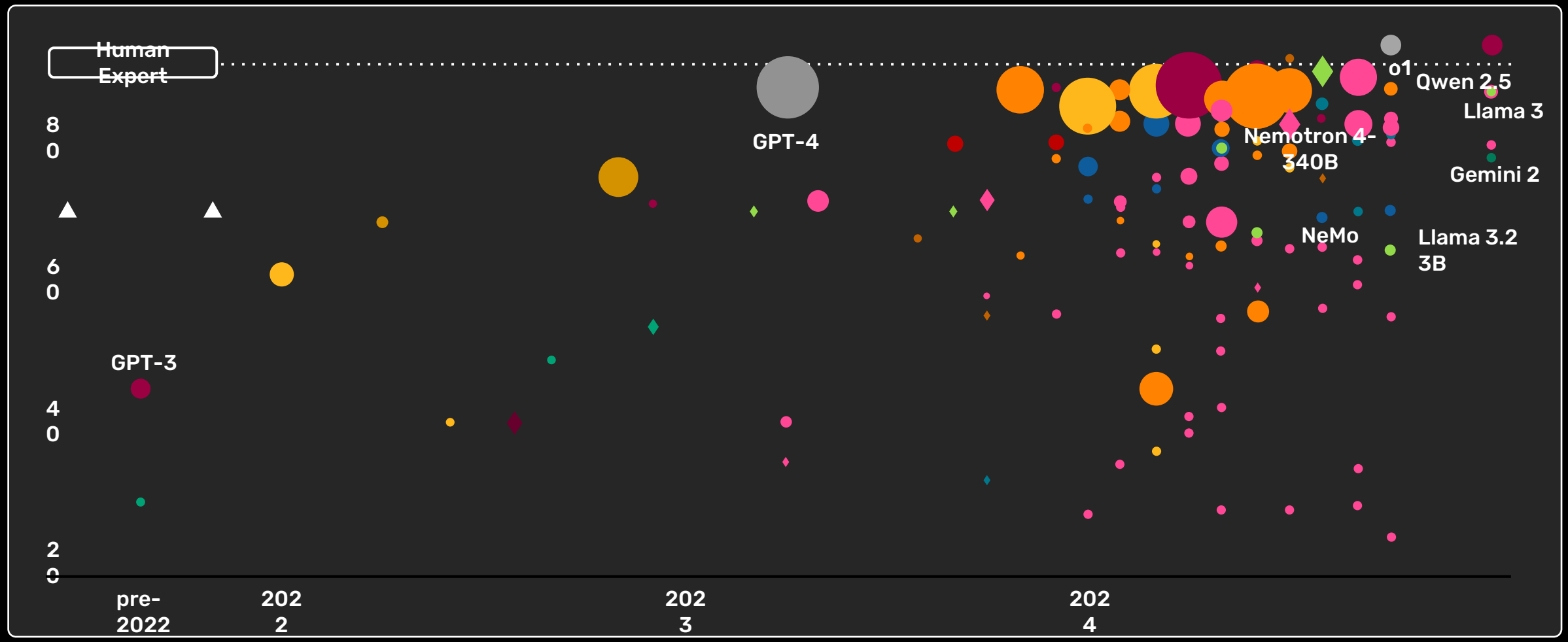
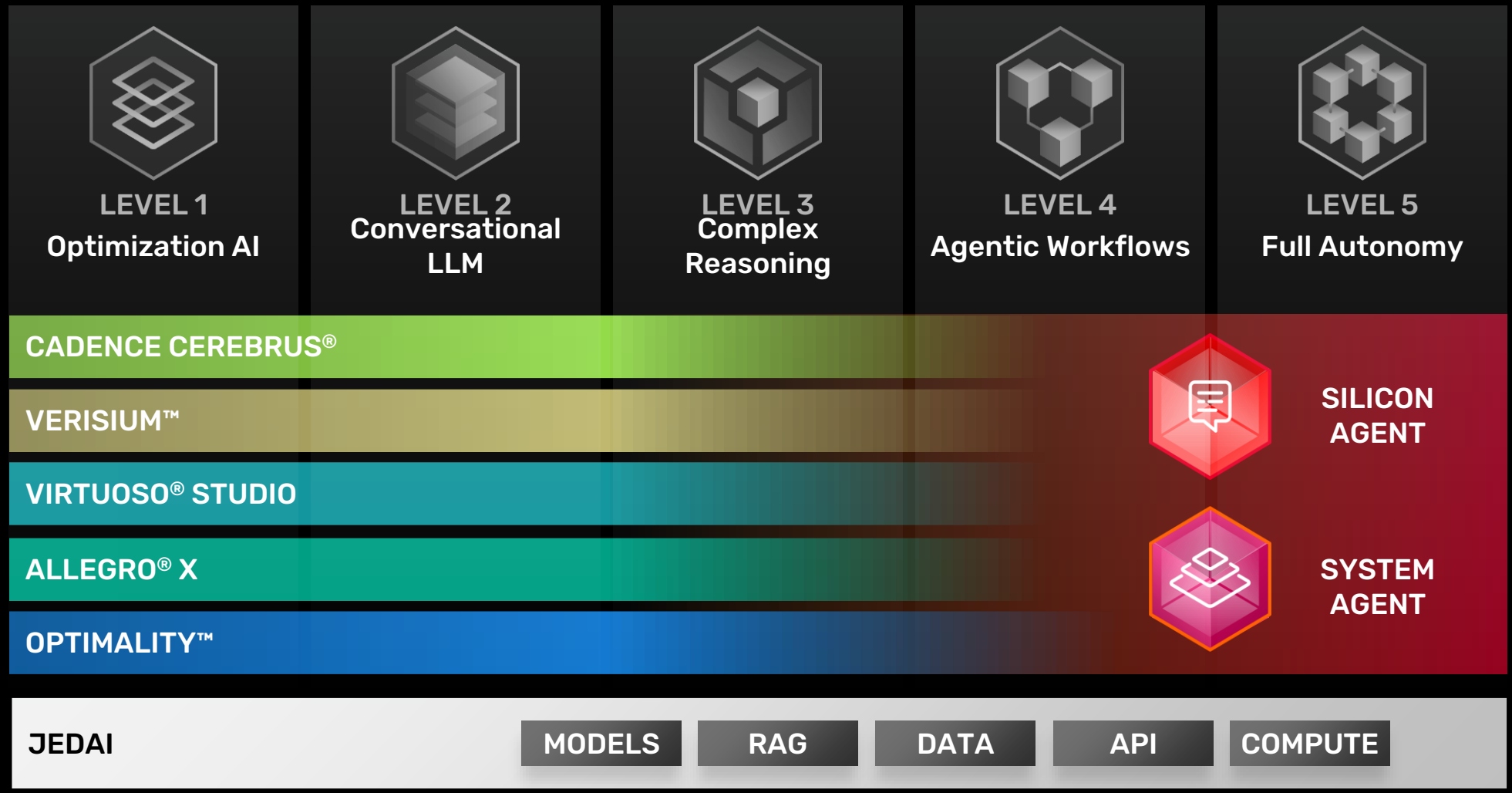
A New Age of Fuel Efficient Models

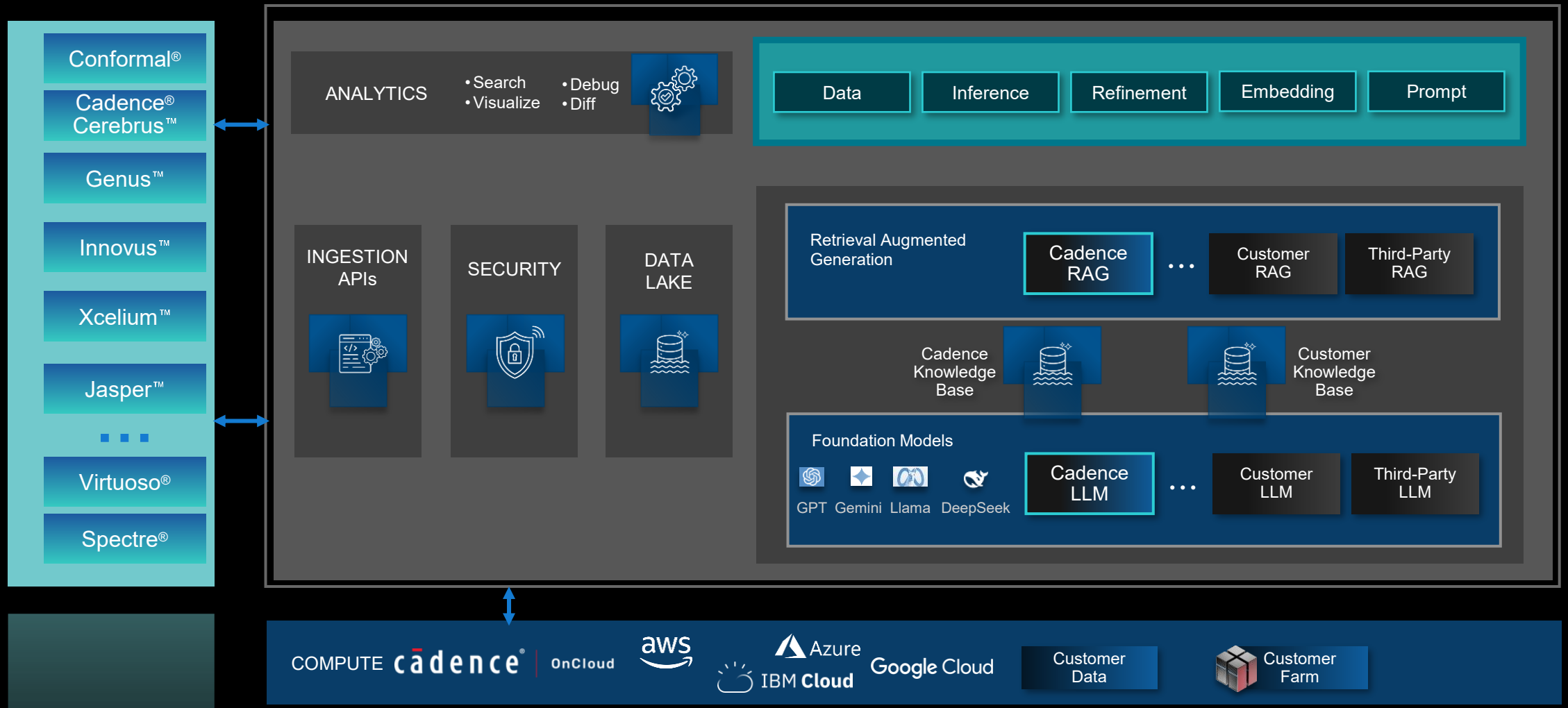


Source: https://labelyourdata.com/articles/llm-model-size

The Journey to Autonomous Design



Cadence JedAI Platform



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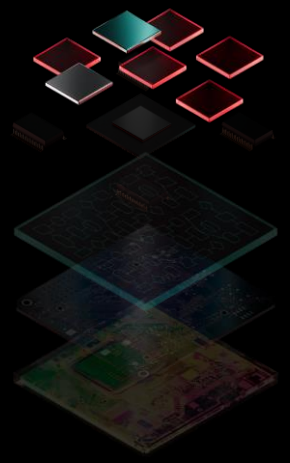
Optimization AI in Digital Implementation with Cadence Cerebrus

PPA-optimized chips and chiplets



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Chips-to-systems intelligent design acceleration

Optimization AI

OPTIMIZATION AGENTS

Cadence®

Cerebrus™

Digital Design

750

Successful design tapeouts

AI-Driven Power, Performance, Area Optimization

AI-ENHANCED DESIGN ENGINES

Genus™ | Innovus™ | Tempus™ | Stratus™ HLS

Customer	Node	Productivity	PPA
Foundry	4nm	**5X**	**8%** leakage
Mobile	4nm	**5X**	**10%** leakage
HPC	6nm	**5X**	**20%** PPA
Foundry	5nm	**5X**	**14%** FmaX
Automotive	7nm	**5X**	**8%** power
HPC	5nm	**5X**	**15%** power
CPU Core	N12	**4X**	**13%** PPA
AI	5nm	**4X**	**25%** power
Image Sensor	40nm	**15X**	**5%** PPA
Mobile	3nm	**5X**	**10%** power
Automotive	5nm	**5X**	**6%** power
Automotive	28nm	**5X**	**15%** leakage

Optimization AI in Digital Verification with Verisium SimAI

Bug-free designs

cadence.ai

Chips-to-systems intelligent design acceleration

Optimization AI

OPTIMIZATION AGENTS

Cadence®

Verisium™ SimAI

Debug and Verification

10X

Verification productivity

AI-driven automation and analysis for digital chip verification

AI-ENHANCED DESIGN ENGINES

Jasper™

Xcelium™

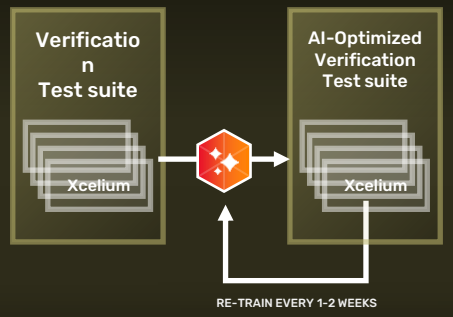
Design Type	Speedup
Modem IP	20X
Mobile SoC	7X
AI IP	8X
AI IP	3X
Memory IP	5X
Base Station	18X
NOC IP	5X
Automotive SoC	5X
CPU IP	3X
Network IP	4X
CPU IP	9X

Verisium

Verisium™

AI-driven digital verification delivers orders of magnitude speedup

AI-Optimized Simulation



SPEEDUP

20x	8x	9x
Modem IP	AI IP	CPU IP

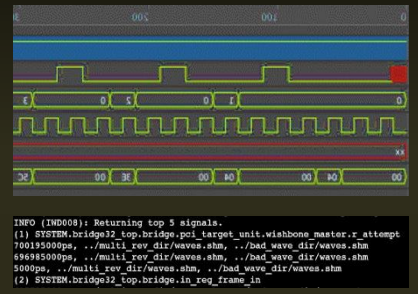
AI-Driven Bug Hunting

REGRESSION RUNS

IMPROVEMENT

6x	40x	7
Faster TAT	Less CPUs	New bugs found

AI-Driven Root Cause Analysis



SPEEDUP

30x	6x	10x
Memory Controller IP	Automotive SoC	Mobile SoC

Optimization AI in Jasper

Parallel runs find more bugs and achieve deeper proofs

Qualcomm CPU JUG 2023 Best Paper

Jasper Smart Proof
AI-Driven Orchestration

Proof Profiling Data	Proof Caching	Trace Replay	Proof Orchestration
• Keep engine-level settings that worked before	• Reuse the existing result if the constraints and COI are unchanged	• **Leverage previously found traces**	• **Use Machine Learning to find the best proof algorithm settings**

Multi-run optimization **+AI**

For fully-converging testcases:
- **5x reduction in runtime**
- **90x reduction in machine slots**

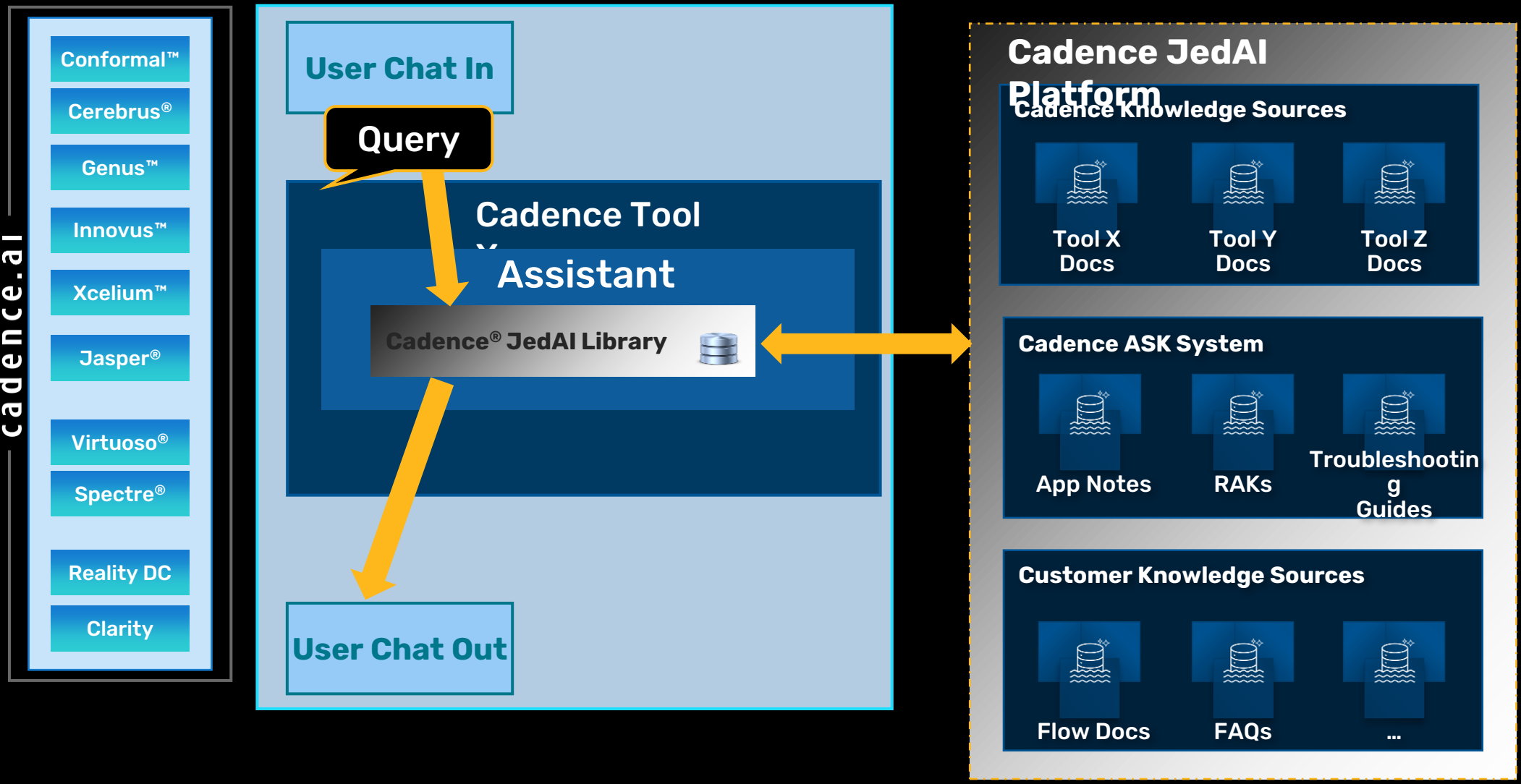
Find more bugs

Better convergence

Faster proofs

Conversational LLM Agents Across the Software Portfolio

LEVEL 2
Conversational LLM



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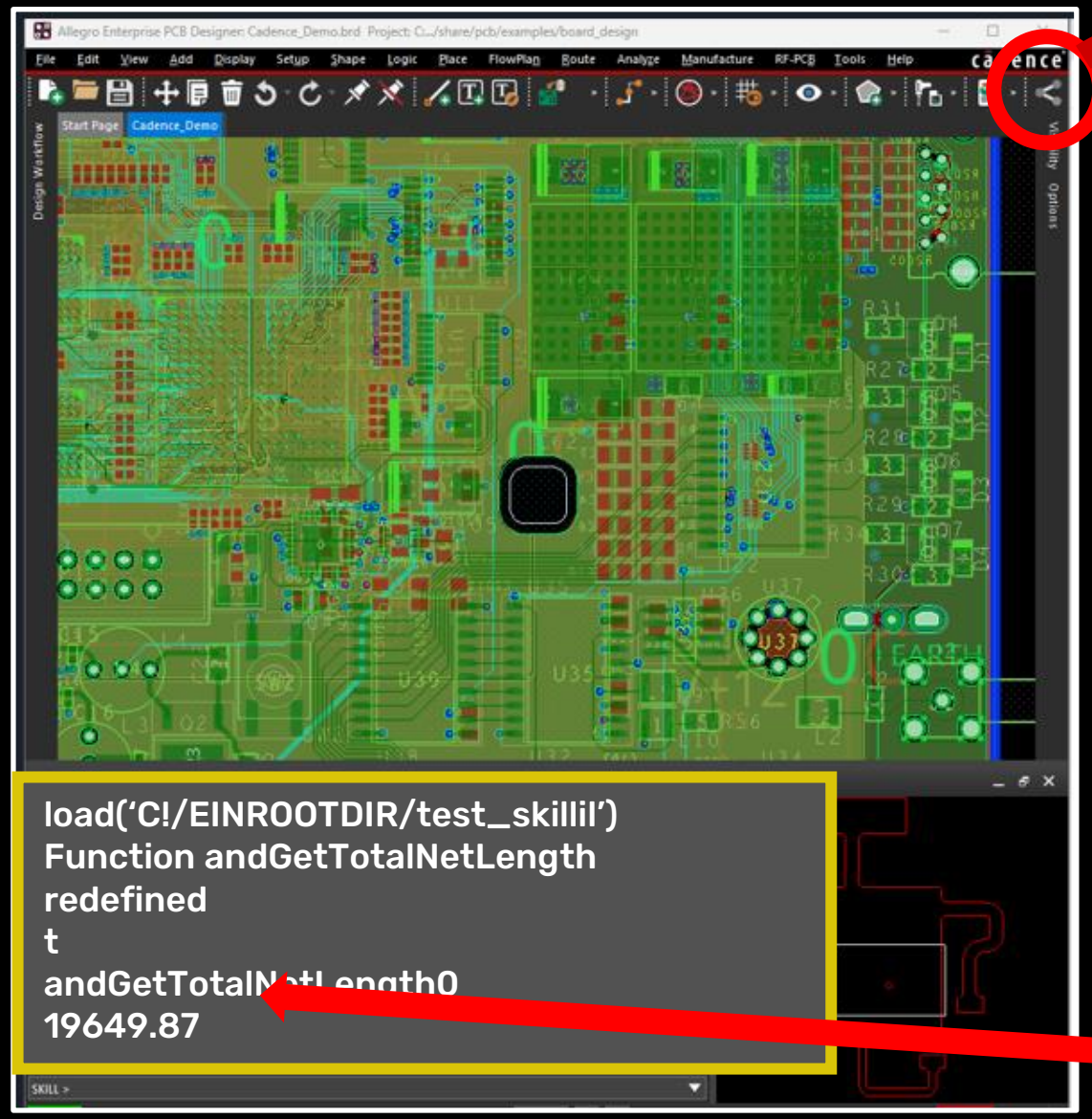
Allegro X Assistant: SKILL Coding Agent

LEVEL 2
Conversational LLM



Allegro SKILL Coding Agent

Enter your query:

Write SKILL code to get the total length of nets in the design?

Progress:

Starting query processing...

Generating draft code (Please wait)...

Draft code generated successfully...

Correcting for API usage: Trial 1...

Final Candidate:

```
```skill
; Get the total length of nets in the design
procedure(axlGetTotalNetLength()
    let((totalLength netList)
        ; Get the list of nets in the design
        netList = axlDBGetDesign()->nets

        ; Initialize total length to 0
        totalLength = 0

        ; Iterate over each net in the design
        foreach(net netList

            ; Add the length of this net to the total length
            totalLength = totalLength + axlDBGetLength(net)

        )

        ; Return the total length of all nets in the design
        totalLength

    )
)
```
```

Query processing complete!

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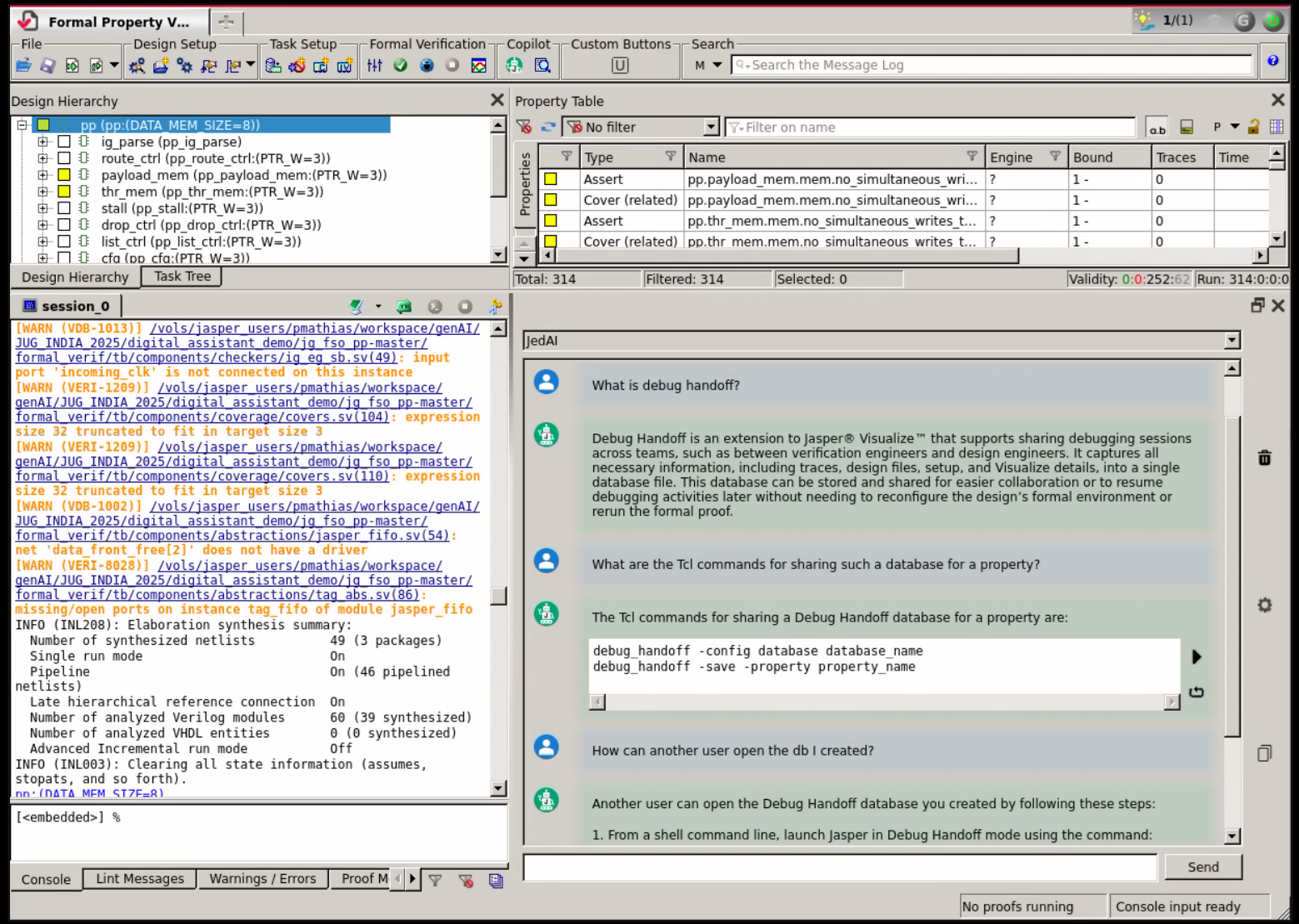
Jasper Knowledge Agent

LEVEL 2
Conversational LLM



- ✓ Basic doc search and straightforward command querying from NL
- ✓ Connection to Cadence or customer-provided LLM via JedAI
- ✓ Open queries to streamline general routines
- ✓ History
- ✓ Future integration with JedAI Library to enable ASK and customer knowledge sources

This slide contains forward-looking statements regarding Cadence's business or products. Actual results may differ materially from the information presented here.

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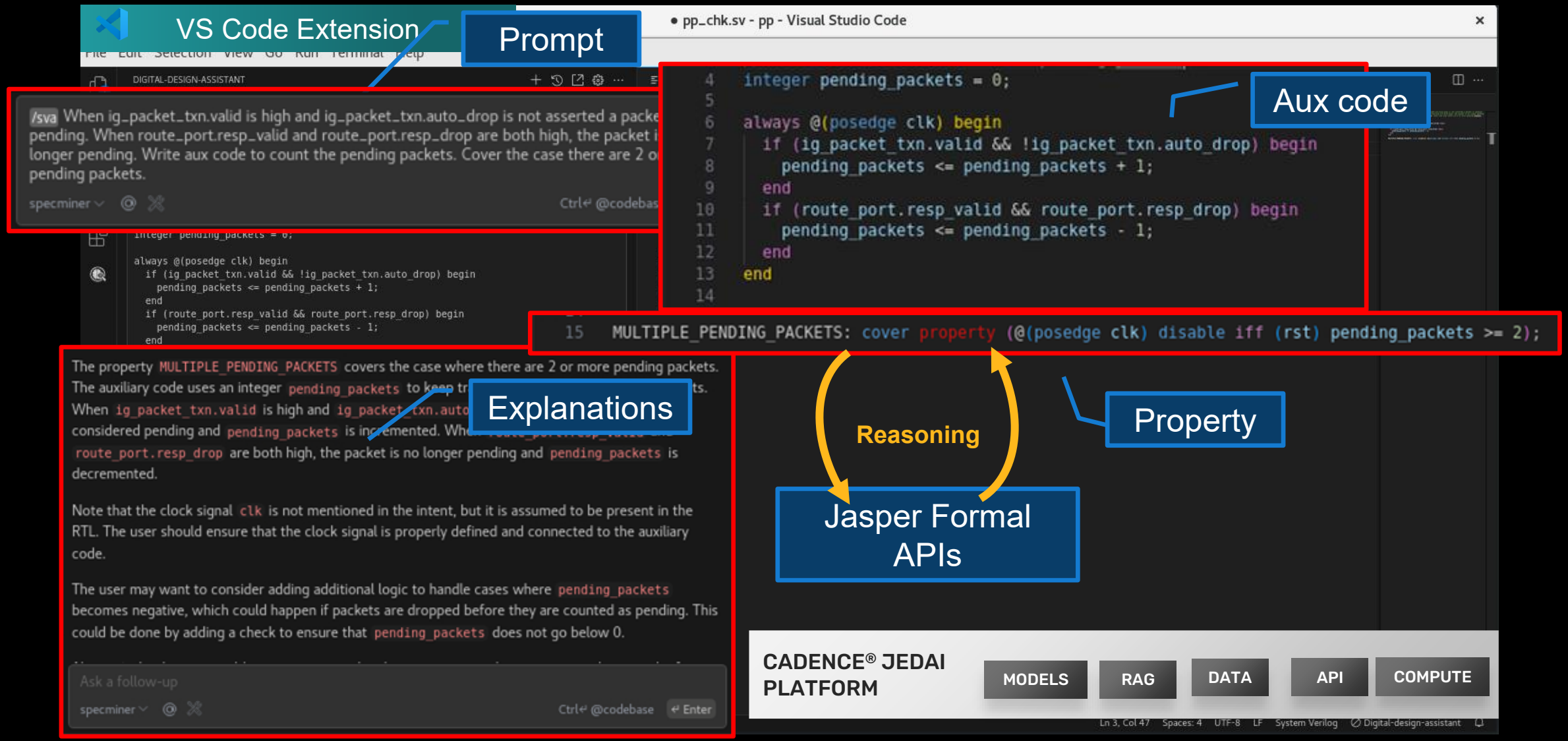
VS Code Extension: Example SVA and Aux Code Gen

LEVEL 3
Complex Reasoning



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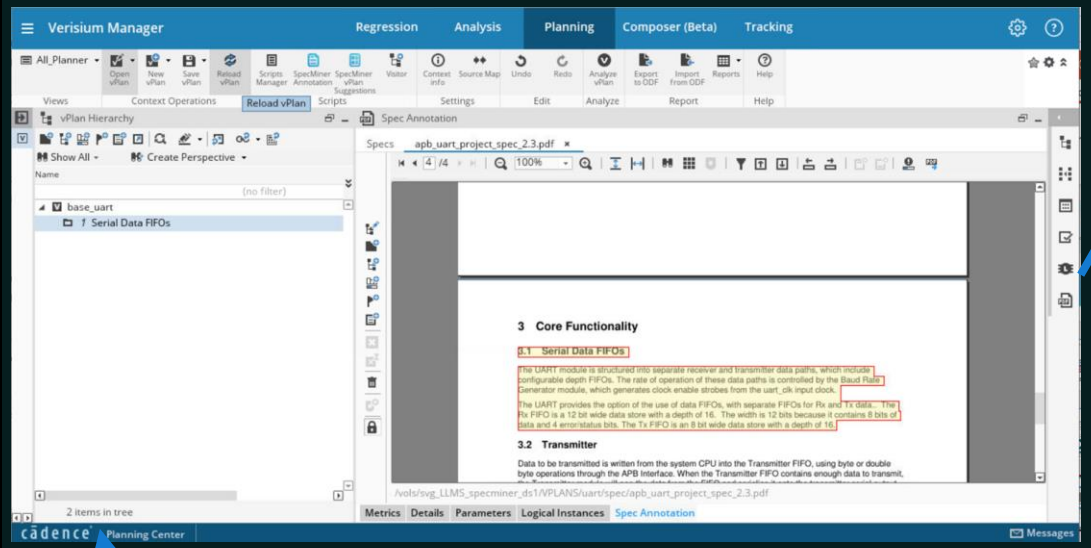
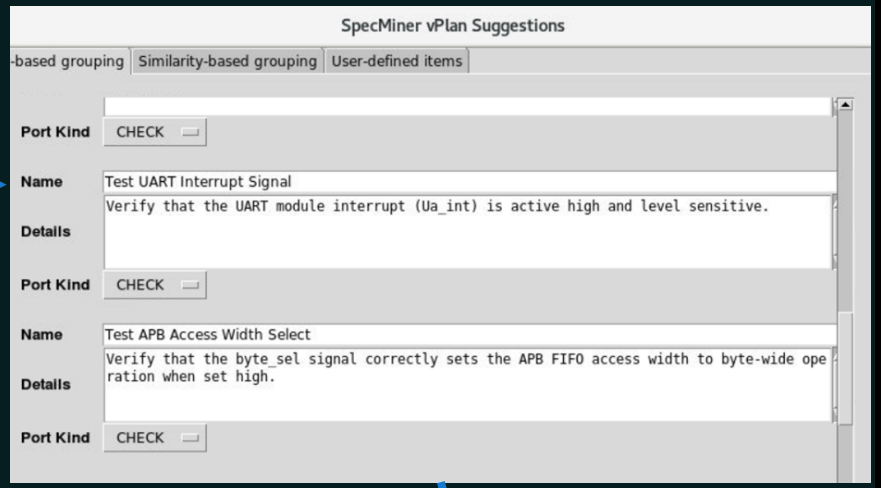
Agentic AI in Verisium UI – Verification Plan Gen

LEVEL 3
Complex Reasoning



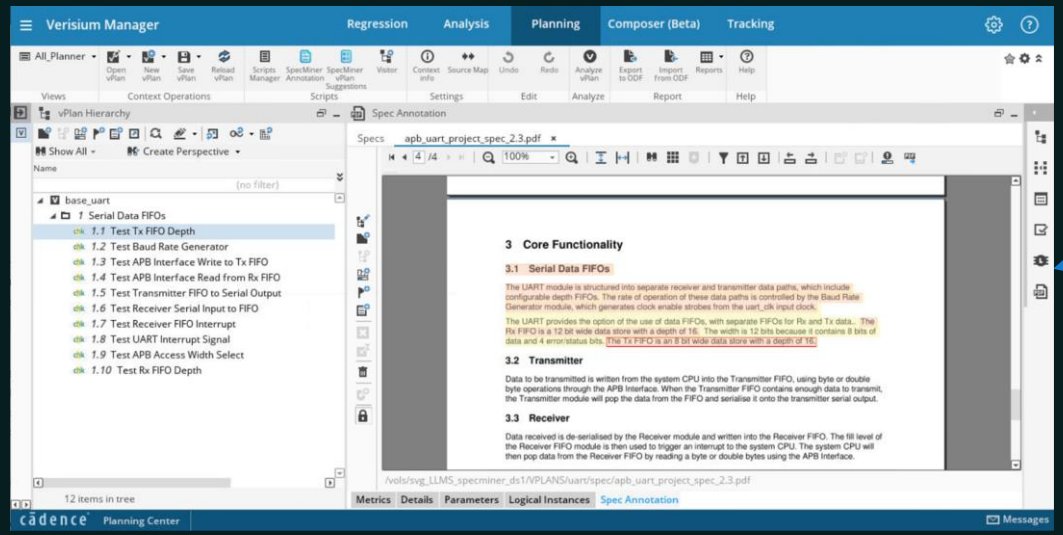
1

SpecMiner proposes vPlan sections



2

User selects suggestions that are relevant, accepts to vPlan



3

User selections recorded and used to improve future iterations

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LEVEL 4
Agentic Workflows

CADENCE Cerebrus

CADENCE

Cerebrus® AI Studio

Agentic AI digital design implementation platform

Accelerated Design Closure

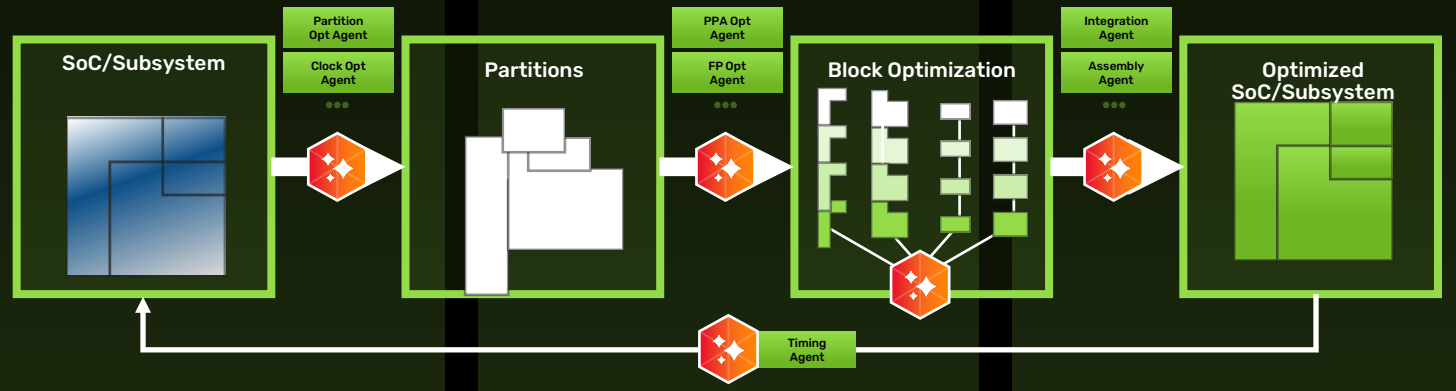
Integrated design platform
Advanced data analytics for faster debug
Smart model selection for faster optimization

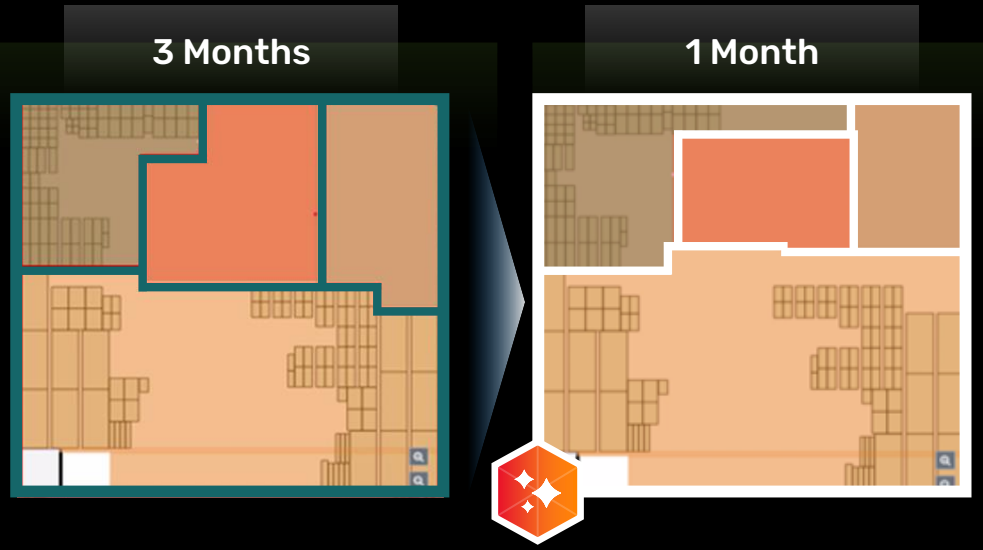
Breakthrough Productivity

Engineer workload parallelization
Accumulated learning over time
Powerful design dashboard

Unparalleled PPA

Agentic AI workflows
Top-block co-optimization
Hierarchical design closure





30%	Improvement in Timing
10%	Improvement in Power
1%	Improvement in Density

Advanced CPU Core	3.3M Instances 5nm

Virtuoso® Studio

Agentic AI enables custom design migration

RENESAS

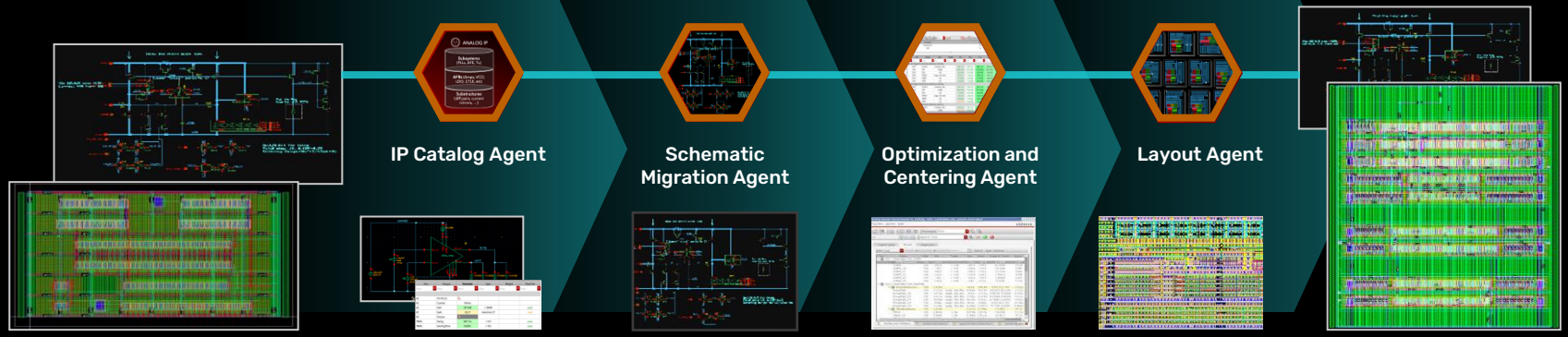
UP TO **70%**
Productivity Improvement

130nm → 55nm
4nm → 3nm
Legacy and Advanced Nodes

Defense | HPC | AI | Powe
ommunications | Imaging | Aerospac
Broad Production Adoption

Suite of AI Agents

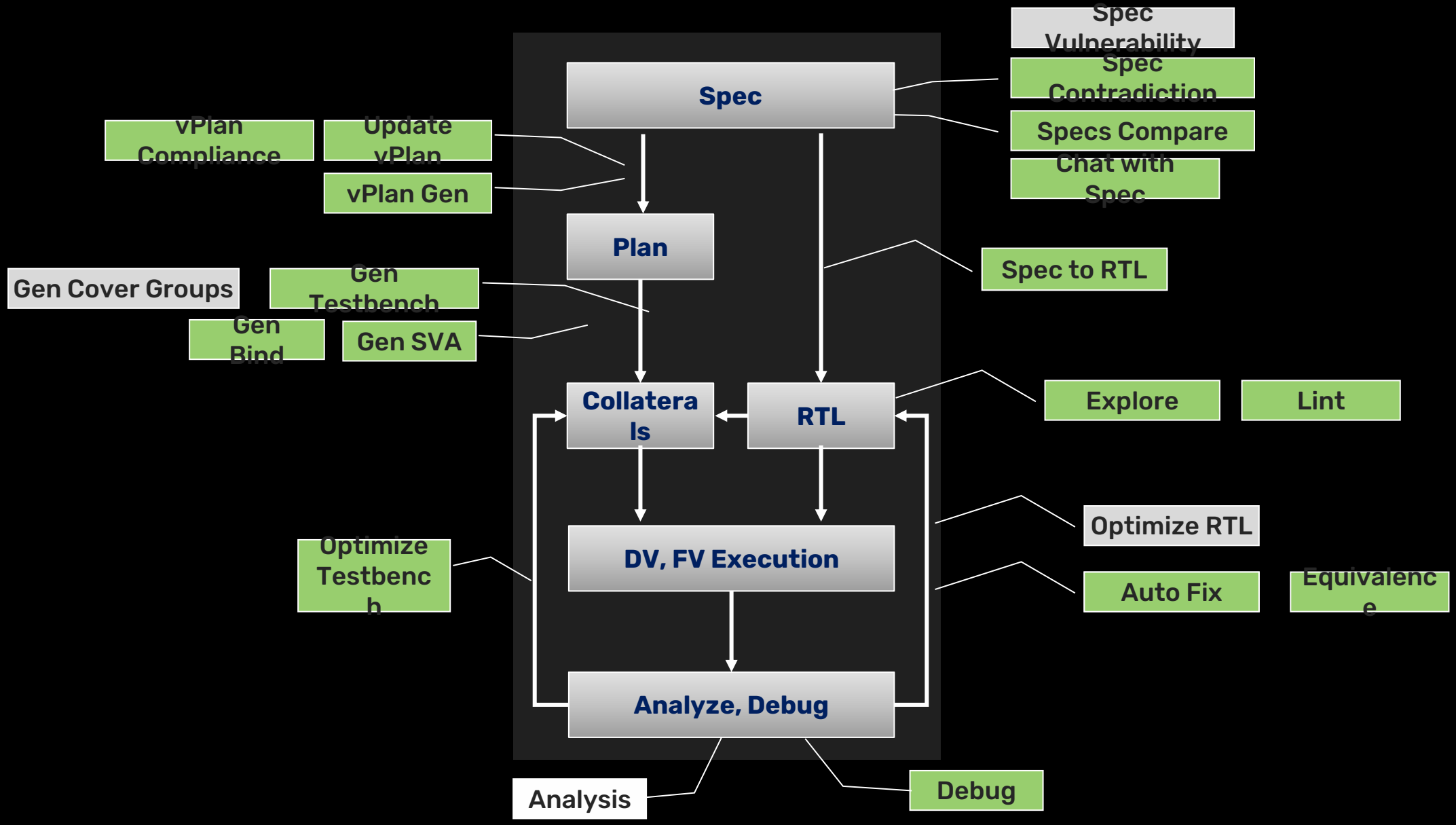
Custom Design Migration



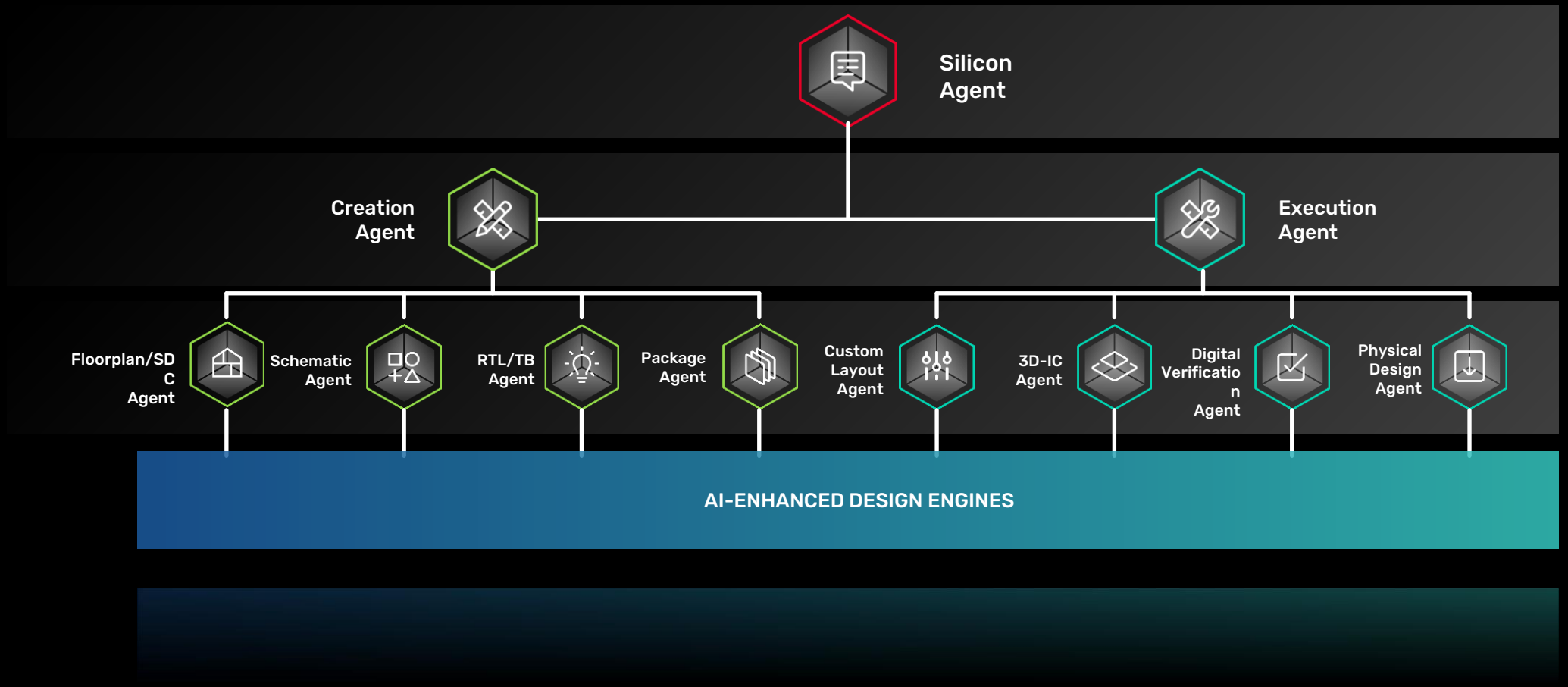
Source
Schematics, Testbench, & Layouts

Migrated
Schematics, Testbench, & Layouts

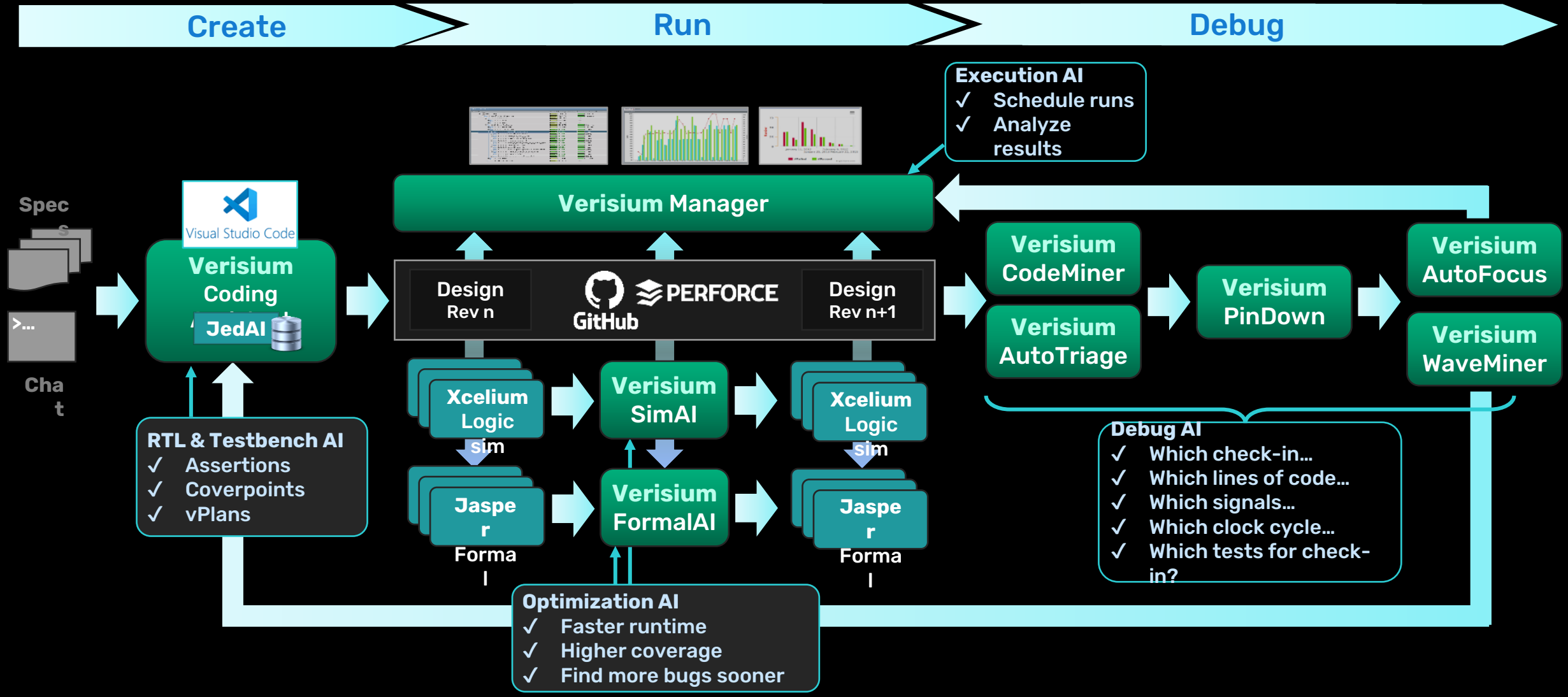
Agentic-AI Spec to Closure



Full Autonomy



AI-Driven Verification Full Flow with Verisium AI



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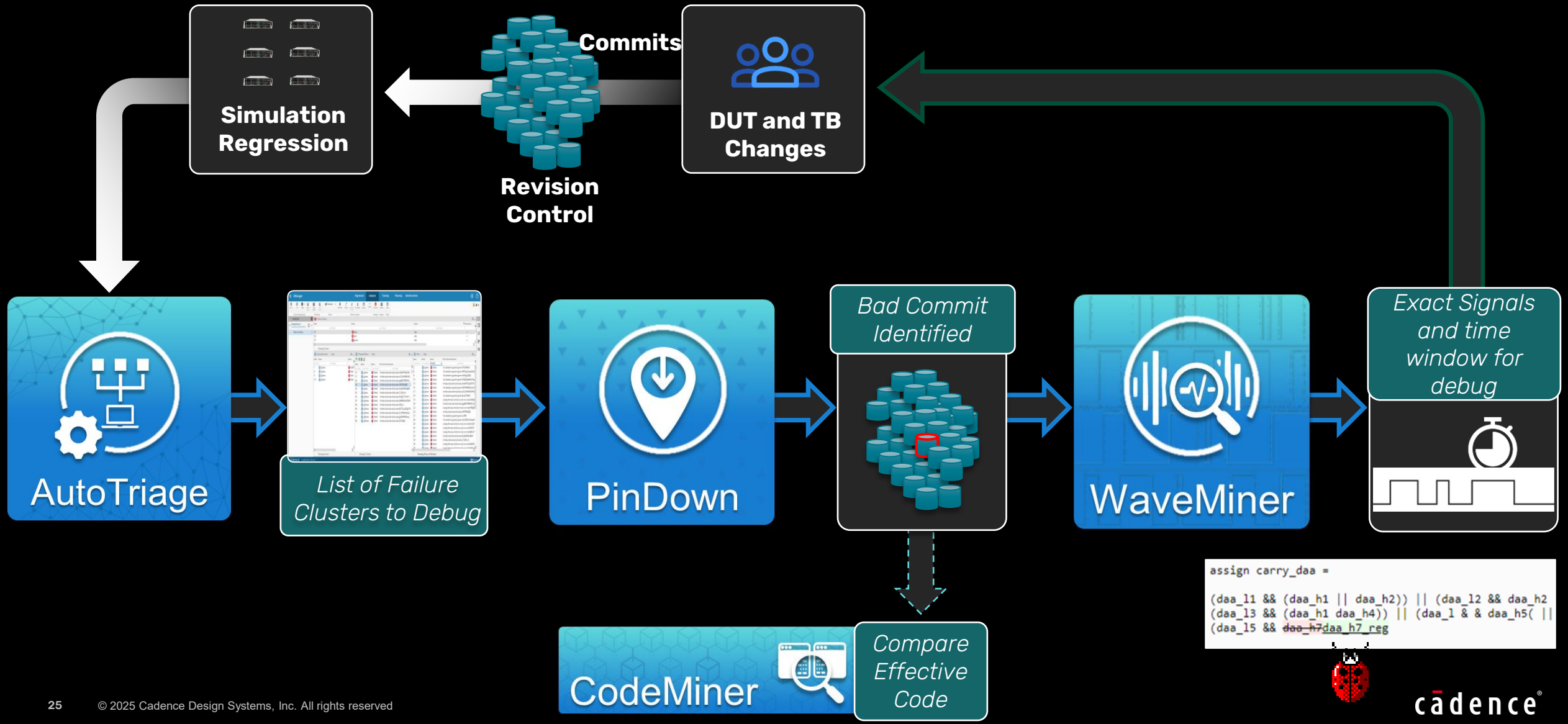
Verisium Apps – Used Standalone or in a Flow

AI-Driven Root Cause for Regression Failures



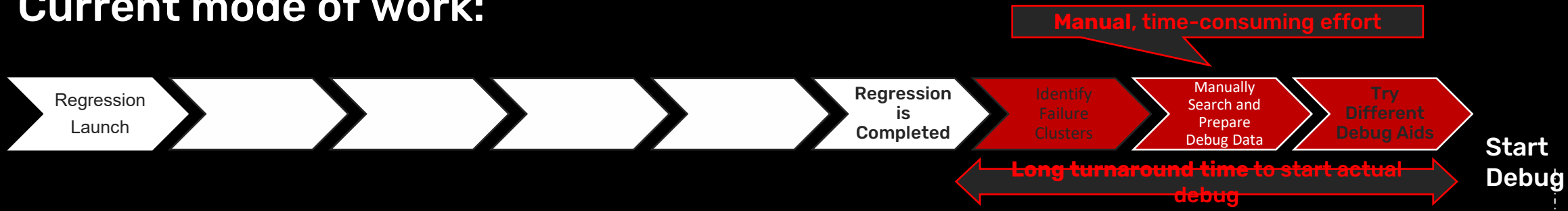
Verisium AI Assistant “Debug Ready”

Start debugging before regression completes, with no prep effort

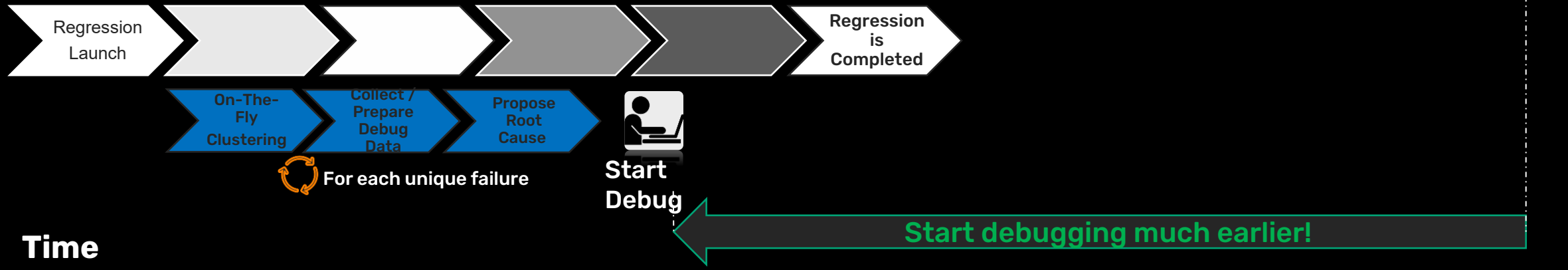
Manual

Automated

Current mode of work:



Debug Ready” flow:



AI Opportunity in EDA

40 years of methodology innovations in design abstraction

Manual Layout → Automated Transistor-Level Layout → Automated Cell-Based Place and Route → RTL Synthesis → High-Level Synthesis

A new generation of task abstraction tools

LLM-Based AI

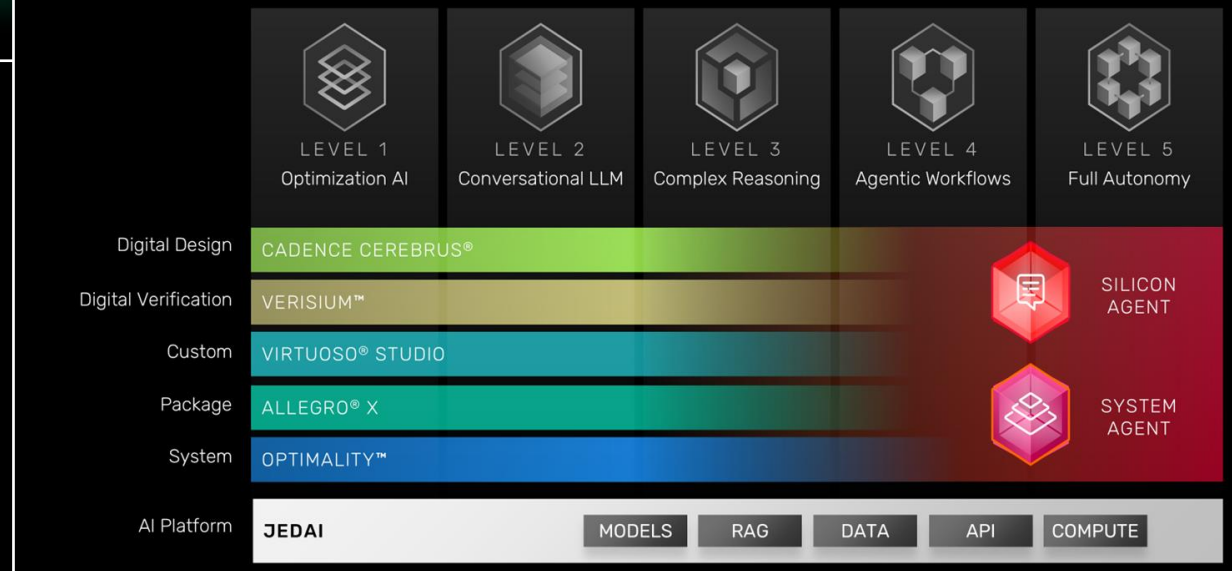
40 years of algorithmic innovations in simulation and optimization

NUMERICAL SOLVERS	SMT SOLVERS	GRAPH THEORY AND TOPOLOGY
BINARY DECISION DIAGRAMS	BOUNDED MODEL CHECKER	DISTRIBUTED PROCESSING
SAT SOLVERS	ADAPTIVE MESHING	NON-LINEAR SOLVERS
SYMBOLIC MODEL CHECKERS	MATRIX SOLVERS	COMPUTATIONAL GEOMETRY

A new leap forward in QOR and performance

Optimization AI

The Journey to Autonomous Design



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Design for AI and AI for Design