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CXL verification using portable stimulus

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< Add Presenter /Co-Presenter Headshot here>

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- Interests: Language design, Technologies that use PS and HSI, Virtual Platforms, Embedded systems

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CXL verification using portable stimulus

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Who are we?

Vayavya Labs

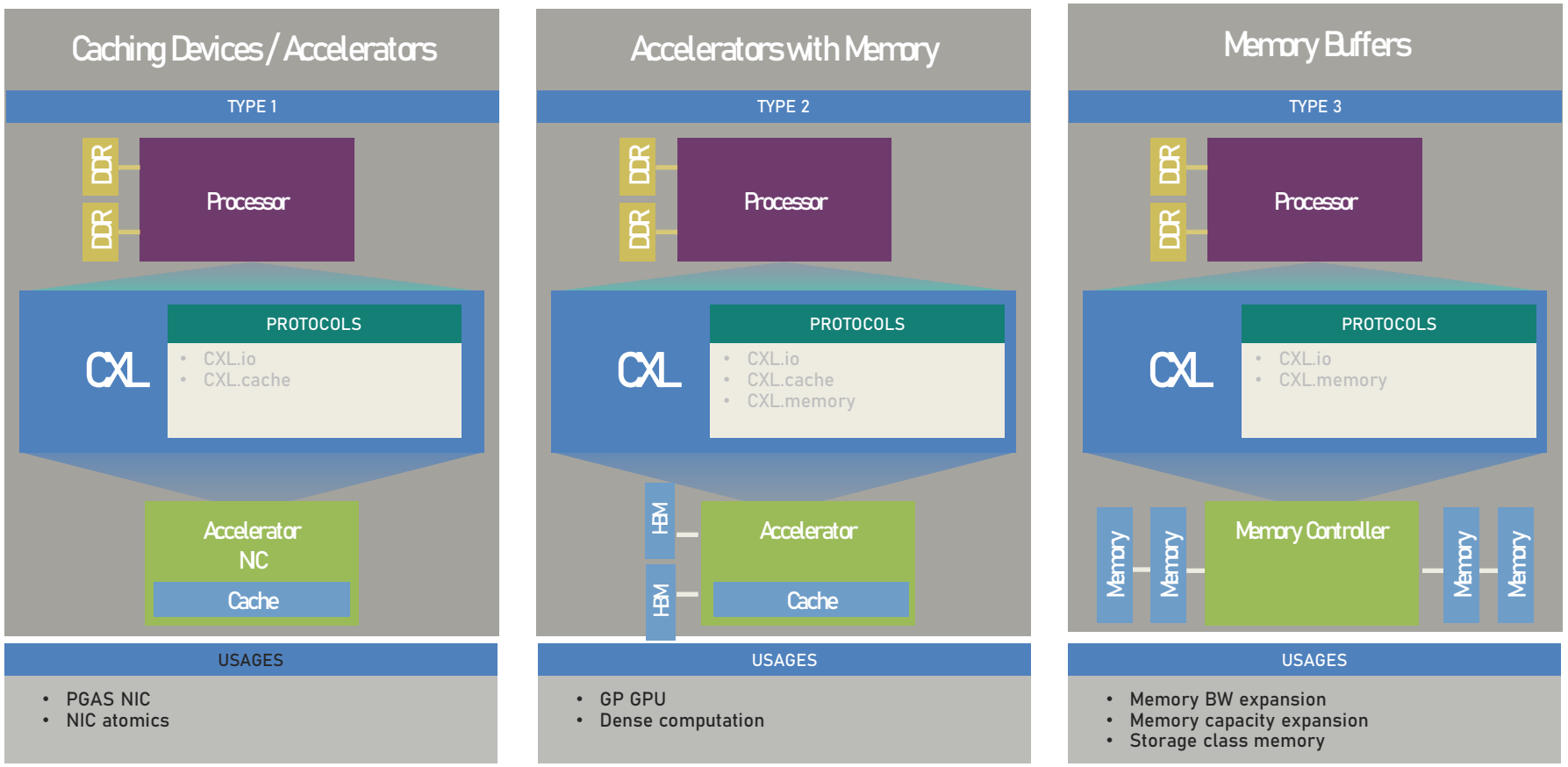
- 17+ old EDA/ESL company
- “Single source” HSI specification
- Embedded software experts
- Part of Accellera PSWG workgroup

Please check the brochure for more information!

What is CXL?

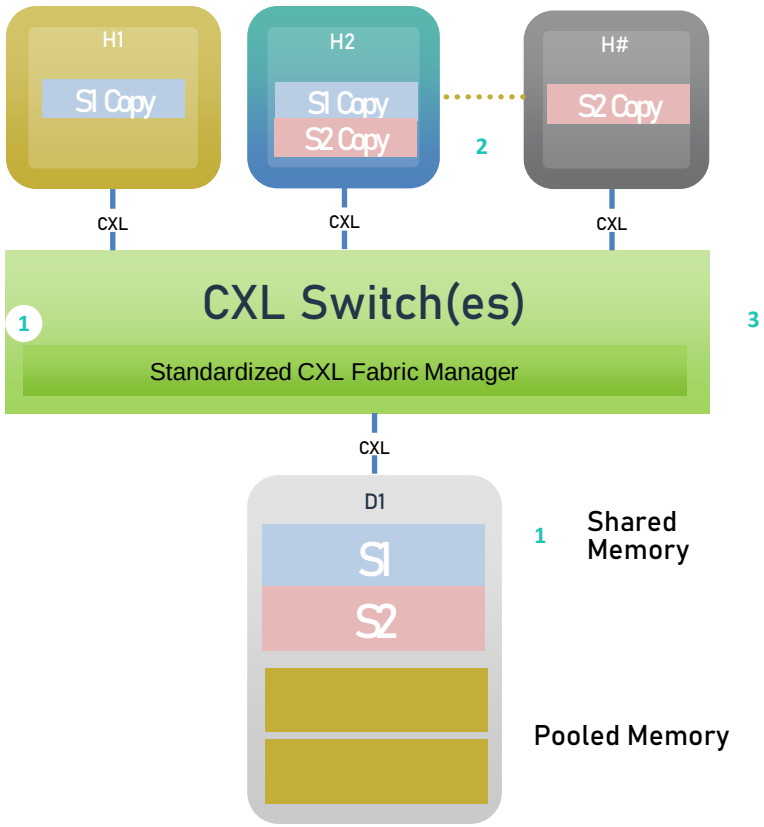
- New breakthrough high-bandwidth and low latency fabric
  - Enables a high-speed, efficient interconnect between CPU, memory and accelerators
  - Builds upon PCI Express® (PCIe®) infrastructure, leveraging the PCIe® physical and electrical interface
  - Maintains memory coherency between the CPU memory space and memory on CXL attached devices
- Delivered as an open industry standard
  - CXL 3.0 specification is fully backward compatible with CXL 2.0 and CXL 1.1
  - Future CXL Specification generations will include continuous innovation to meet industry needs and support new technologies

Representative CXL Usages



Source: CXL™ Consortium 2022

CXL 3.0: COHERENT MEMORY SHARING



Source: CXL™ Consortium 2022

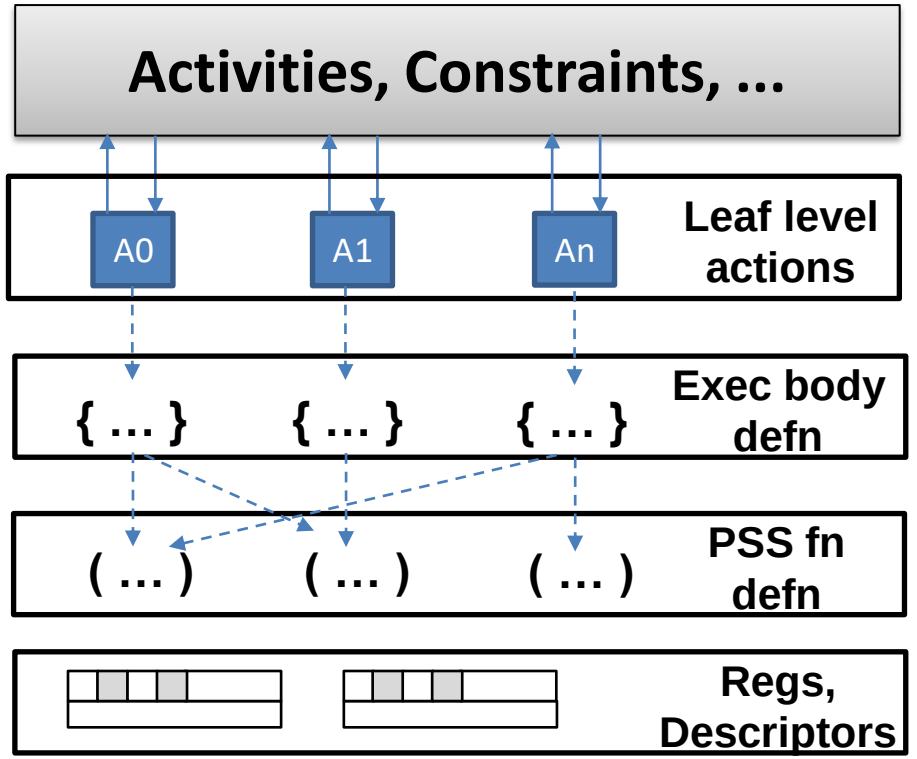
1. Device **memory can be shared by all hosts** to increase data flow efficiency and improve memory utilization

2. Host can have a **coherent copy of the shared region** or portions of shared region in host cache

3. CXL 3.0 defined **mechanisms to enforce hardware cache coherency** between copies

What is Portable Stimulus Standard(PSS)

- Standard developed by Accellera
- Specification to create a single representation of stimulus and test scenarios
- Generation of diverse implementations of a scenario that run on a variety of execution platforms
- Representation of some view of a system's behavior, along with a set of abstract flows



Why PSS model for CXL

Multiple dynamic and configuration parameters needs crossing, making hard for randoms to cover

Coherency and ordering rules cannot just be verified at unit level

Scalable topologies, shared resources and scheduling challenges

SW world behaviour needs to be modelled for verification

Software behaviour modelling for verification

- System firmware and drivers, OS hypervisors have important role to play in CXL
- They are micro-architecture aware so we need to model their behaviour to certain extent in verification environment early to make sure we model the traffic more realistically to expose issues that matter
  - System firmware(UEFI BIOS) does enumeration and sets up CEDT(CXL Early Discovery Table) for the OS
  - Hypervisors participate in the memory scaling using HMAT(Heterogeneous Memory Attribute Table) and SRAT(System Resource Affinity Table) tables created through ACPI
- If it needs to be modelled better done through PSS so we can leverage it at different hierarchies

Coherency and ordering rules

- CXL aims to build heterogeneous and disaggregated compute environments
- Which means memory sub-systems and coherency problem is no longer problem of unit implementing it
  - Cache coherence is no longer restricted to CPU clusters
  - Memory ordering is no longer restricted to Memory subsystems
- Where we need the cache coherency/memory ordering verification?
  - Unit
  - Subsystem (Headless)
  - Full system – Software driven system
  - Emulation and prototyping
  - Post silicon

Multiple configuration and dynamic state crossing

- Cache state transitions (MESI)
- Multi-processor and devices with shared states
- Different physical memory types
  - Persistent (Storage class)
  - Non-persistent (DRAM)
- Memory pooling
  - Single logical devices (SLD)
  - Multiple logical devices (MLD)
- RAS
- Security
- Integrity and Data encryption(IDE)
- Low power states handling

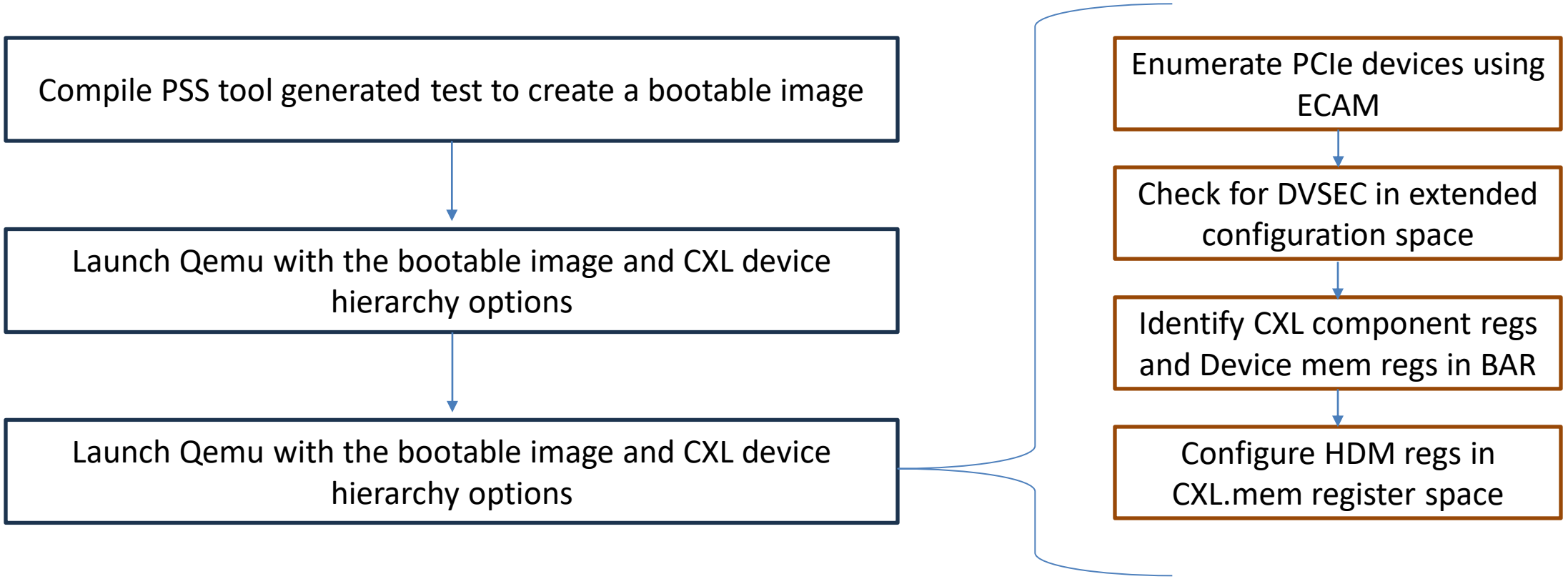
CXL PSS Model – Common parameters

Area	PSS model configuration parameters
CXL Version	• CXL 1.1, CXL 2.0 and CXL 3.0
Topologies	• Single Type1, Type2 and Type 3 Device directly connected to Host • Single Multi-headed Type 3 device connected to Host • Host port connected to multiple Type1, Type2 and Type 3 Devices with single level Switch • Host port connected to multiple Type1, Type2 and Type 3 Devices through multiple level Switch
PCIe Speed	• Gen 5.0 and 6.0
Memory Devices	• Single Logical Device(SLD) • Multiple Logical Device(MLD)
IDE	• Enabled and Disabled
Security	• Keys enabled and disabled

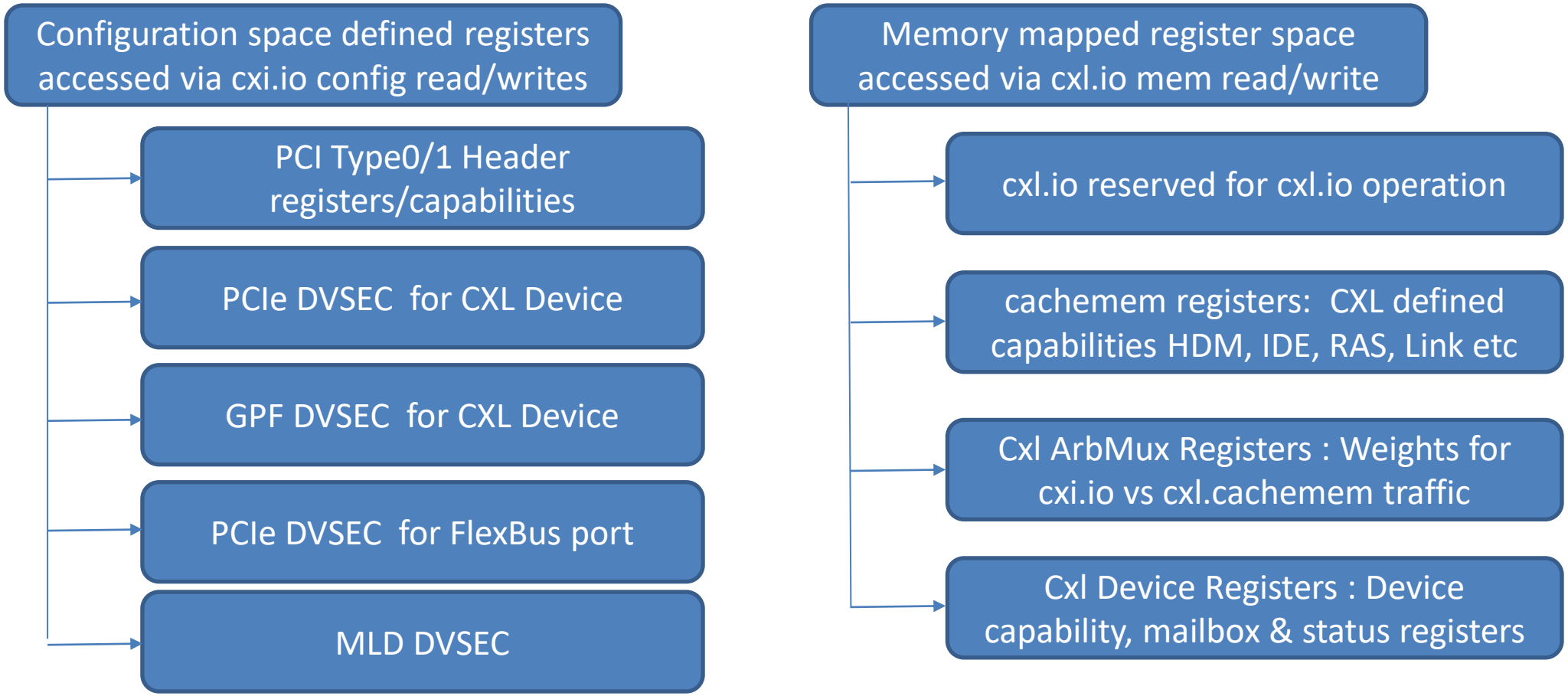
Demo : CXL Type 3 device enumeration on Qemu

- Uses Qemu as the target platform
- Uses the topology of Type 3 device connected to host
- Models the CXL type 3 register space
- Top level activity does the following
  - Enumerates CXL host and device through ECAM using CXL.io
  - Check for CXL DVSEC in extended configuration space
  - Uses the DVSEC information to Identify the location of CXL component registers and device mem registers in the BAR region
  - Configure the HDM registers in the CXL.mem register space

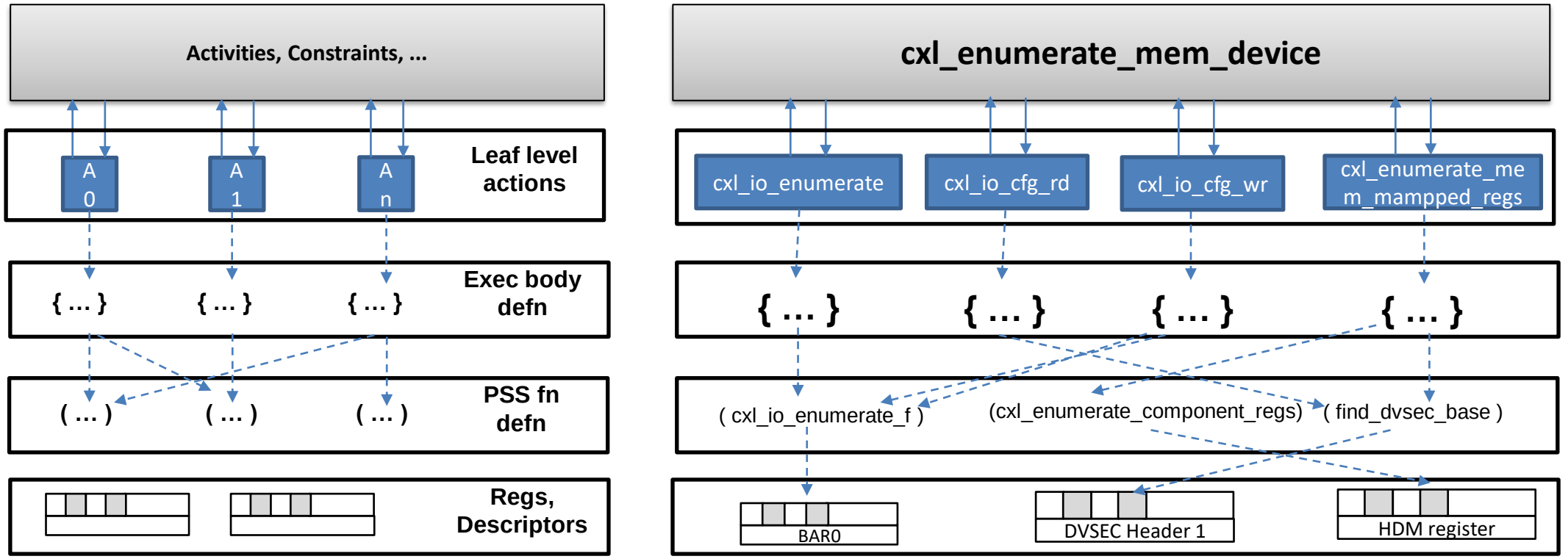
Demo flow



CXL Type 3 Device – Register space to be modelled



CXL Type 3 Device Model



Q&A? FEEDBACK?