Navigating the Maze: Verifying Multi-Module PHY designs in UCIe Multi-Die Systems

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Abstract- The demand for increasingly complex and high-performance semiconductor solutions has led to the rise of multi-die systems, where multiple chiplets are integrated into a single package to achieve superior functionality and performance. **UCIe (Unified Chiplet Interconnect Express)** is an interface protocol aims to standardize the interface between chiplets allowing them to interoperate seamlessly regardless of their manufacturer or specific functionality within a single package.

The **multi-module PHY (Physical layer)** in UCIe plays a crucial role in scaling the bandwidth between chiplets. The main idea centers around leveraging the inherent advantages of multi-module configurations within the UCIe PHY to maximize throughput. It connects using the existing single RDI (Raw Die-Die Interface) with upper layer and multiplies the PHY link interface as showcased in **"Fig. 1"**.

This paper delves into the intricacies of verifying multi-module PHY designs within UCIe multi-die systems, emphasizing the critical role of pre-silicon verification in achieving post-silicon success.

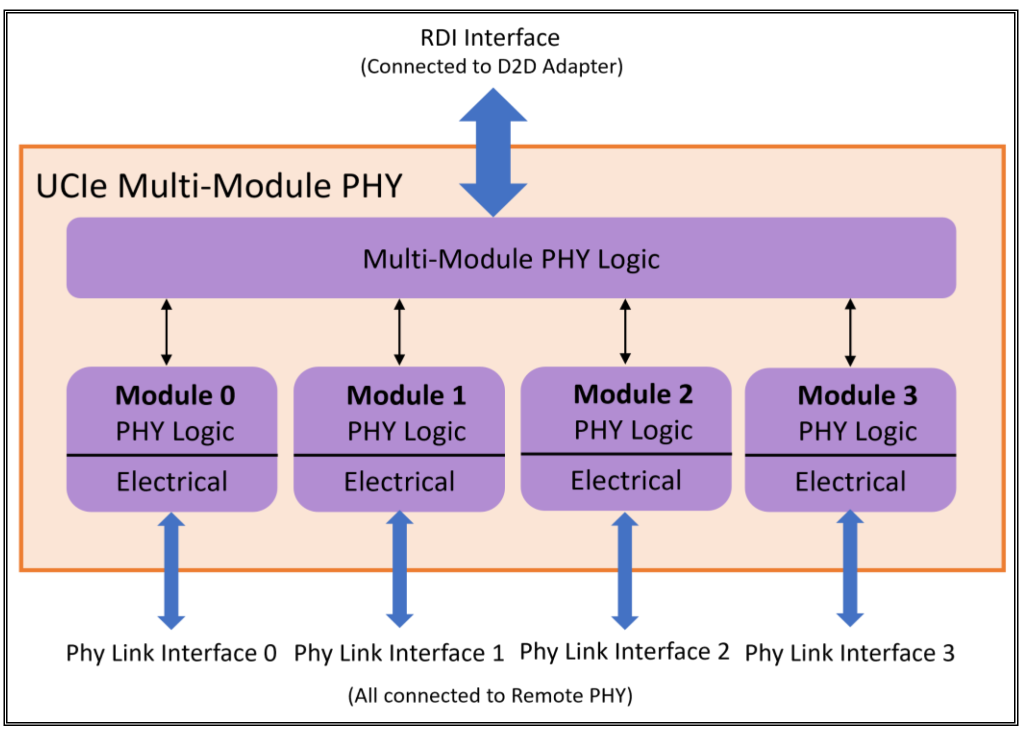

Figure 1. Four-module configuration for UCIe PHY

I. INTRODUCTION

Before diving into the key design considerations for multi-module PHY systems, it's crucial to understand the foundational aspects that ensure seamless functionality and interoperability. Multi-module PHY designs are inherently complex due to the need for consistent performance and synchronization across various interconnected modules. Achieving this requires meticulous attention to detail in both design and verification phases.

Key design considerations for multi-module PHY are as below:

- Maintain same speed and width between individual modules.
- Maintain interdependency between individual modules and coordinate with common RDI (Raw Die-to-Die Interface) and Adapter for state transitions.
- RDI byte-to-Module mapping for differing module-ID connections.

Considering the above design considerations, some of the critical aspects need to be verified. We are focusing on the verification solutions to effectively verify multi-module PHY designs overcoming the challenges due to the complexity and interdependency of the modules by navigating a verification maze and avoid obstacles as showcases in "**Fig. 2**"

Below are key focus areas in verifying a multi-module PHY in UCIe multi-die systems:

- Interoperability Testing:

  Interoperability testing of Design IPs is crucial in the semiconductor industry for development of complex SiPs (System in Package). It ensures compatibility, reduces time to market, lowering development costs. Especially for UCIe, it could be a combination of IPs from multiple vendors. Interoperability testing ensures that these multi-vendor solutions can be successfully integrated, providing more flexibility and options for designers.
- LTSM (Link Training State Machine) states synchronization with other modules during Link initialization and Training:

  Synchronization with other modules ensures robust communication between interconnected chiplets by following a specific sequence of states to achieve link up. LTSM inside each PHY consists of 27 states including the substates covering different intent and verification challenges like sideband interface path initialization and mainband interface path initialization.
- Configurability and Scalability:

  In UCIe, a multi-module PHY offers scalability from x1 to x2 and x4 modules, allowing for the expansion of the interconnect to support a larger number of devices or higher bandwidth requirements. Each module has a unique module ID connection. The module ID connection is important in a multi-module PHY system because it allows the system to identify and address specific modules. Cross-Module connections are allowed.

- Aggregate Bandwidth utilization:

  The aggregate bandwidth utilization in a UCIe Multi-Module PHY (Physical Layer) depends on several factors including the data rate per lane, the number of lanes, number of modules and the efficiency of the protocol.

- Distinct Features for Advance package vs Standard package:

  Based on different applications and use cases, UCIe offers two types of packages i.e. Advanced Package and Standard Package. Advanced package has more pins having clk/valid/lane repairing capabilities whereas Standard package offers width degrade feature verification.

- Clocking and Timing:

  With increasing number of modules, the number of Physical link interfaces also multiplies which comes with challenges of clock synchronization, calibration, deskew and jitter management.

- Error Handling and Recovery during runtime:

  Due to different possible state transitions and multiple pins involved at Physical link interface, possibility of errors are high. Verification needs to ensure that the chiplets are capable of handling different error and recover from it re-achieve the link up state.

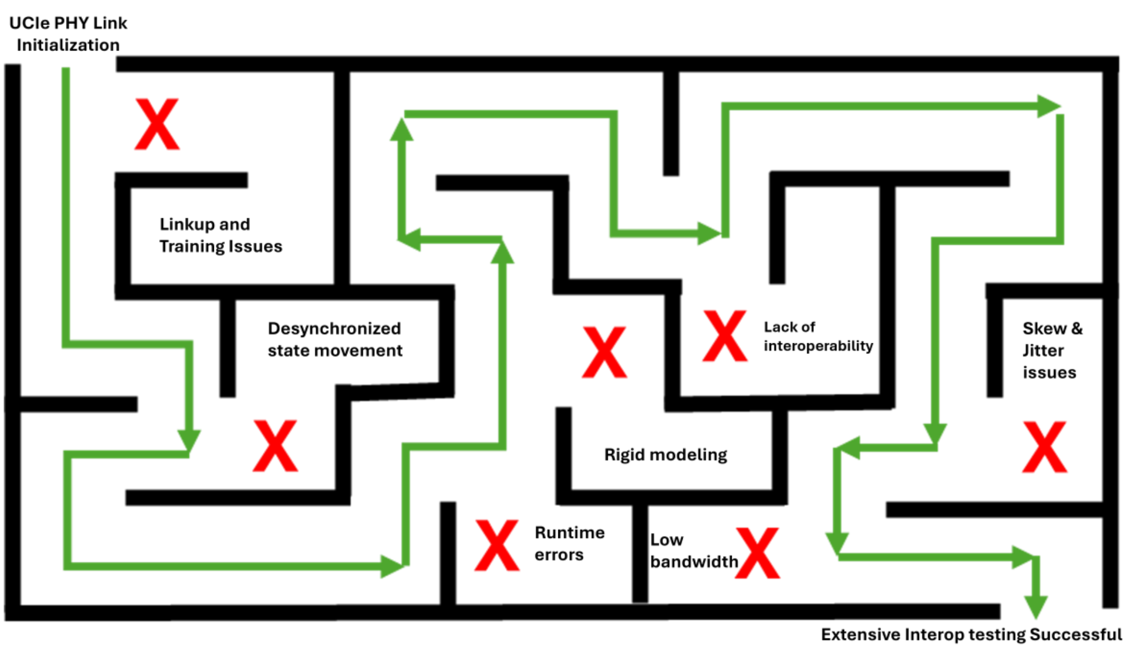

Figure 2. Avoiding obstacles of the verification maze of UCIe PHY

Addressing these verification challenges requires a comprehensive verification strategy involving a combination of simulation, emulation, formal verification techniques. Each of these techniques plays a critical role in identifying potential issues at different stages of the design and development process. Simulation helps in modeling and predicting the behavior of the system under various conditions, while emulation offers a faster, hardware-accelerated environment to validate complex scenarios that might be impractical to simulate fully. Formal verification techniques, on the other hand, provide mathematical proof of correctness, ensuring that the design adheres to its specifications without any corner-case escapes.

Collaboration among IP vendors, chip designers, and verification engineers is essential to ensure the successful integration and validation of UCIe multi-module PHY implementations for multi-die systems.

II. Applications

Multi-module PHY designs are crucial for meeting the ever-growing demands of data-intensive applications to achieve maximum throughput. Data centers, High performance computing (HPC) environments, AI workloads, Automotive electronics needs to be facilitated by multi-module PHY UCIe systems to provide high-speed, reliable, and scalable connectivity. Typically, Advanced package is used for AI accelerators and high-performance computing (HPC) applications and Standard Package is used for Consumer electronics, general-purpose computing.

III. Related Work

Compliance testing and extensive testing ensures that the implementation of UCIe Multi-module PHY adheres to the specification. Different layers of UCIe including the Physical layer are checked independently with a suite of tests for directed and randomized testing. Below example topology as per "**Fig. 3**" explains the Verification IP solution provided to support built in traffic/pattern generation, checkers, and basic common test interface requirements acting as golden die reference.

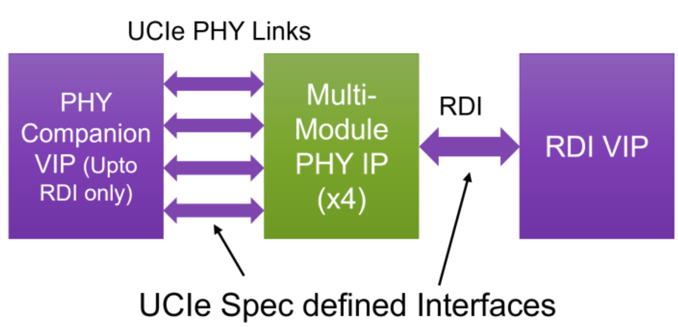

Figure 3. Verification topology for UCIe Multi-Module PHY

IV. Solution Novelty and Preliminary results:

Synopsys UCIe Verification IP provides configurable x1, x2 and x4 multi-module PHY solutions to meet the demanding market design verification expectations. It ensures that UCIe-based systems can efficiently accommodate growth in data traffic, user volumes, or service offerings, thereby supporting long-term sustainability and scalability objectives.

X-factors:

- Easily **scalable** from single to multimodule using configuration settings only and without changing the environment/components.
- Per-module independent **state machine tracking and traffic traceability**.
- Future proof to **accommodate additional modules** based on specification evolution.
- **Easy programming** of modules for differing module ID set up.

Testbench update effort for users to switch from single module set up to multi-module set up: **~1 day.**

Below aids are provided in Synopsys UCIe Verification IP Multi-Module PHY solution to help in debugging complex verification scenarios.

- **Per-module Debug ports** for debugging interface level data integrity issues of **mainband transfers** using Verdi tool waveform as shown below in "**Fig. 4**" and "**Fig. 5**" for both transmit and receive direction.

Figure 4. Tx Debug port example of Synopsys UCIe Verification IP Multi-Module PHY (x8 degraded)

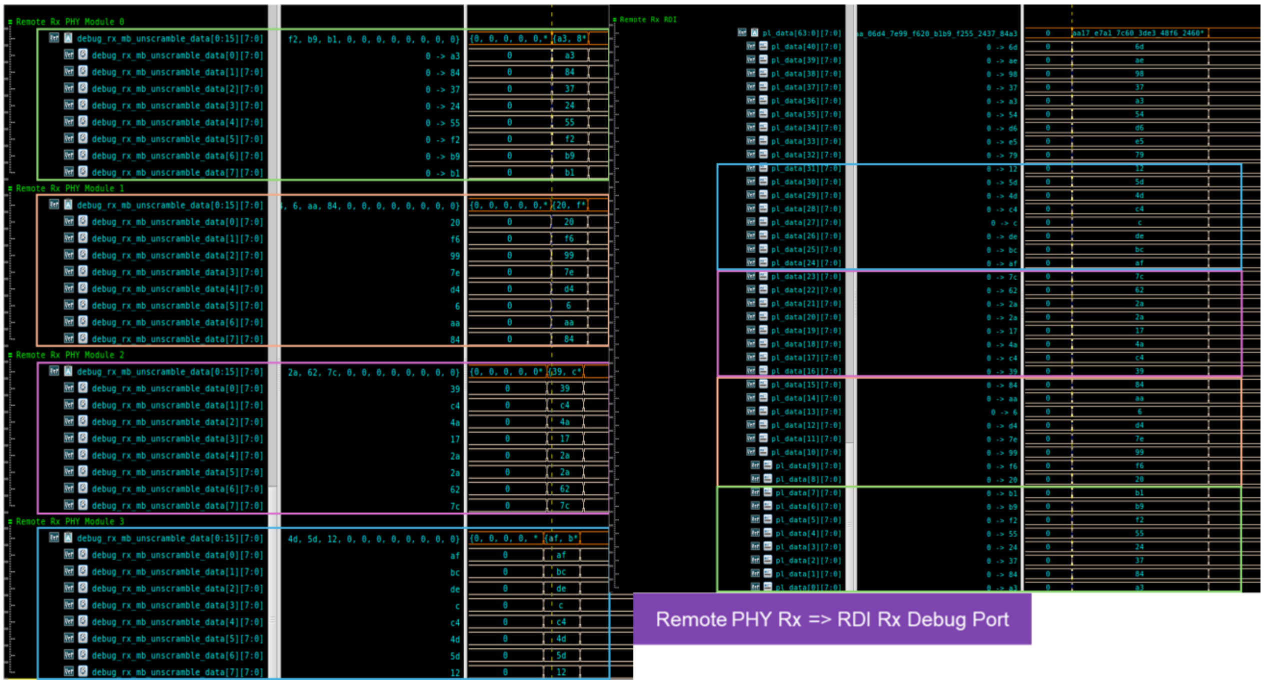

Figure 5. Rx Debug port example of Synopsys UCIe Verification IP Multi-Module PHY

- **Comprehensive per-module traceability** of **sideband transfers** in multi-module PHY as per "**Fig. 6**":

Module 0 SB log

```
Field Description:
START TIME           - Begin time of the transaction in ns.
END TIME             - End time of the transaction in ns.
DIR(Tx/Rx)           - Transaction Direction(Tx/Rx)from VIP perspective.
SRC_ID               - Indicates the source.
DST_ID               - Indicates the destination, where L stands for Local Die and R stands for Remote die
OPCODE               - Indicates about the packet type as well either it carries 32b or 64b of data.
TAG                  - Indicates the completion tag associated with the corresponding request.
MSGCODE              - Indicates the type of Message.
ADDR                 - Indicates address of the request.
MSG_INFO              - Indicates the Message information.
DATA                 - Indicates payload which can be 32 bits or 64 bits wide depending on the opcode ({Phase 2, Phase 3}).
COMP_STATUS          - Indicates the completion status of the request.
BE                   - Indicates byte_enable for the request.
MSG_DESCRIPTION      - Indicates the description of the Msg code and Msg subcode.
MSGSUBCD             - Indicates the sub type of Message.
DATA BIT DESCRIPTION  - Indicates the data field name and its value.
```

START TIME (in ns)	END TIME (in ns)	DIR	SRC_ID	DST_ID	OPCODE	TAG / MSGCODE	ADDR / MSG_INFO	DATA	COMP_STATUS	BE / MSGSUBCD	MSG DESCRIPTION
5009.000000	5089.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5189.000000	5269.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5369.000000	5449.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5371.000000	5449.00000	RX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5489.000000	5569.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5491.000000	5569.00000	RX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5609.000000	5689.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h95	0000	'{}		'h01	SBINIT done req
5611.000000	5689.00000	RX	PHY	PHY(R)	MSG_NO_DATA	'h95	0000	'{}		'h01	SBINIT done req
5729.000000	5809.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h9a	0000	'{}		'h01	SBINIT done resp
5731.000000	5809.00000	RX	PHY	PHY(R)	MSG_NO_DATA	'h9a	0000	'{}		'h01	SBINIT done resp
5849.000000	6049.00000	TX	PHY	PHY(R)	MSG_64B_DATA	'ha5	0000	'{'h201, 'h0}		'h00	MBINIT.PARAM configuration req
5851.000000	6049.00000	RX	PHY	PHY(R)	MSG_64B_DATA	'ha5	0000	'{'h1604, 'h0}		'h00	MBINIT.PARAM configuration req
6089.000000	6289.00000	TX	PHY	PHY(R)	MSG_64B_DATA	'haa	0000	'{'h201, 'h0}		'h00	MBINIT.PARAM configuration resp
6091.000000	6289.00000	RX	PHY	PHY(R)	MSG_64B_DATA	'haa	0000	'{'h201, 'h0}		'h00	MBINIT.PARAM configuration resp

Module 1 SB log

START TIME (in ns)	END TIME (in ns)	DIR	SRC_ID	DST_ID	OPCODE	TAG / MSGCODE	ADDR / MSG_INFO	DATA	COMP_STATUS	BE / MSGSUBCD	MSG DESCRIPTION
5369.000000	5449.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5491.000000	5569.00000	RX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5549.000000	5629.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5611.000000	5689.00000	RX	PHY	PHY(R)	MSG_NO_DATA	'h95	0000	'{}		'h01	SBINIT done req
5669.000000	5749.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5789.000000	5869.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h9a	0000	'{}		'h01	SBINIT done resp
5909.000000	5989.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h95	0000	'{}		'h01	SBINIT done req
5992.000000	6071.00000	RX	PHY	PHY(R)	MSG_NO_DATA	'h9a	0000	'{}		'h01	SBINIT done resp
6119.000000	6318.00000	RX	PHY	PHY(R)	MSG_64B_DATA	'ha5	0000	'{'h1e04, 'h0}		'h00	MBINIT.PARAM configuration req
6183.000000	6384.00000	TX	PHY	PHY(R)	MSG_64B_DATA	'ha5	0000	'{'ha01, 'h0}		'h00	MBINIT.PARAM configuration req
6387.000000	6586.00000	RX	PHY	PHY(R)	MSG_64B_DATA	'haa	0000	'{'h201, 'h0}		'h00	MBINIT.PARAM configuration resp
6424.000000	6624.00000	TX	PHY	PHY(R)	MSG_64B_DATA	'haa	0000	'{'h201, 'h0}		'h00	MBINIT.PARAM configuration resp

Module 2 SB log

START TIME (in ns)	END TIME (in ns)	DIR	SRC_ID	DST_ID	OPCODE	TAG / MSGCODE	ADDR / MSG INFO	DATA	COMP_STATUS	BE / MSGSUBCD	MSG DESCRIPTION
5369.000000	5449.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5491.000000	5569.00000	RX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5549.000000	5629.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5611.000000	5689.00000	RX	PHY	PHY(R)	MSG_NO_DATA	'h95	0000	'{}		'h01	SBINIT done req
5669.000000	5749.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5789.000000	5869.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h9a	0000	'{}		'h01	SBINIT done resp
5909.000000	5989.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h95	0000	'{}		'h01	SBINIT done req
5992.000000	6071.00000	RX	PHY	PHY(R)	MSG_NO_DATA	'h9a	0000	'{}		'h01	SBINIT done resp
6071.000000	6271.00000	TX	PHY	PHY(R)	MSG_64B_DATA	'ha5	0000	'{'h1a01, 'h0}		'h00	MBINIT.PARAM configuration req
6184.000000	6383.00000	RX	PHY	PHY(R)	MSG_64B_DATA	'ha5	0000	'{'he04, 'h0}		'h00	MBINIT.PARAM configuration req
6383.000000	6583.00000	TX	PHY	PHY(R)	MSG_64B_DATA	'haa	0000	'{'h201, 'h0}		'h00	MBINIT.PARAM configuration resp
6424.000000	6623.00000	RX	PHY	PHY(R)	MSG_64B_DATA	'haa	0000	'{'h201, 'h0}		'h00	MBINIT.PARAM configuration resp

Module 3 SB log

START TIME (in ns)	END TIME (in ns)	DIR	SRC_ID	DST_ID	OPCODE	TAG / MSGCODE	ADDR / MSG INFO	DATA	COMP_STATUS	BE / MSGSUBCD	MSG DESCRIPTION
5489.000000	5569.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5573.000000	5652.00000	RX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5652.000000	5733.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h91	000f	'{}		'h00	SBINIT out of Reset
5693.000000	5772.00000	RX	PHY	PHY(R)	MSG_NO_DATA	'h95	0000	'{}		'h01	SBINIT done req
5773.000000	5853.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h95	0000	'{}		'h01	SBINIT done req
5856.000000	5934.00000	RX	PHY	PHY(R)	MSG_NO_DATA	'h9a	0000	'{}		'h01	SBINIT done resp
5893.000000	5973.00000	TX	PHY	PHY(R)	MSG_NO_DATA	'h9a	0000	'{}		'h01	SBINIT done resp
6021.000000	6219.00000	RX	PHY	PHY(R)	MSG_64B_DATA	'ha5	0000	'{'h604, 'h0}		'h00	MBINIT.PARAM configuration req
6062.000000	6261.00000	TX	PHY	PHY(R)	MSG_64B_DATA	'ha5	0000	'{'h1201, 'h0}		'h00	MBINIT.PARAM configuration req
6264.000000	6463.00000	RX	PHY	PHY(R)	MSG_64B_DATA	'haa	0000	'{'h201, 'h0}		'h00	MBINIT.PARAM configuration resp
6301.000000	6501.00000	TX	PHY	PHY(R)	MSG_64B_DATA	'haa	0000	'{'h201, 'h0}		'h00	MBINIT.PARAM configuration resp

Figure 6. Sideband trace log example of Synopsys UCIe Verification IP Multi-Module PHY

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