Beyond Boundaries: Overcoming Chiplet Verification Challenges

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Abstract - –The Universal Chiplet Interconnect Express (UCIe™) offers high-bandwidth, low-latency, power-efficient, and cost-effective on-package connectivity between heterogeneous chiplets. This Die2Die (D2D) Chiplet technology is a paradigm shift in semiconductor design. It provides a modular and efficient approach to building complex systems by quickly assembling pre-verified off-the-shelf components in different technology nodes using UCIe™ interconnect.

While there are several discussions about chiplet strategy to overcome Moore's Law and continue boosting performance, it is important also to discuss the verification challenges and plan necessary changes to meet the verification execution and quality goals.

At the broader level, this presentation addresses three aspects of the chiplet verification challenges.

The first aspect is to build an efficient verification strategy to handle the multi-die system requirements. Performance simulation and analysis is one of the main requirements when considering a multi-die system. This includes deep performance analysis to identify bottlenecks and provide early feedback on latencies and bandwidth to the architecture team. The multi-die system verification presented in this paper includes efficient performance analysis setup, D2D scoreboards to ensure system-level transaction integrity is verified. The system-level portable tests developed can be easily run on multiple engines and topologies, promoting reuse.

The second challenge deals with the automotive verification of UCIe IP. One of the primary concerns of UCIe IP design is to ensure excellent SNR, data rate while keeping the bit error rate as low as possible. This is particularly useful in automotive applications where the margin of error is negligible. The verification environment developed for UCIe 1.1 PHY includes a common setup for the efficient systematic and functional safety verification of UCIe PHY IP, meeting the automotive verification expectations.

The third aspect of the verification challenge relates to the common problem of verification quality and execution quality. However, this common verification challenge is somewhat complex for UCIe and requires an innovative approach. The verification setup presented in this paper includes the UCIe IP in-house SV-UVM verification setup and VIP that is useful in building a scalable, configurable, plug-and-play high-quality verification environment that can be adapted at different levels of abstraction like the layered approach of the UCIe PHY IP, adapter designs.

In summary, the holistic verification approach presented in this paper provides a verification solution to address the chiplet verification challenges of system-level verification, automotive verification, and the requirement of reusable high-quality verification setup for different design topologies.

The verification strategy presented in this paper helped minimize the verification execution time and resulted in finding several design issues before the design release, thereby improving the quality of silicon. It is imperative to share the implementation details of the verification strategy to understand the verification challenges and the approach taken to overcome these challenges.

Keywords – UCIe, Die-to-Die, System Level Verification, Performance

I. ADDRESSING DIE2DIE SYSTEM-LEVEL VERIFICATION CHALLENGES

Building a comprehensive verification setup to overcome the chiplet system verification challenges is a daunting task especially when considering performance analysis and end-to-end data integrity checks. For instance, the path from initiator to target can have many steps with potential “throttle” points that can increase the outstanding transaction count. Data packet assembly and decomposition across the chiplet interconnects can add significant overhead.

The in-house VIP-based solution addresses these challenges by analyzing performance bottlenecks. Figure 1 illustrates the complete system performance and integrity check solution.

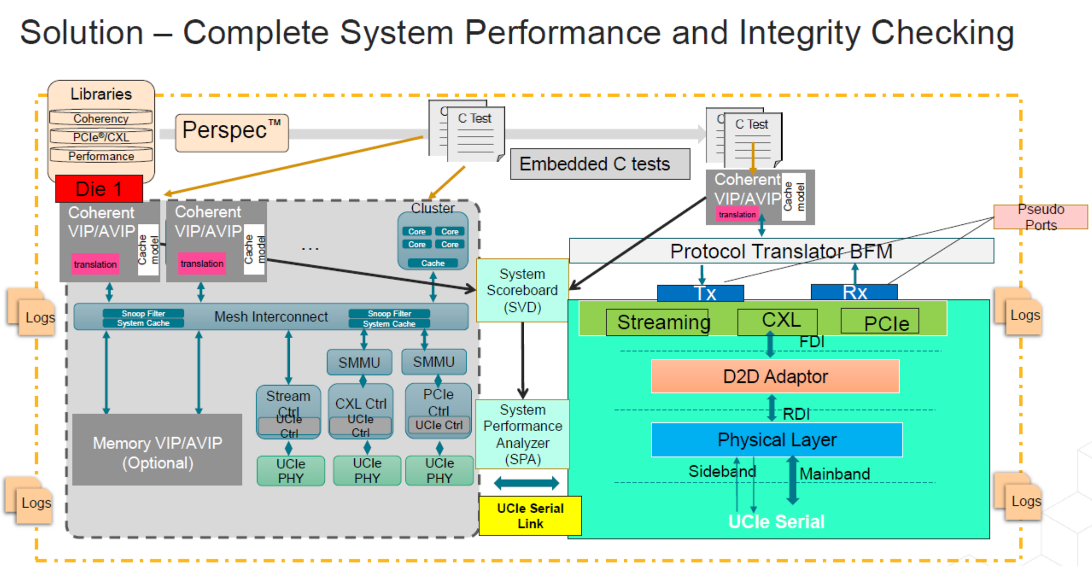

Figure 1: Die-to-Die System Performance and functionality verification environment.

A performance simulation setup using System Performance Analyzer (SPA) analyzes factors influencing latencies. Figure 2 provides useful information for understanding the relationship between latencies, transactions, and bandwidth (B.W) over time.

Reduced B.W and increased latency, as well as outstanding transactions from the plots, indicate that the system is overloaded by the specific test stimulus/transaction. Heuristics provides insight into real design performance compared to the theoretical performance numbers. This can then be used to update the design as per the end application. Reduced B.W utilization with low chain length indicates the controller design is not processing the incoming request efficiently and requires design analysis.

Figure 2: Bandwidth, Latencies, and Outstanding transaction plots over time

This system analysis allowed bottlenecks to be identified and investigated early in the design cycle.

Apart from performance requirements, the verification setup is also used to perform system-level testing thereby ensuring correct functionality of the device.

II. MEETING AUTOMOTIVE VERIFICATION REQUIREMENTS WITHOUT EXPONENTIALLY INCREASING EFFORT

The UCIe 1.1 standard is extended to include automotive usage. In general, the automotive design cycle is very long. Chiplets present an attractive solution for reducing this long development cycle by enabling the assembly of multiple chips. However, the challenge lies in seamless safety verification coupled with the functional and performance verification of chiplet designs. Meeting safety verification requirements can be time-consuming if not planned during the early phase of verification environment development.

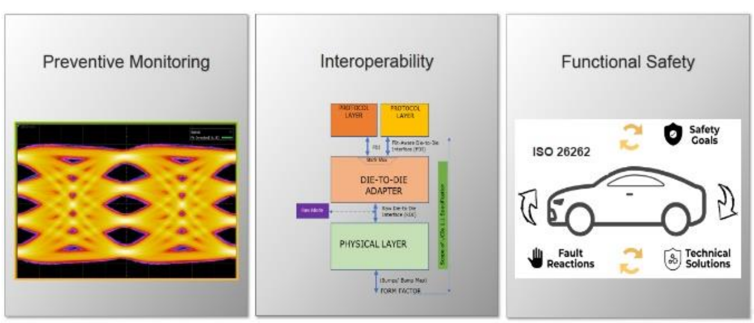

Figure 3: Focusing on Preventive Monitoring, Interoperability & Functional Safety

The UCIe 1.1 automotive enhancements are all verified using the common SV-UVM testbench. The automotive feature verification includes:

1. Preventive monitoring using registers added in UCIe to capture eye margin information and per lane error counter with the ability to send interrupts.
2. Interoperability, multi-protocol support with a streaming protocol using the D2D adapter and enabling the co-existence of multiple protocols.
3. Mainband (MB) CRC, retry mechanism, and sideband safety features such as parity, and newly added CRC.

The verification setup for UCIe PHY IP encompasses automotive safety verification for specified ASIL requirements. Safety features/mechanisms such as CRC on sideband, timeout in low-power states, high/low priority interrupts, parity, data/valid lane eye margin information capture in link health register are all part of the design for both systematic functional verification and qualitative direct fault injection verification to validate the failure mode and safety mechanism. Functional Safety verification is architected along with nominal verification and not added later. The same verification setup is used as is with additional configurable, lightweight testcases for safety verification. This minimized changes to the Design Verification (DV) environment.

III. Addressing the Common Problem of Improved Execution Efficiency with Reuse and Improving the Quality of Deliverables

This common problem is somewhat challenging for UCIe and requires careful consideration when developing a verification strategy. The first “section a” shares information on building an effective design verification environment and methodology to seamlessly support multiple design requirements with minimal effort:

i) IP/Subsystem (SS)/Back2Back Chiplet environment
ii) Designs with single (x1) or multiple (x2, x4) PHY and Adapter
iii) Automotive requirements
iv) New requirements with incremental spec update: UCIe 1.1
v) Advanced Package (AP)/Standard Package (SP) designs

The verification challenges in general are not new, as configurable and scalable systems have been used for long. However the interesting verification challenge for chiplet design is to effectively build a common framework to verify all the above requirements together in a scalable way with minimal effort and high confidence for signoff.

The second part, “section b,” demonstrates a verification approach to overcome gaps with analog and digital verification.

Section a. Effective design verification environment and methodology: Minimize development time and improve the execution efficiency.

The UCIe system brings in a new level of interdependencies that adds to the verification complexity. Each die must be thoroughly verified at the IP, subsystem, and the entire D2D system. A high-quality verification environment is a key enabler for meeting the verification goals for different design topologies. The verification environment is built in such a way that it allows easy configurability to support all the requirements as listed above. The overall verification environment can be configured and reused for new UCIe designs in standard or advanced packages in a matter of couple of weeks, instead of the standard testbench bring-up time of couple of months. This not only minimizes development effort but also supports the debug effort in finding the design issues instead of DV environment issues.

Figure 4 represents a complete pictorial view of the PHY IP level Design Under Test (DUT) with the verification environment. The configurable DV environment includes a local Die that represents the Adaptor UVC functionality, while the remote DIE UVC has the complete representation of the PHY IP DUT. It includes a serial external interface UVC, mimicking the LTSM functionality, as listed in the UCI design specification for initialization bring-up. The built-in intelligence with the response handler in UVC enables a handshake with the DUT as per LTSM. The other functionalities of the DUT, such as decoder, serialization, and deserialization, are also implemented in the remote Die UVC, facilitating a complete exhaustive verification of the DUT.

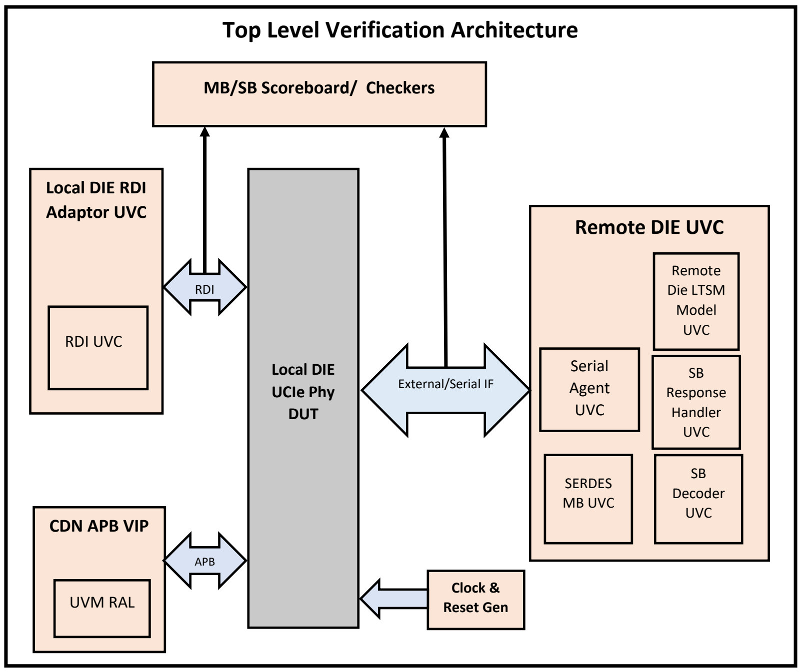

Figure 4: Top Level Verification architecture

As Figure 5 shows, the UVM verification environment provides easy reuse for the UCIe PHY Standard Package design versions or new Advanced package designs with minimal changes.

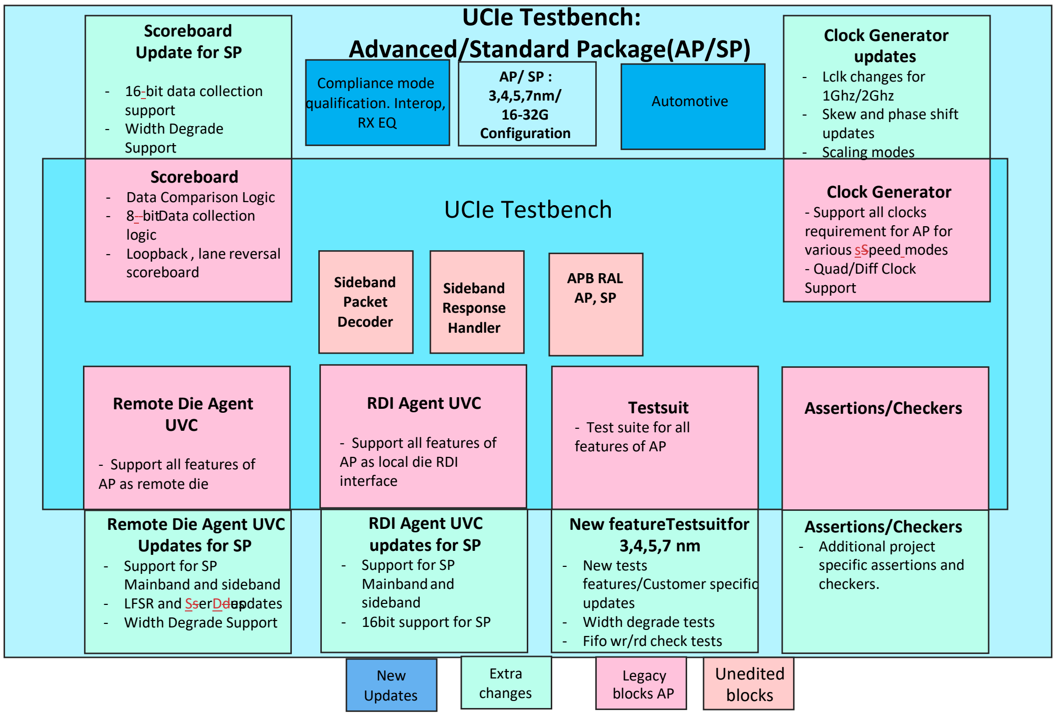

Figure. 5: Configurable UCIe™ Verification Setup

The configurable UCIe verification setup enabled optimized effort and improved verification productivity. Best design verification practices are used in creating a framework for a configurable, reusable verification environment. A large part of the verification code base is reused with minimal changes for design verification. Any new updates can be incrementally added with minimal update/impact to the existing setup.

The verification environment also supports UCIe PHY IP and subsystem topologies for verification, as shown in Figure. 6

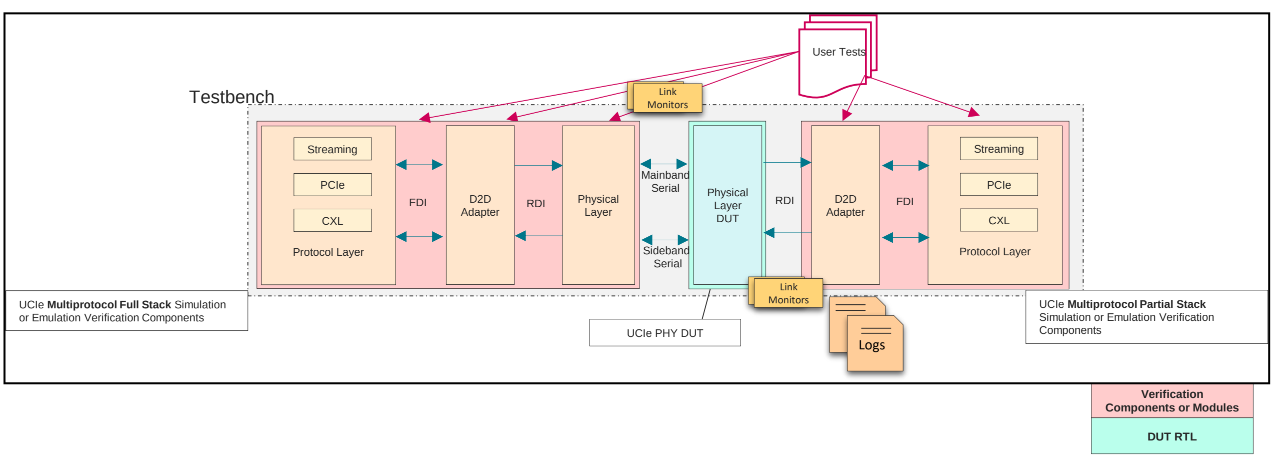

Figure. 6: Standalone IP verification and Subsystem level verification with Coherent, Non-Coherent protocols.

Besides IP, Subsystem(SS) design verification setup; the same common testbench is utilized for back2back multimodule subsystem Chiplet configuration verification as shown in Figure. 7

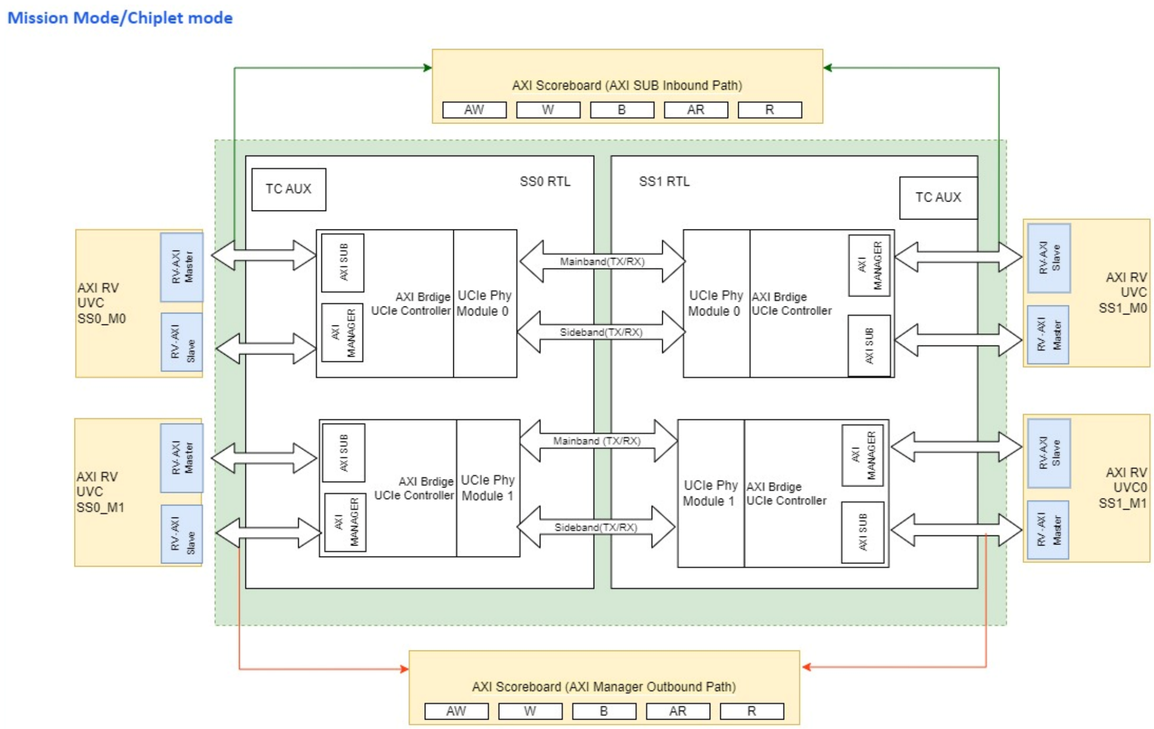

Figure. 7: Example of back2back multi-module Subsystem configuration

This configurable and scalable verification strategy enabled the verification team to not only minimize development effort but also reduced the overall debug effort, which otherwise consumes most of the verification cycle.
Besides reuse, careful consideration is also given to the **simulation performance** (minimizing the simulation run time). For example, the UCIe PHY standalone IP LTSM takes significant simulation time. Test bench optimization and a review of delays improved the simulation performance as shown in Table 1.

Sno	LTSM state	Simulation Time(%)	Optimization(%)
1	SBINIT	~1us(10%)	~800ns(10%)
2	MBINIT	~1ms(35%)	~0.9us(35%)
3	MBTRAIN	~1.8ms(50%)	~1.2ms(50%)
4	LINKINIT	~600ns(5%)	~300ns(5%)
	Overall	**2.96ms(100%)**	**2.13ms(100%)**

Table 1: Testbench optimization for various LTSM states

Similar optimization was done in other parts of the testbench for different design topologies. Simulation tool (profiling) capabilities such as "IPROF" further aids in improving the simulation performance. An emulation solution setup with emulation-friendly analog models has also been developed to support faster system-level real testing due to longer simulation times with traditional RTL simulation.

Section b. Overcoming gaps in analog mixed-signal design verification for a high-quality design signoff:
UCIe PHY has a significant analog design potion. Minimizing gaps or functional issues between analog and design modules is important.
Due to the long simulation runtime, it is common practice to use models to represent an analog schematic for verification. However, if the quality of the model is incomplete, the design will be of low quality.
Initial verification starts with a High-Level Behavioral model (HLM). Later, as the schematic is developed and the design environment stabilizes, more detailed System Veilog (SV) Wreal models are used.

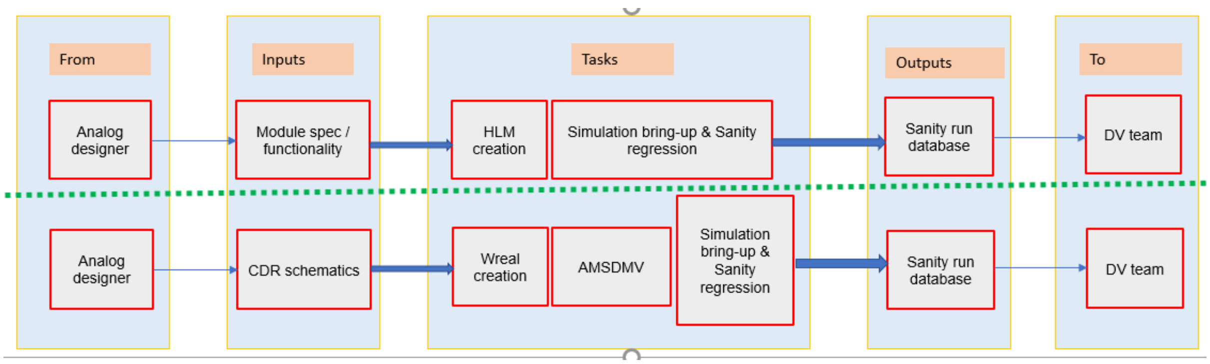

Figure. 8-: High-Level Behavioral model (HLM) creation from a set of inputs

The following listed qualification process is followed, and quality checks are implemented to **maintain the quality of analog and digital verification**:

- AMSDMV tool is run to find model issues/differences by using the same test scenarios as input for schematic and models.
- Model inaccuracies are addressed for completeness [1]

- A new approach like digital verification plan (Vplan) is used to develop AMS Vplan ensuring there are no gaps between analog and digital IP designs. Models are implemented with inbuilt switches that are used in the digital DV environment to verify critical analog functionalities.

SNo	Features/Functions	MLM Switches	Description
1	DCC	DV_**TX/RX_CLOCK/VALID/DATA***_EN_DUTY_DISTORT, DV_**TX/RX_CLOCK/VALID/DATA***_DUTYCYCLE_TARGET	Generate distortion on the TX side. Apply Duty Cycle Distortion on the TX, RX side of EXT interface
2	DESKEW	DV_**TX_CLOCK/VALID/DATA***_DESKEW_CAL_TARGET **RX_SKEWON**	Generate distortion on the TX side Apply Skew on the TX and RX side of EXT interface
3	PLL	DV_CMN_**BANDGAP**_CODE DV_CMN_**VCOCAL**_CODE	Apply offset to verify bandgap calibration Apply offset to verify VCO calibration

Table 2-: Sample AMS Vplan

Apart from model usage, vcd-based approach is also used [2] to uncover system-level issues as co-simulation at the system-level is time consuming and difficult. The steps taken to close the verification gaps between analog and digital design issues resulted in finding corner case bugs much earlier in the design process.

IV. Conclusion and Benefits

Chiplet verification requires a novel thought process. The robust, high-quality verification setup presented in this paper meets the requirements for Chiplet verification by ensuring Quality of deliverables and Execution quality without increasing cost.

The main benefits of the UCIe chiplet verification presented in this paper are as follows:

1. Provided early feedback to the architecture team for design changes based on system performance verification at the chiplet level. The design bottlenecks were identified and investigated early.

   This avoided late architecture changes in new Chiplet designs.

2. Developed common framework for reuse of test environment/testcases across IP/SS for functional verification, safety verification, and performance simulation.

   This minimized effort; for example, automotive verification effort was reduced to **1.3X** instead of 2X. Common configurable testbench setup and test cases also drastically reduced verification development efforts for single or multiple PHY modules or Advances/Standard package designs. The overall environment bring-up time for new designs was reduced from ~1.5 months to **2 weeks**.

   Simulation run time was also improved for design sections such as LTSM, and in general, with the test bench, models, profiling/analysis and subsequent updates.

3. Improved the quality of design. Found several design issues before the release by using advanced dynamic and formal verification approach with good signoff criteria (includes process improvement such as Feature Analysis meeting /review for signoff of every new feature, exhaustive verification with AMS VPLAN stressing the digital-analog verification with configurable switches).

Acknowledgements

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References

[1] An Approach to Overcome Modeling Inaccuracies for Performance Simulation Signoff of High-Speed SerDes.

[2] Overcoming challenges of verifying complex mixed signal designs.

[3] UCIe™ specification.