

# Protocol Environment: A Dynamic approach to Enable Multi- Protocol UCle Design Verification

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**Abstract** - In recent years, the chip design industry has witnessed a significant trend, the increasing development of chiplets. In response to this shift, leading-edge semiconductor companies have collaboratively formed a consortium and developed a new open standard for chiplet interconnects, known as Universal Chiplet Interconnect Express (UCIe). This standard represents a major advancement in chiplet integration and defines a pathway from a monolithic chip architecture to chiplet based systems. The UCIe specification, at its core, defines a layered protocol that utilizes interfaces to manage and co-ordinate various interconnect requirements, delivering a comprehensive set of features. While the specification officially supports standardized protocols such as PCIe and CXL, it is designed with flexibility in mind and includes provisions for raw or streaming protocols, allowing for the integration of additional protocols beyond PCIe and CXL. In this paper, we introduce a solution designed to validate systems incorporating one or more of these protocols operating over the UCIe interconnect. It facilitates verification of protocol implementations within the UCIe ecosystem, ensuring robust interoperability and functionality across different protocol layers.

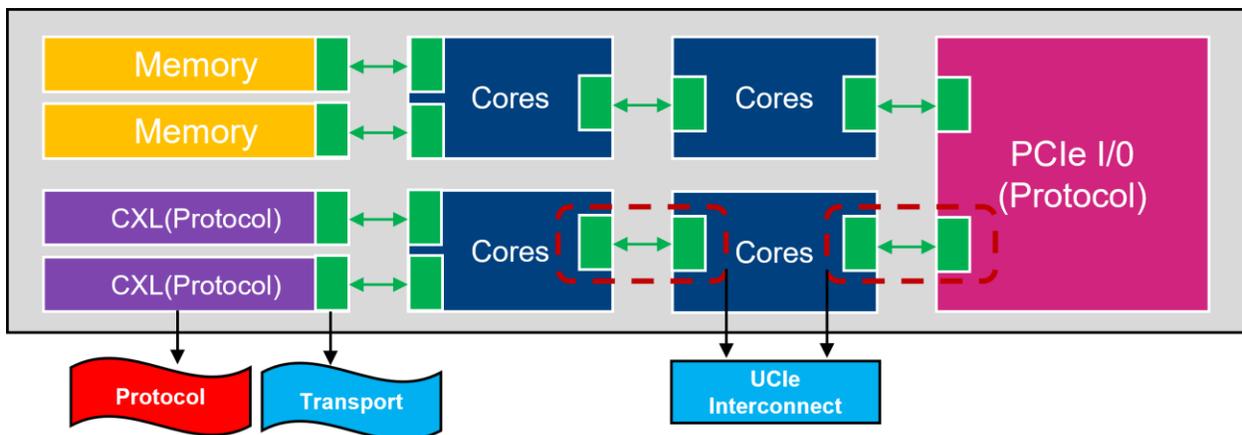


Figure 1: Chiplet based system utilizing UCIe as transport layer



## I. INTRODUCTION

UCIe (Universal Chiplet Interconnect Express) is an open standard designed for on-package interconnection, facilitating the integration of multiple semiconductor dies within a single package. Its primary goal is to foster a dynamic ecosystem that supports disaggregated die architectures, enabling them to be interconnected via UCIe. UCIe supports a range of protocols, including PCIe, CXL, and streaming formats, as well as a raw format that can be adapted to any chosen protocol, provided both ends are compatible with its shared physical and link layers. This flexibility ensures that UCIe can accommodate various communication needs and architectural configurations.

UCIe supports a broad array of usage models, initially integrating protocols such as PCIe, CXL, and streaming formats. The inclusion of PCIe and CXL—both extensively utilized protocols—facilitates enhanced on-package integration by replacing traditional PCIe SERDES PHY and PCIe/CXL LogPHY interfaces. Moreover, UCIe's support for streaming protocols allows them to utilize the Link Level Retry feature of the UCIe Adapter, ensuring reliable transport for protocols beyond PCIe and CXL. This capability broadens UCIe's applicability and reliability in diverse interconnect scenarios.

UCIe encapsulates multiple application protocols such as PCIe, CXL or any other Streaming Protocol (AXI, CHI or user proprietary protocol). It allows application-level workloads to be driven as standard flit formats which is agnostic to any specific protocol specification. Thus, UCIe provides transport mechanisms which is protocol agnostic and generic in nature (e.g., PCIe non-Flit mode packets are transported using CXL.io 68B Flit Format)

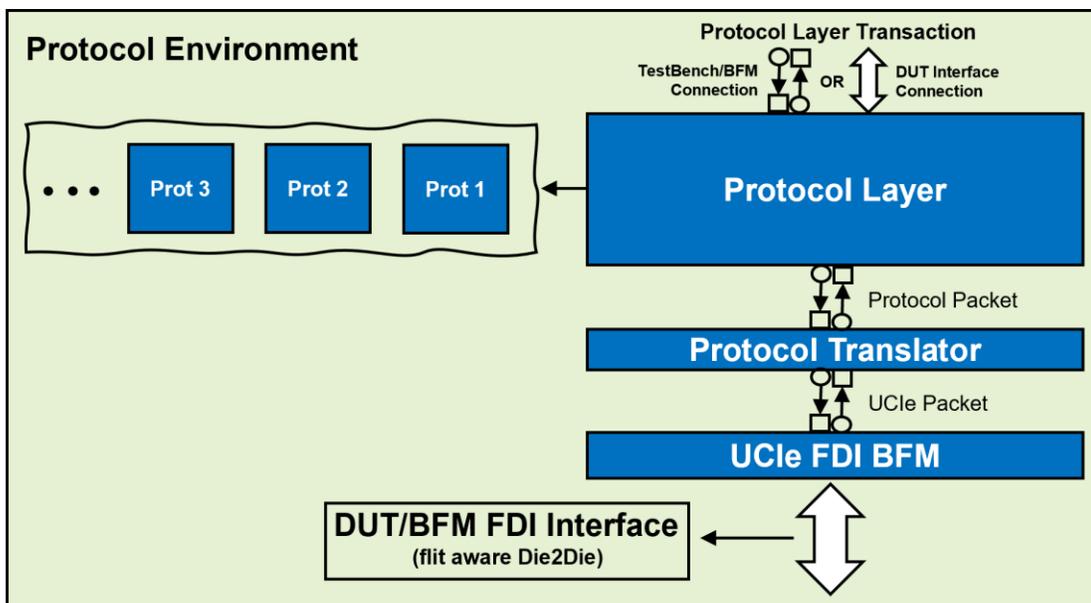
Since UCIe has the capability to carry multiple protocols, it creates a need of a generic verification solution which can cater to different verification requirements of users to validate multiple subsystems such as CXL over UCIe, PCIe over UCIe, AXI over UCIe.... We have identified a way, where we can leverage these UCIe feature set and create a functional verification ecosystem with a top-level environment known as **Protocol Environment**, capable of testing designs where various protocols interact over the UCIe interconnect.

The key advantages of this include:

- **Protocol-Agnostic:** Designed to accommodate any future set of protocols. The solution is adaptable to evolving standards.
- **Multi-Stack Support:** It leverages UCIe's Multi-Stack capability, allowing multiple protocols to operate over a single UCIe transport.
- **Scalability:** The architecture's consistent configuration facilitates easy scaling to support additional protocols.
- **Simplified Maintenance:** A uniform architecture across protocols reduces complexity and maintenance efforts by minimizing the number of files.
- **Generic Behaviour:** The system's design ensures broad applicability and flexibility.

## II. RELATED WORK

**Protocol Environment: a Versatile Protocol Integrator**, provides a comprehensive solution for integrating various protocols with UCIE as the transport layer. It serves as a versatile verification platform designed to connect industry-standard protocols with UCIE's D2D (Die-to-Die) and physical layer verification components. This enables complete stack verification, ensuring that protocols operate seamlessly over the UCIE interconnect. It facilitates thorough testing and validation by bridging the gap between protocol-specific requirements and UCIE's transport mechanisms, offering a robust framework for verifying end-to-end functionality within multi-die systems.



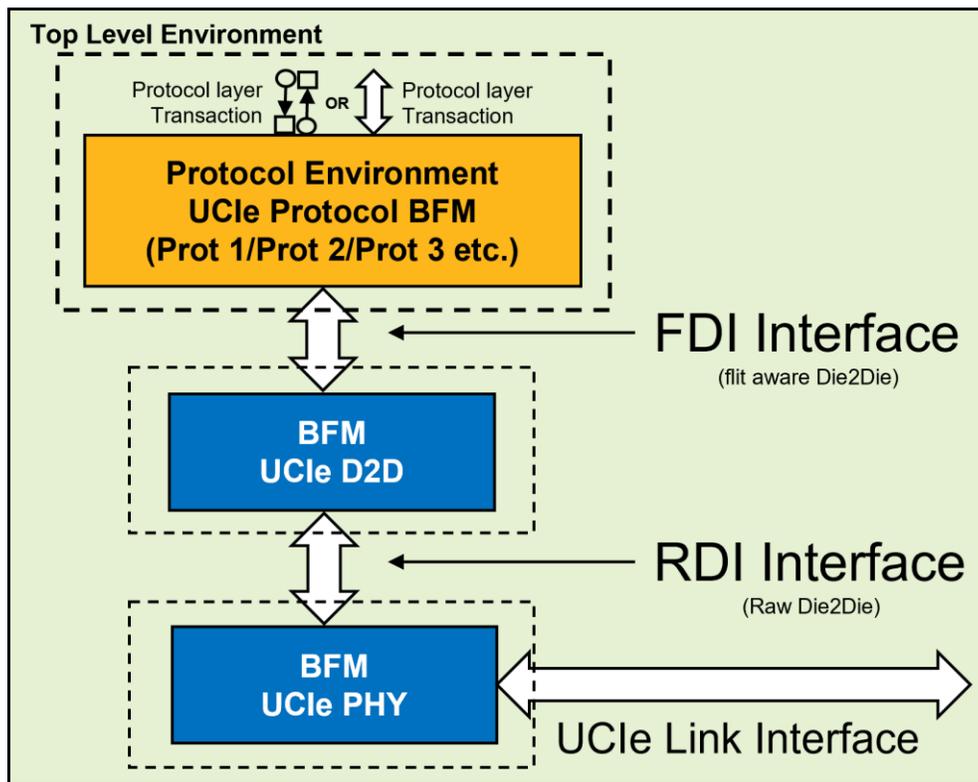
**Figure 2: Protocol Environment Block Diagram**

The verification solution consists of three primary components: the Protocol Agent, a Protocol Translator and the UCIE FDI Agent. These elements collectively form the core of the verification framework:

- **Protocol Agent:** This component represents the protocol-specific BFM (Bus Functional Model). It can be any protocol supported over the UCIE interconnect, such as PCIe, CXL, AXI, CXS or any proprietary protocol. For protocols like PCIe or CXL, which typically have their own PHY layers, the instances are configured without these native PHYs. Instead, UCIE's PHY is employed to transport Protocol data across the interconnect to the partner chiplet, as UCIE itself handles the physical layer.
- **Protocol Translator:** This is responsible for converting data between the protocol-specific domain and the UCIE domain. This translator facilitates the data conversion, aligning it with the selected protocol and flit format.

- UCIe FDI Agent:** The FDI Agent interfaces between the protocol Layer and the UCIe D2D Adapter Layer, adhering to the scope defined in the UCIe base specification. It facilitates the interaction and data flow between the protocol-specific verification and the UCIe interconnect.

In a comprehensive full stack verification framework, this environment approach is strategically positioned as illustrated in Figure 3 below. The utilization can be as simple as a protocol switch or a parameter within the BFM configuration, specifying the protocol in use. Subsequently, one can provide traffic that is compatible with the selected protocol. This traffic is directed through environment, which manages the interaction between the protocol-specific data and the UCIe D2D (Die-to-Die) adapter. From there, the traffic is transmitted across the link through the UCIe PHY (Physical Layer), enabling thorough verification of the entire stack's functionality and interoperability with the remote DUT or remote partner.

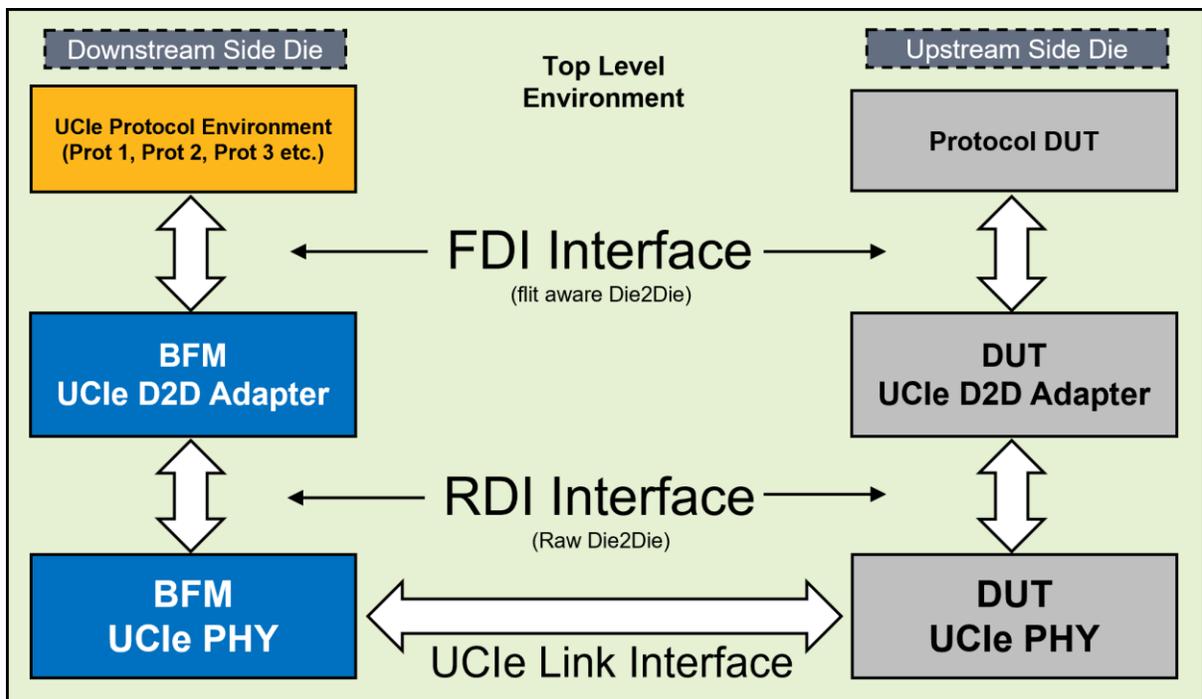


**Figure 3: Protocol Environment in a Top-level Test Environment**

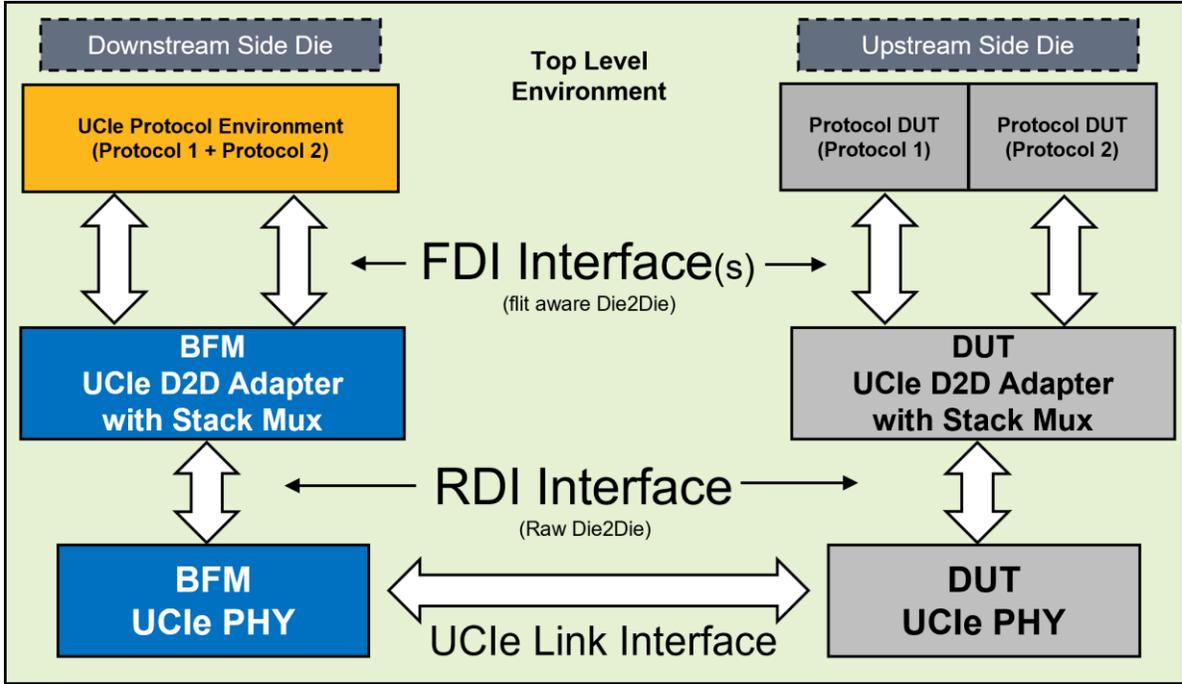
### III. SOLUTION NOVELTY

Initially, we discussed about the capabilities of UCle, highlighting its ability to function as a Multi-Stack Protocol. In simple terms, Multi-Stack means that multiple protocols can simultaneously utilize the same UCle transport infrastructure. The solution scales to verify multi-stack adapter designs as is illustrated in “**Figure 4 & Figure 5**” below. It demonstrates that this top-level environment approach can support both modes of UCle operation i.e., **Single Stack and Multi-Stack modes**.

In Single Stack mode, a single protocol layer is instantiated over the UCle transport, providing a comprehensive full-stack verification solution. Conversely, in Multi-Stack mode, two distinct protocols are concurrently managed over the same UCle transport, offering a seamless full-stack verification solution. This flexibility underscores the versatility of this dedicated environment approach, in accommodating different protocol configurations while maintaining robust verification capabilities.

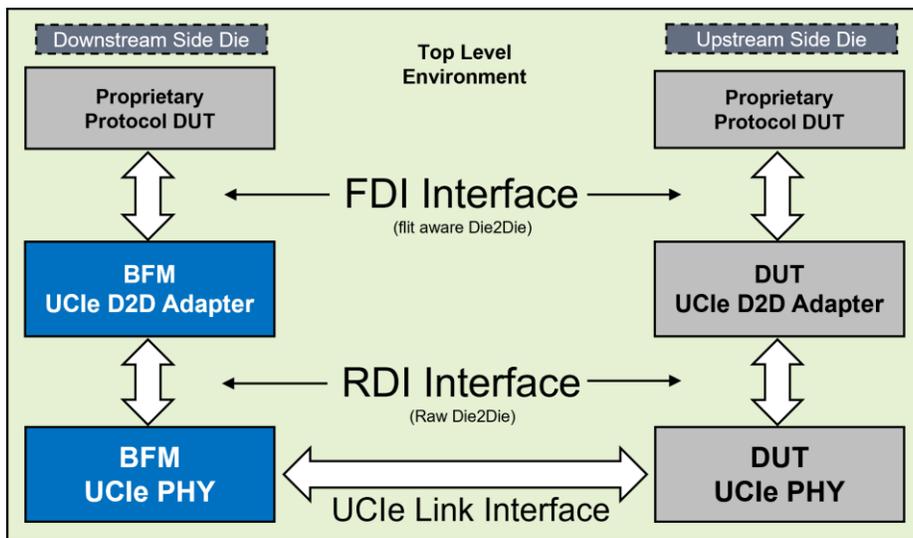


**Figure 4: UCle Protocol Environment in Single-Stack topology**



**Figure 5: UCle Protocol Environment in Multi-Stack Topology**

**Proprietary Protocol Topology**, the top-level environment can include any proprietary protocol layer DUT to connect with the verification solution thus allows full-stack verification in-case of non-standard protocols.



**Figure 6: Proprietary Protocol DUT Topology**







## V. SUMMARY – THE FUTURE OF MULTI-DIE

**Protocol Environment** has ability to integrate and support new protocols, thereby enhancing its utility and applicability across diverse use cases. This adaptability is crucial for broadening its market reach and accommodating evolving technological requirements.

The potential for protocol integration over the UCIe interface is expanding as the industry increasingly adopts multi-die architectures. The variable representing the number of supported protocols, is not fixed; it is dynamic and subject to growth. As the number of protocols, increases, so too does the capacity and functionality of the Protocol Environment. This growth trajectory highlights the evolving nature of protocol support within UCIe, reflecting the broader trend towards more complex and versatile multi-die designs in contemporary semiconductor technologies.

At present, the UCIe standard stipulates that a single UCIe PHY Link interface can support either one protocol (Single-Stack) or two protocols (Multi-Stack) concurrently. However, the UCIe consortium can revise and potentially expand these limits, as has been observed with other standards. The solution is designed with flexibility in mind, enabling us to scale and adapt to any future increase in the number of supported protocols as the standard evolves.

## ACKNOWLEDGMENT

Special thanks and heartfelt acknowledgment go to Narasimha Babu G V L, Scientist at Synopsys SDG and a member of the Technical Program Committee for DVCON India 2024. His invaluable contributions included reviewing both our paper and presentation on this topic, as well as providing comprehensive guidance throughout the entire process. His support was instrumental in helping us achieve these significant milestones.

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