Power Dynamics: Shaping the future of the data centric era

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Agenda

- Why has power become important?
- Traditional methodologies and flows
- Siemens power solution
- Siemens power solution technical overview

Food for thought

Are you running end-user software or target applications for power analysis?

Are you doing power analysis at block-level or chip-level or system-level?

Have you verified that all user defined clock gating cells are saving power rather than wasting energy?

Are you confident you met your power goals before silicon tape-out?

What happens next if you exceed your thermal budget?

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Why has power become important?

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Semiconductor industry: at a glance

Data-centric Era

Mobile Era

Computer Era

1960 1980 2000 2020 …..

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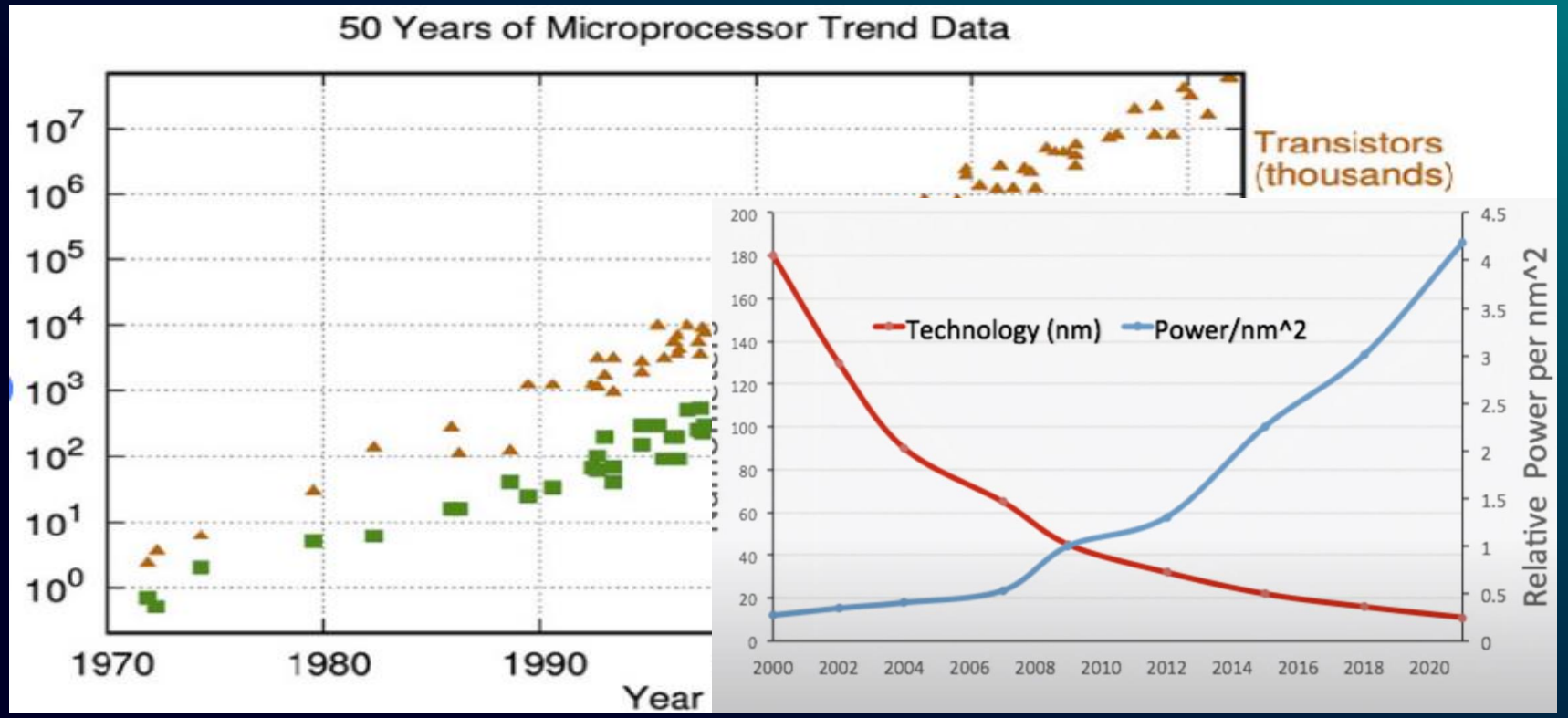
Semiconductor industry: at a glance



1960 1980 2000 2020 …..

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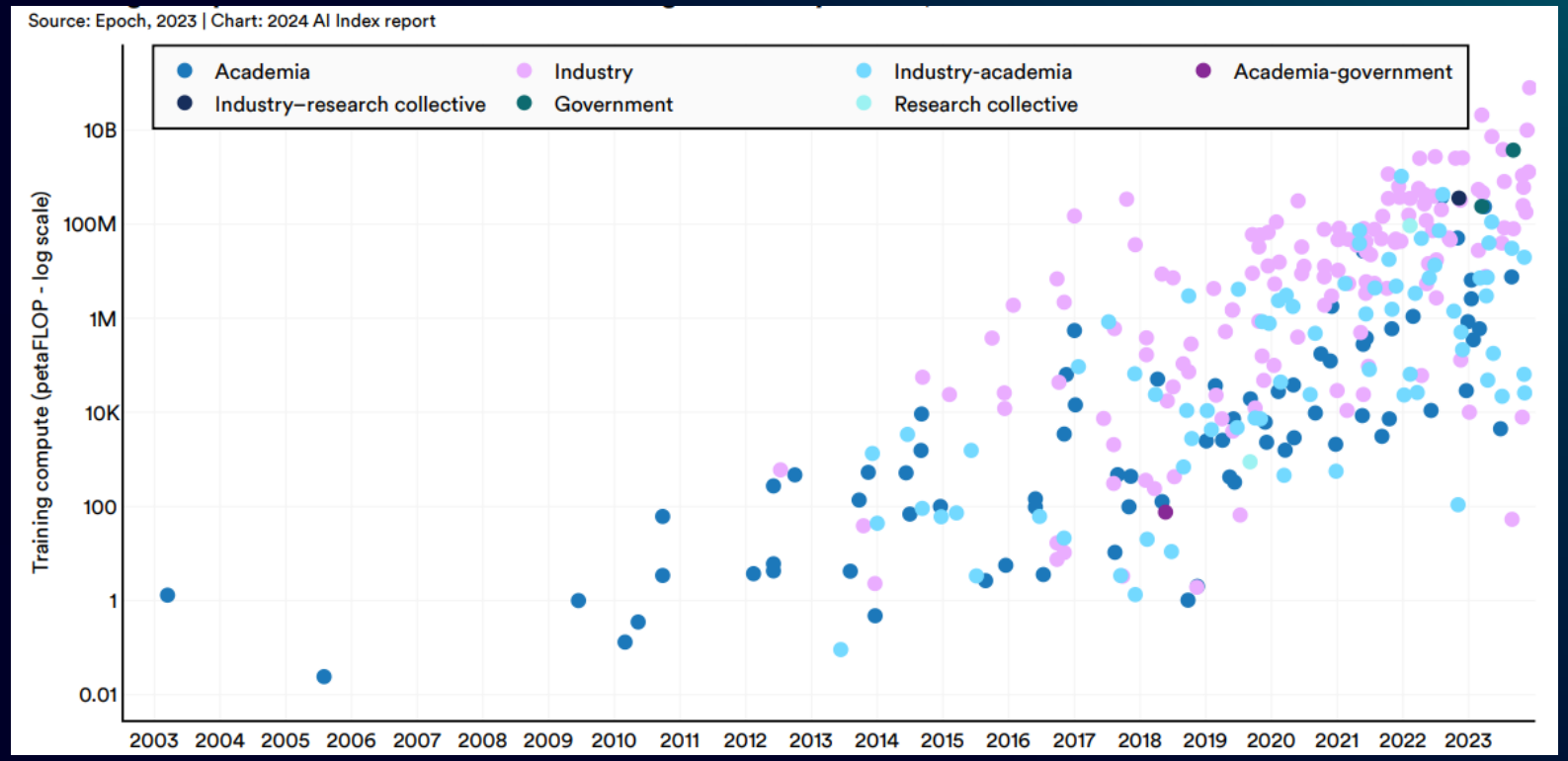
Data centric era is synonymous with AI



Massive computations

Maximum parallel processing (no idle phase)

High bandwidth memories

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Traditional methodologies and flows

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Traditional power flow and challenges

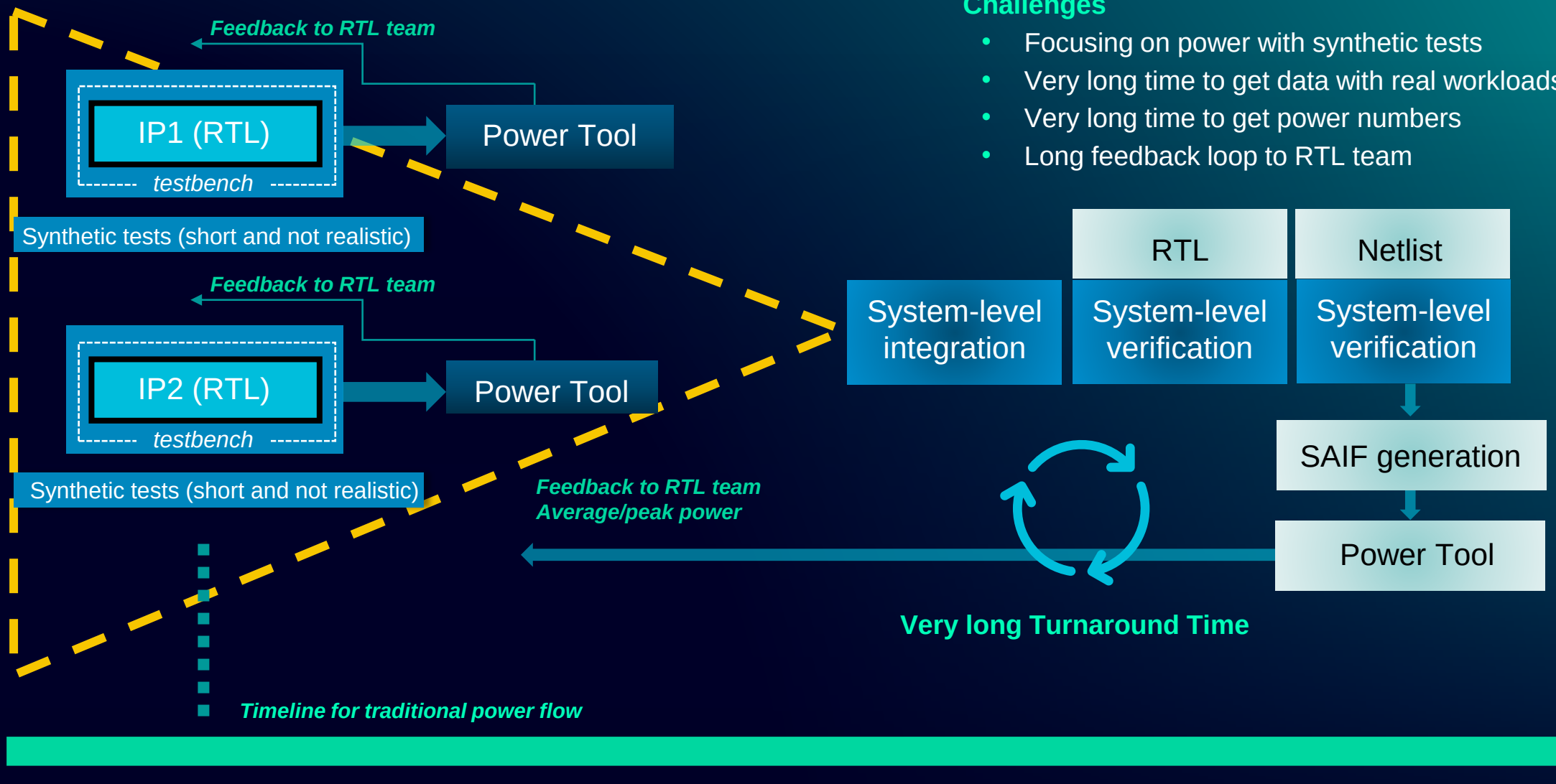
Power Flow

- Power team develop synthetic test cases representing best /worst case scenarios
- Block-level power is calculated using Power tools
- Aggregate chip-level power is calculated by adding power of all blocks

Potential Challenges

- You may over or under design chip for power, which can cost money
- When chip is used in targeted application may consume different power
- Does not enable power / performance tradeoff analysis/ optimizations

Traditional power flow



Challenges

- Focusing on power with synthetic tests
- Very long time to get data with real workloads
- Very long time to get power numbers
- Long feedback loop to RTL team

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Siemens power solution

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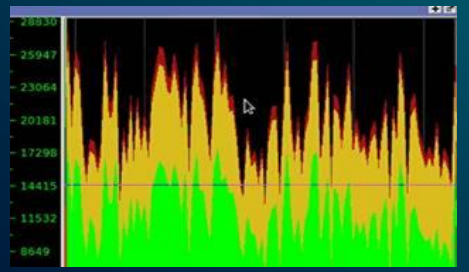
Siemens power solution delivers

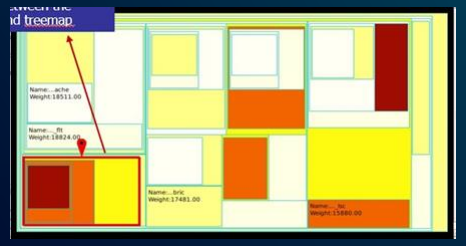
- Accuracy to make data driven decisions – within 5% accuracy of power tools
- Speed to run SW applications and workloads – billions of cycles
- Scalable platform to run IP, chip, and system level – power campaigns
- GUI-based analysis for power issues and chip heatmap analysis
- Actionable matrix and dashboard for early HW / SW power optimizations
- Integration with leading industry power tools

Siemens Veloce Strato CS platform offers efficient solution

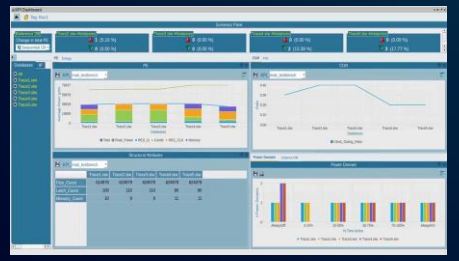
- Capacity: 40MG to 44BG
- Cycle accurate Power (full visibility)
- Fast power data generation
  (2 billion cycles in one hour)



Cycle accurate power profile



Chip Heatmap



Power Dashboard

Full integration with PowerPro (Siemens), PowerArtist (Ansys), PrimePower (Synopsys)

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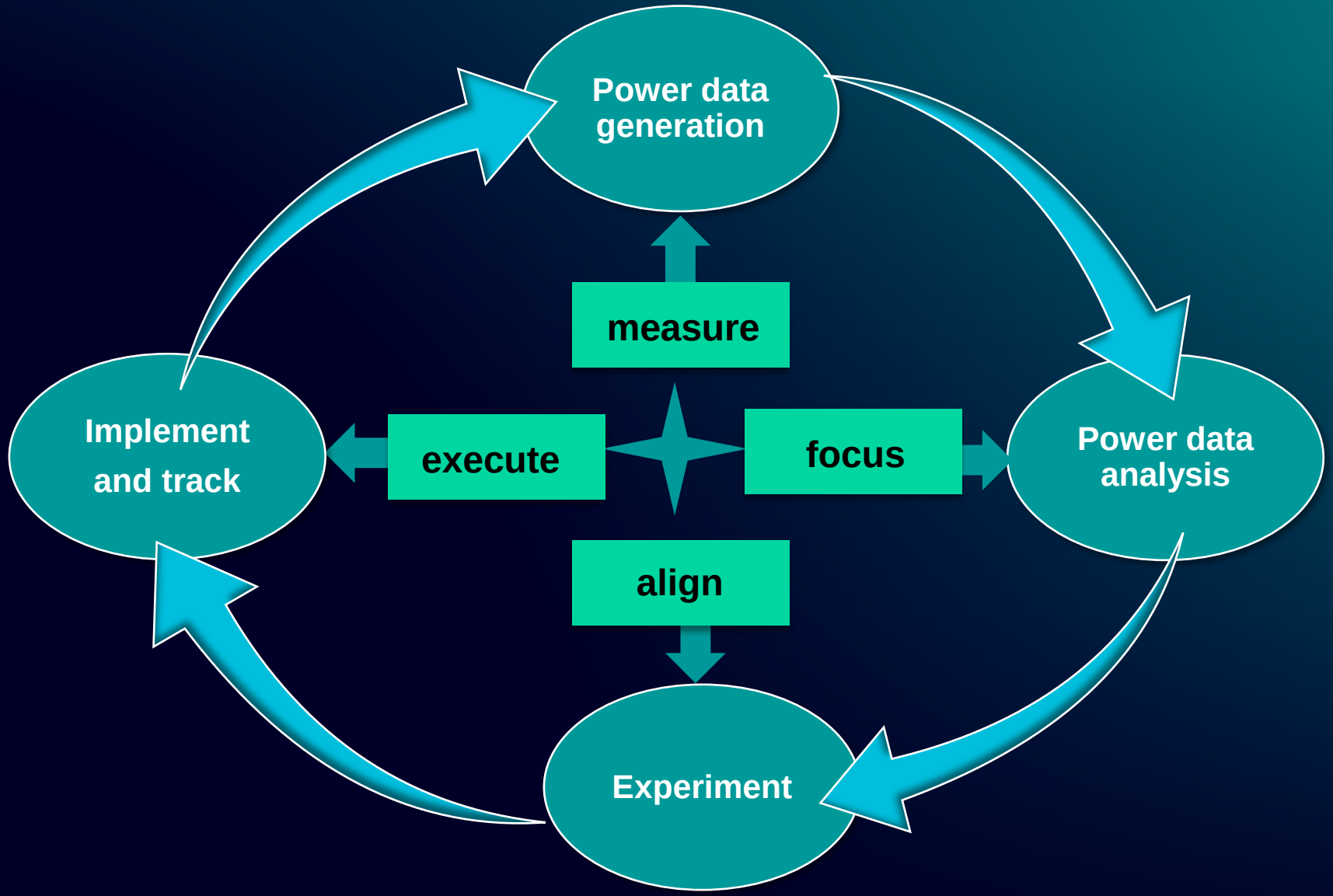
Shift-left flow for power analysis



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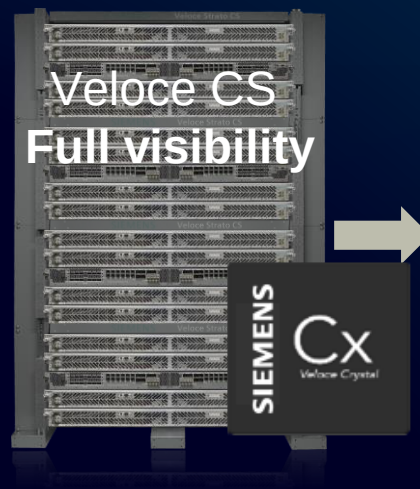
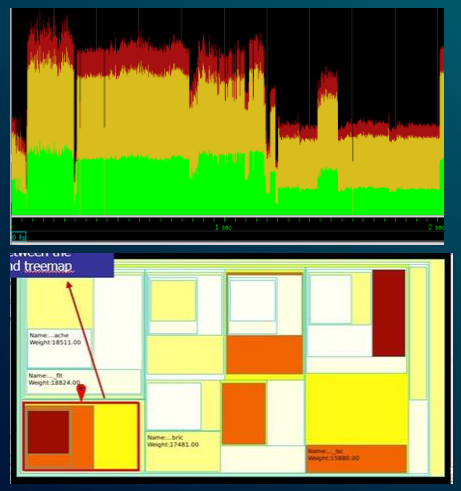
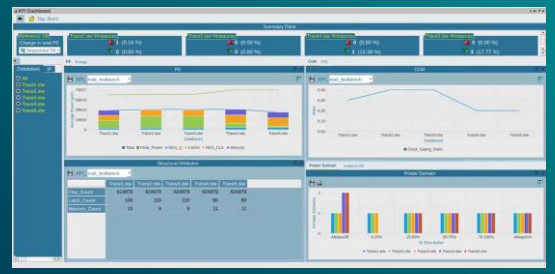
Veloce Power App delivers end-to-end power solutions

- Design
- Liberty
- UPF
- Workload



Power trend analysis





Time-base CGE

Time-based FFE

Customer design	Capacity (AVB)	Design cycles (M)	Emulation execution time (hrs:min:sec)	Plot generation time (hrs:min:sec)
Design #1	1	175	0:09:09	0:09:51
Design #2	8	56	0:06:06	0:10:50
Design #3	13	550	0:45:18	1:00:14

- ✓ Capturing power profile for entire workload
- ✓ Capturing key power indicators at cluster or SoC level
- ✓ Accurately finding peaks

Generating power profile for Billions of cycles

Making key decisions based on real data

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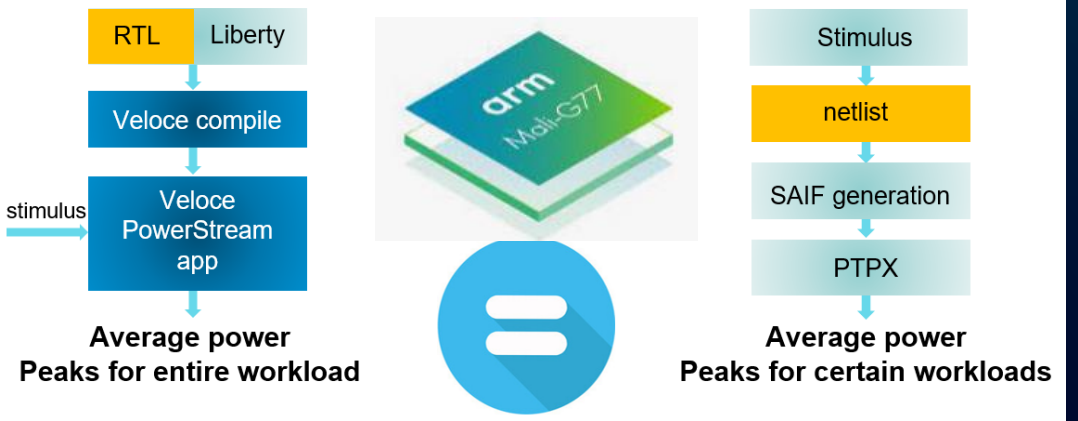
Accuracy is key for customers



Alibaba.com

Veloce power app is a key instrument for below use cases:

- Finding peaks
- IR drop analysis → Leveraging power data for packaging guidance
- De-peaking

Emulation based power analysis address some of the challenges

- Faster TAT for activity generation & analysis
- Faster & accurate power calculation via streaming mode between emulator & power analysis tool

Qualcomm

Veloce Power App provides customers with accuracy requirements for early RTL power analysis

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Siemens power solution technical overview

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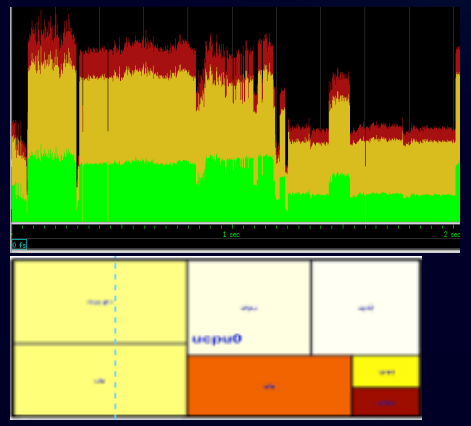
Veloce Power App offerings



Time-based CGE
Time-based FFE

- Built-in Power profiling and Heat map
- Physical aware Power

Power Analysis

- Power metrics generation
- Track power in project life cycle

Power tracking

- Accurate power numbers with power tools

Power estimation

FSDB

SAIF

Streaming API

Power aware verification

- Validate power gating with UPF

Ensuring functionality with UPF running real workloads

Firmware validation and SW tuning with UPF

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Early power trend analysis, estimation and sign-off power

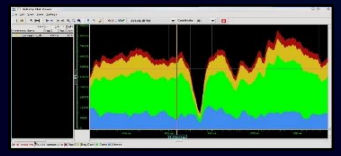
Power profiling at 100s of KHz

Power estimation

Sign-off power numbers

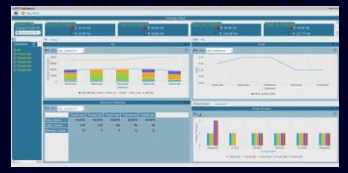
No compile and visibility restriction

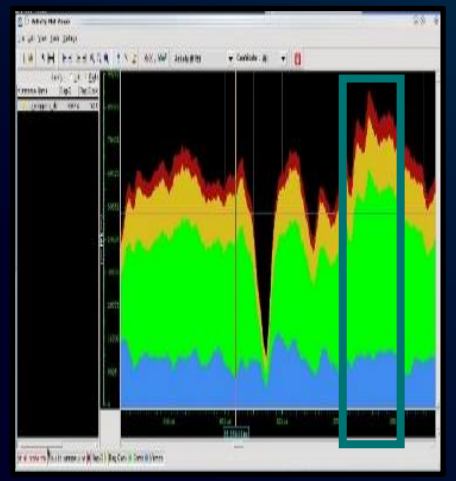
Power Profile



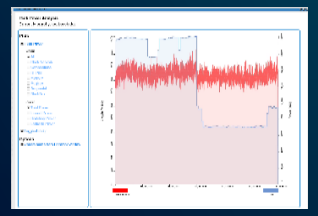
Design Hotspot

Power Dashboard

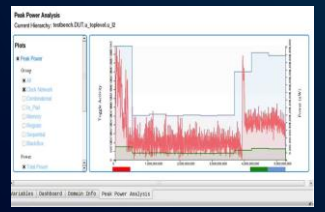




Average power



Peak power



Gate-level sign off

Gate-level sign off

Billions of cycles

Millions of cycles

Thousands of cycles

Profile real workloads on full SoC
Identify hotspots, peaks, di/dt
Metric based power Tracking (**CGE/FFE**) power dashboards

Generating stimulus for power estimation of real scenarios: average and peak power analysis

Sign off power analysis using RTL or Gate switching activity at full SoC

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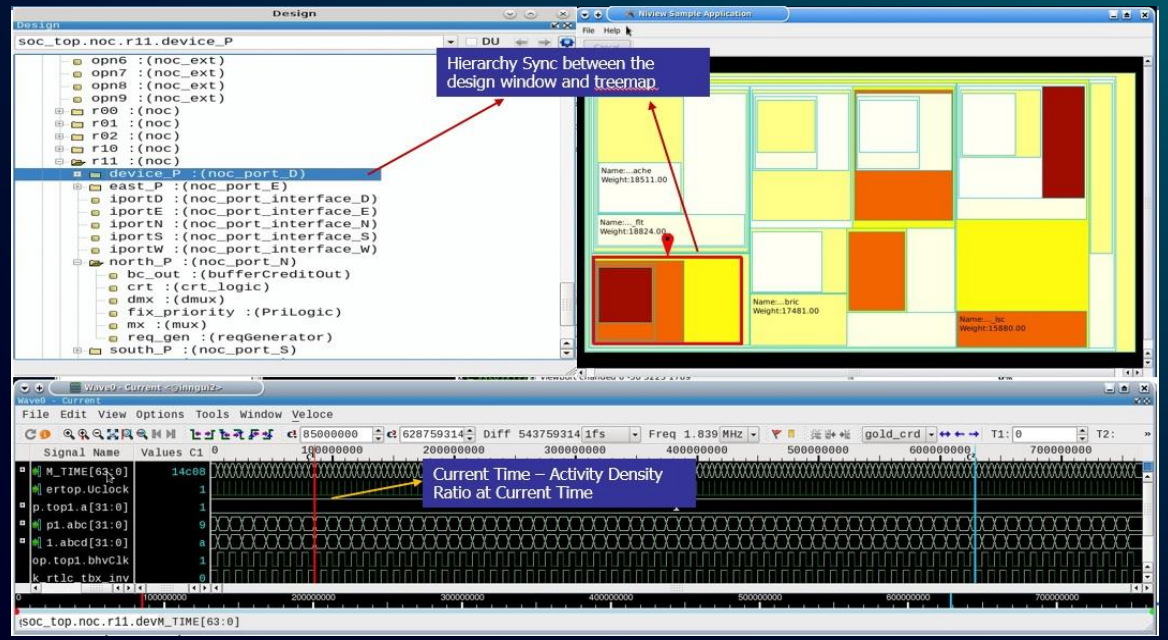
Hotspot analysis with Veloce Power App
Time and space analysis

- Identify design hotspots for representative scenarios
- Visual drill down into design hierarchies of concern
- Identify mistakenly active power domains (power estimation + UPF)
- Time synced with activity plot and waveform



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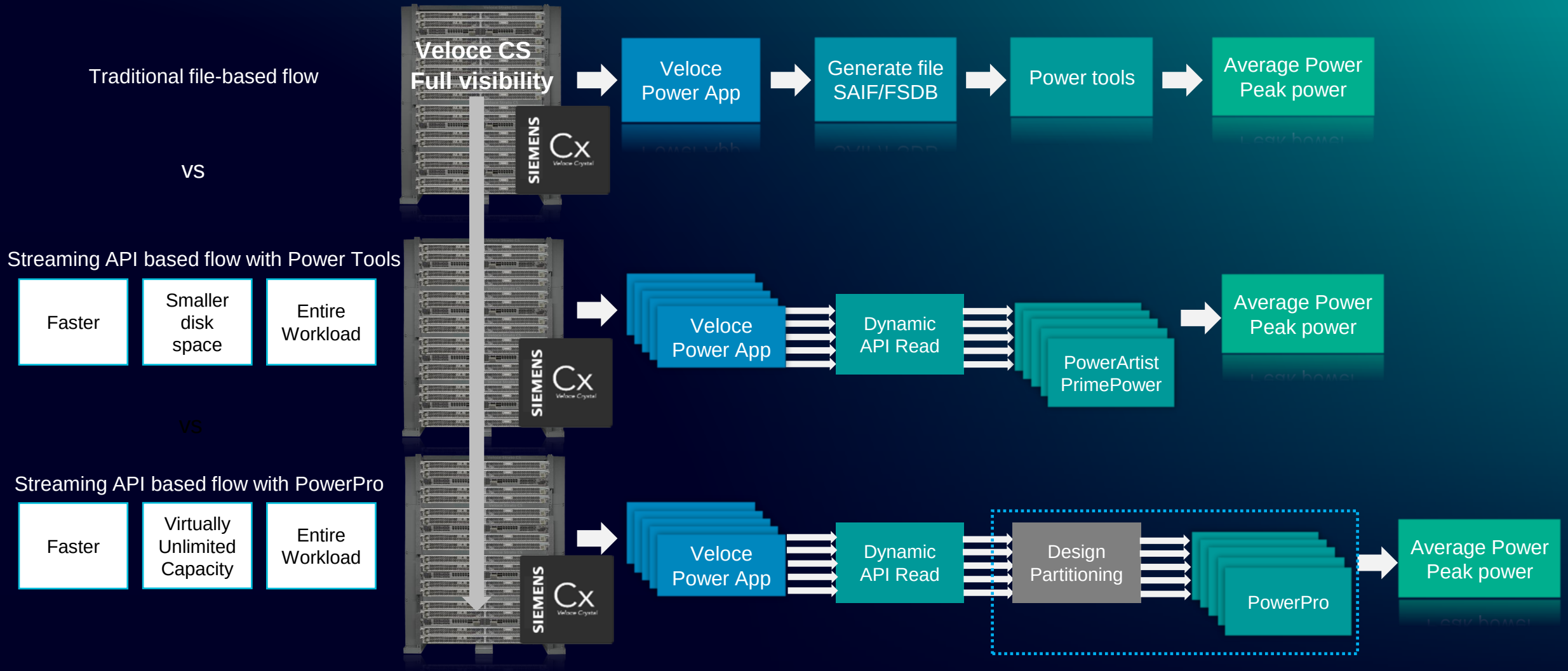
Veloce and PowerPro differentiated solution

High performance for virtually unlimited capacity through design partitioning



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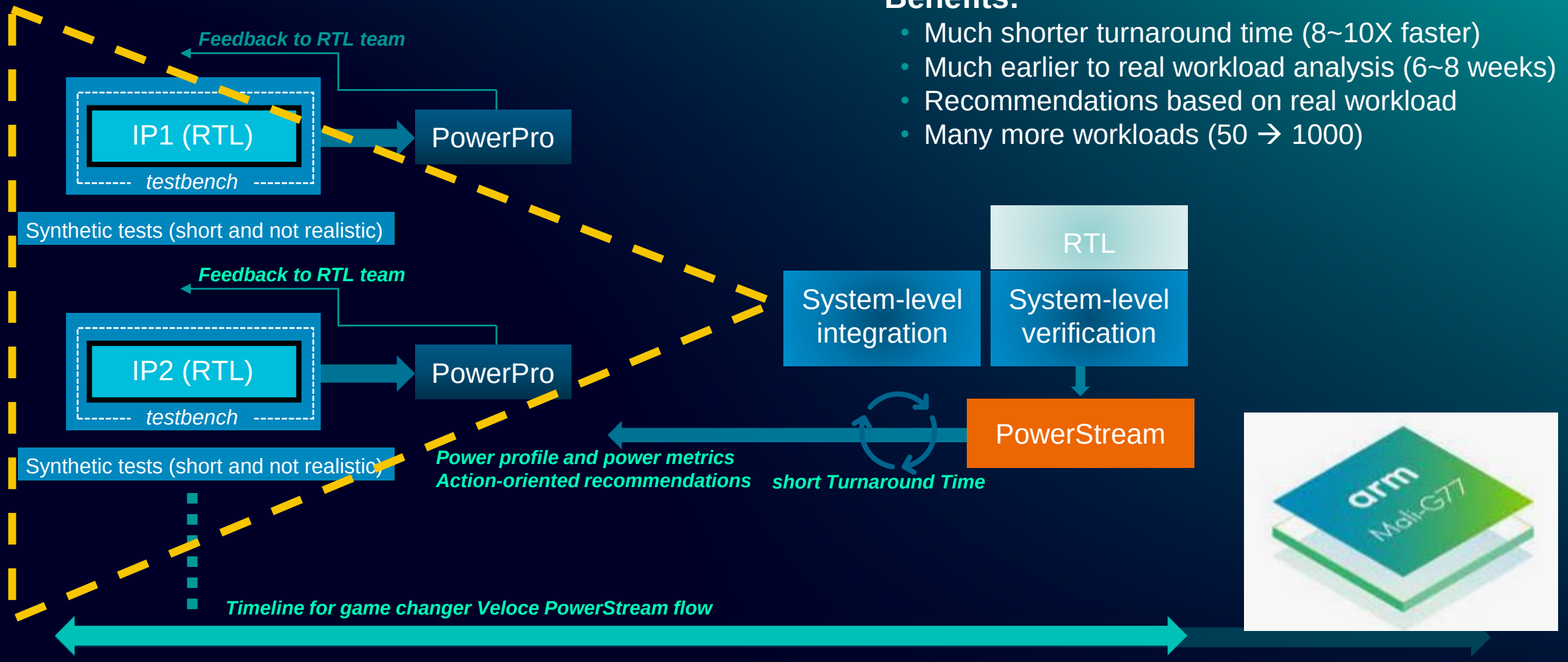
Veloce PowerStream is a game changer



Benefits:

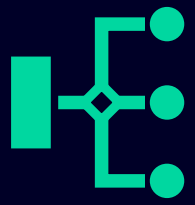
- Much shorter turnaround time (8~10X faster)
- Much earlier to real workload analysis (6~8 weeks)
- Recommendations based on real workload
- Many more workloads (50 → 1000)

Key power indicators are provided by default

Data for sub blocks

Right instances to focus

Design Hierarchy



Module	# Reg/Latch	# Gated Inferred Flop	Avg PT (µW)	Total ET (pJ)	Peak PT (µW)	Avg FFE	Avg CGE (G/L)
	164790/2	154738	1165.42	1608077220.40	8815.00	2.15	97.70/97.70
	154553/0	152041	301.66	416244444.63	7118.59	6.24	99.42/96.69
	15010/0	14951	2.94	4056469.05	443.21	0.00	99.93/99.02
	14698/0	14645	1.27	1753042.75	466.34	5.26	99.97/99.23
	56984/0	54980	41.50	57264643.74	4839.80	0.08	99.77/93.00
	27743/0	27488	93.82	129453756.42	1975.67	1.83	98.93/98.93

Reg/Latch: number of registers/latches in this instance
#Gated Inferred flop: # of inferred clock gating elements
Avg PT: Average Power
Peak PT: Peak Power
Avg FFE: Average Flip Flop Efficiency
Avg CGE (G/L): Average Clock gating efficiency (global/local)

This data and much more details can be dumped in CSV for post analysis

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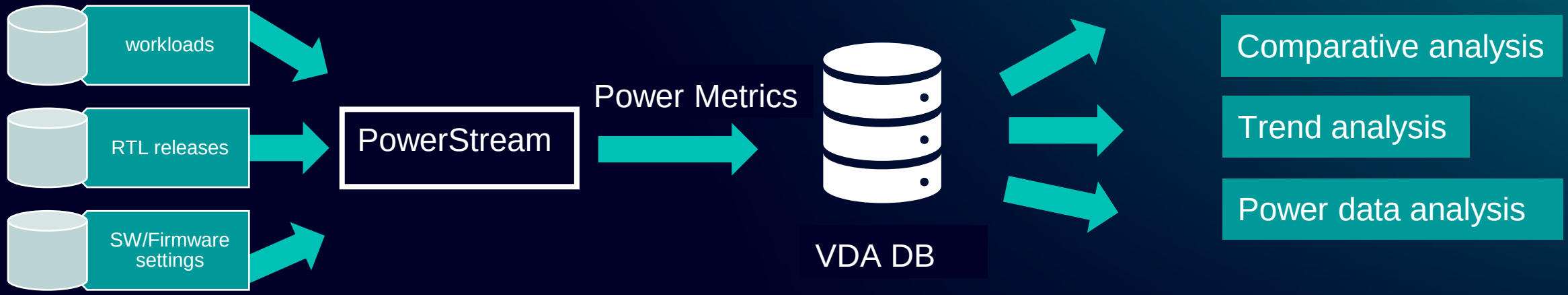
Power analysis is a journey: Tracking data (KPIs) throughout this process

- Power data needs to be kept for various RTL releases and tests for comparison.
- Trend will help the design team and architecture team to identify possible issues
- There are many hardware and software related parameters which can impact power. It is crucial to be able to collect the data and compare scenarios
- An infrastructure for data-oriented power analysis is provided



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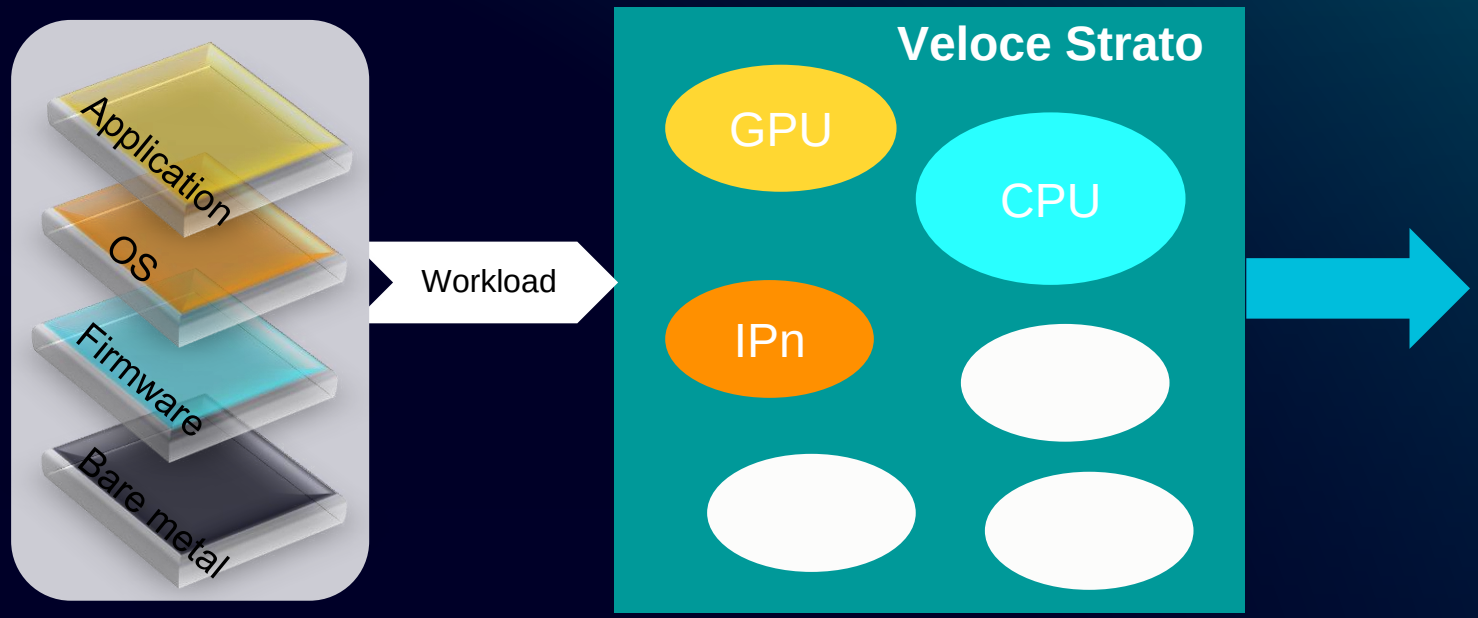
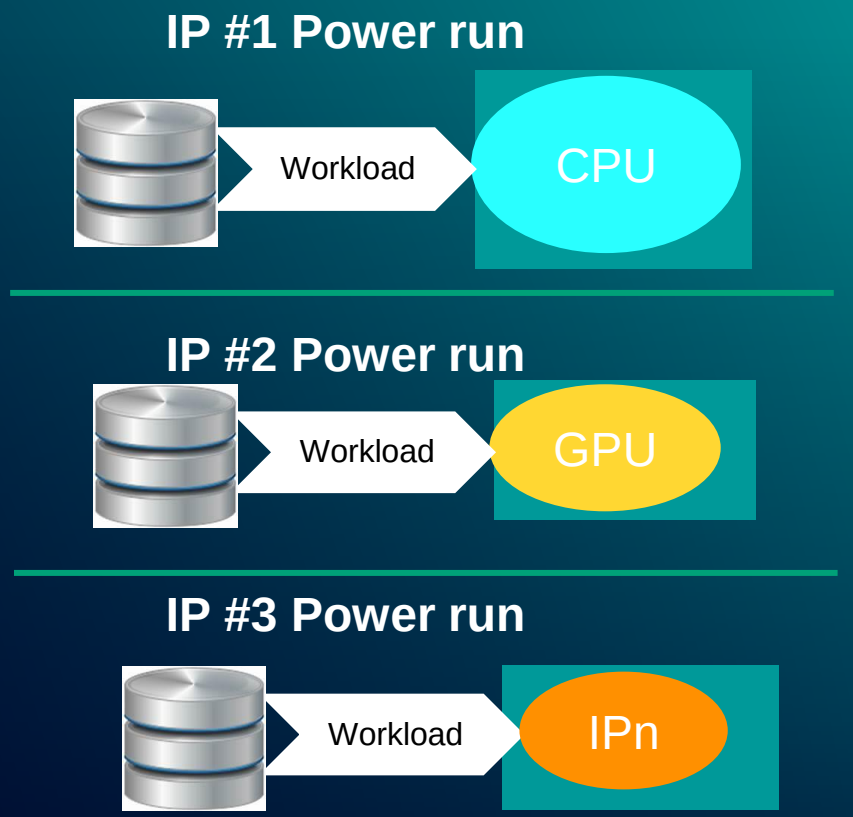
IP power profiling/analysis using system-level workloads

IP power in SoC context

System Level run with Modular Replay instrumentation





Smaller HW capacity for IP power data generation	
Faster turn-around time for power analysis	
Enabling much easier job placement (IP vs Full SoC)	

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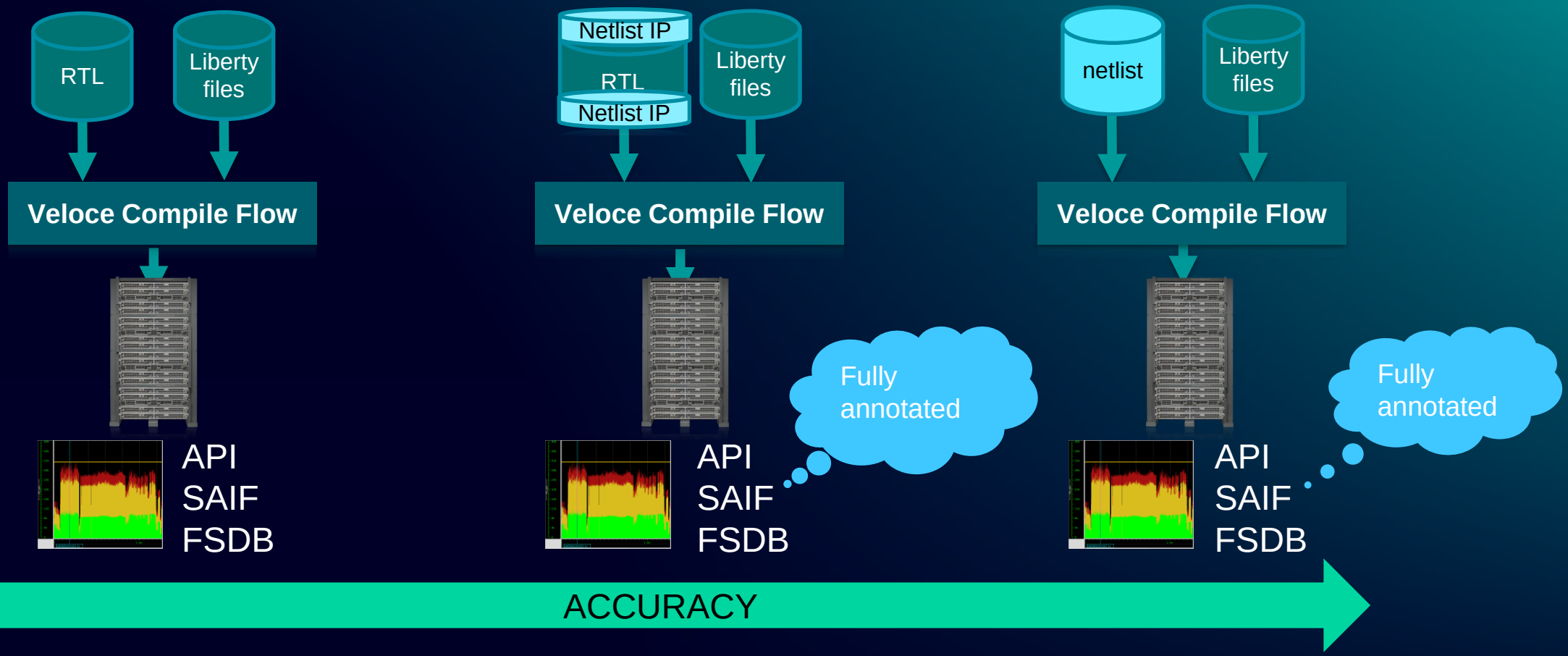
Veloce Power App provides flexibility for different phases of your design cycle



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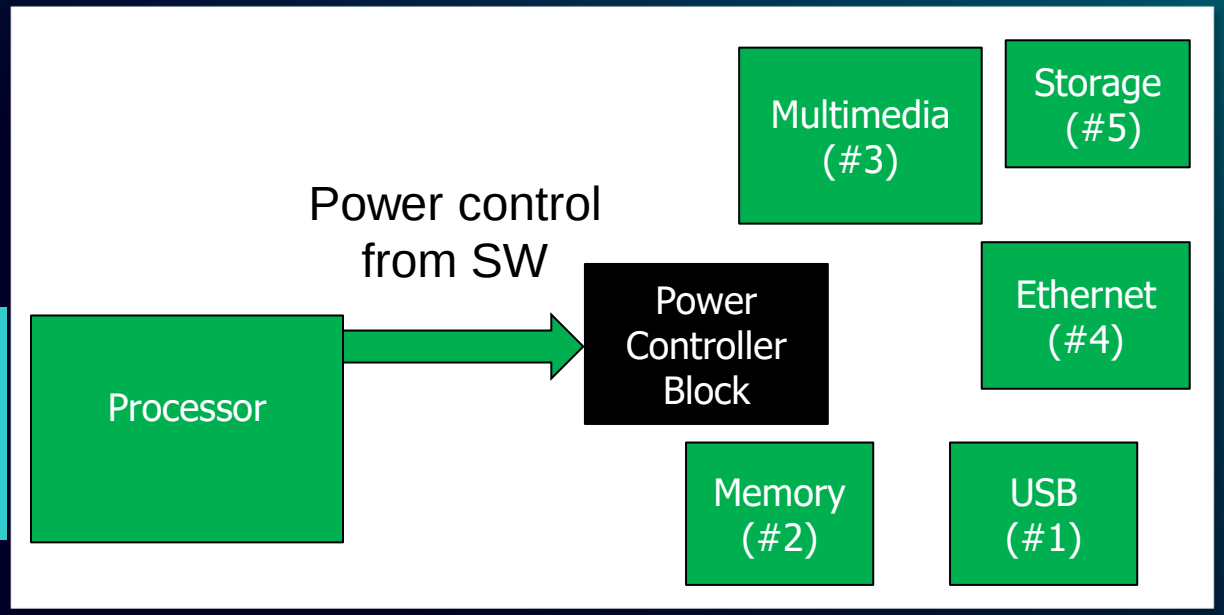
SW-driven power management

Veloce running full SoC



SW running on embedded processor

IEEE Std 1801™-2013

SW-driven power management validation

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Early, accurate power analysis with real workloads

Power analysis needs to be performed as early as possible with real workload

Highly configurable platforms will provide missing pieces to enable real workload analysis in early design cycle

Running 100s of benchmarks early in the design cycle is possible and essential!

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Power impacts: What you can do…

Data centers could consume 20% of total electricity by 2030 ….

….or we can reduce that with effective power management

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Thank you

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