Find and Fix Excessive Power Dissipation of your Chip Very Early in the Design Cycle

Mohammed Fahad

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PowerPro – Platform and Offering

Market's #1 Power Optimization

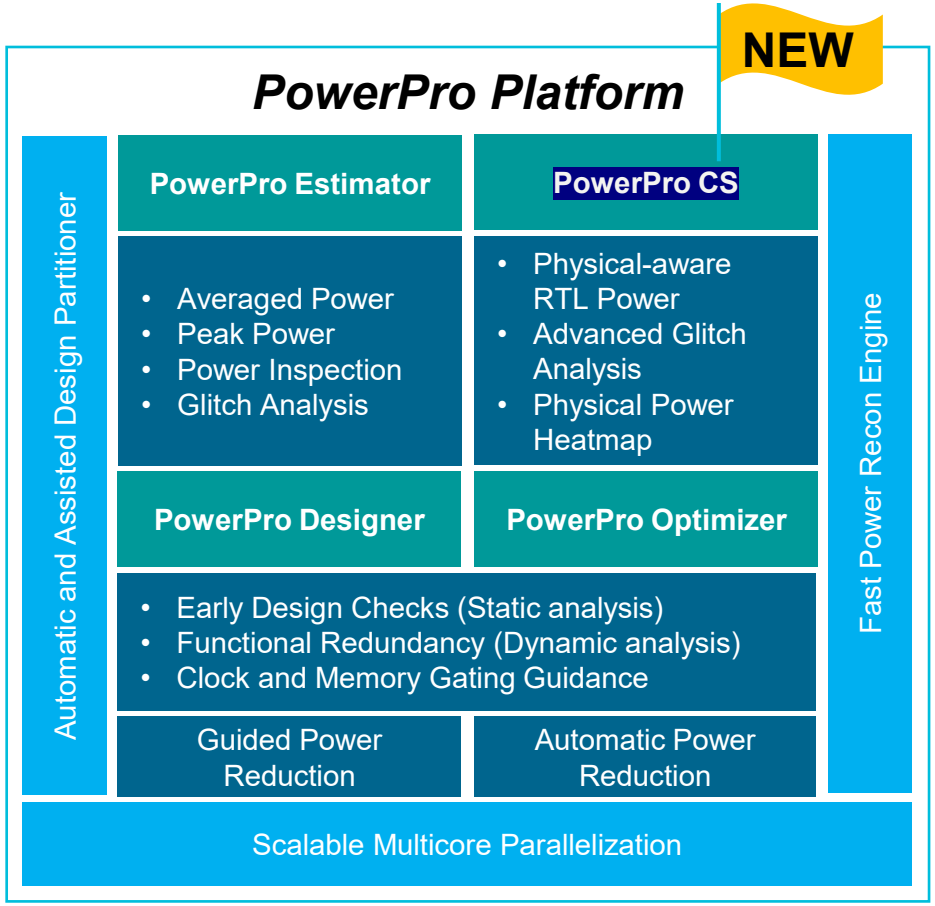
- Offers manual and automatic RTL patching flows
- Industry's flagship power optimization solution offering highest QoR
- Only solution that provides fully automatic power reduction

Highest Capacity, Fastest TAT for Power

- Highest capacity in the market for billion plus gate SOCs enabled through unique design partitioning
- Fastest TAT with highly scalable multicore architecture supporting analysis for millions of cycles

New Physical-aware Estimation

- New accurate power estimation with physical-aware engine
- Advanced analysis like glitch power, physical-aware power heatmap



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Power along the design life cycle

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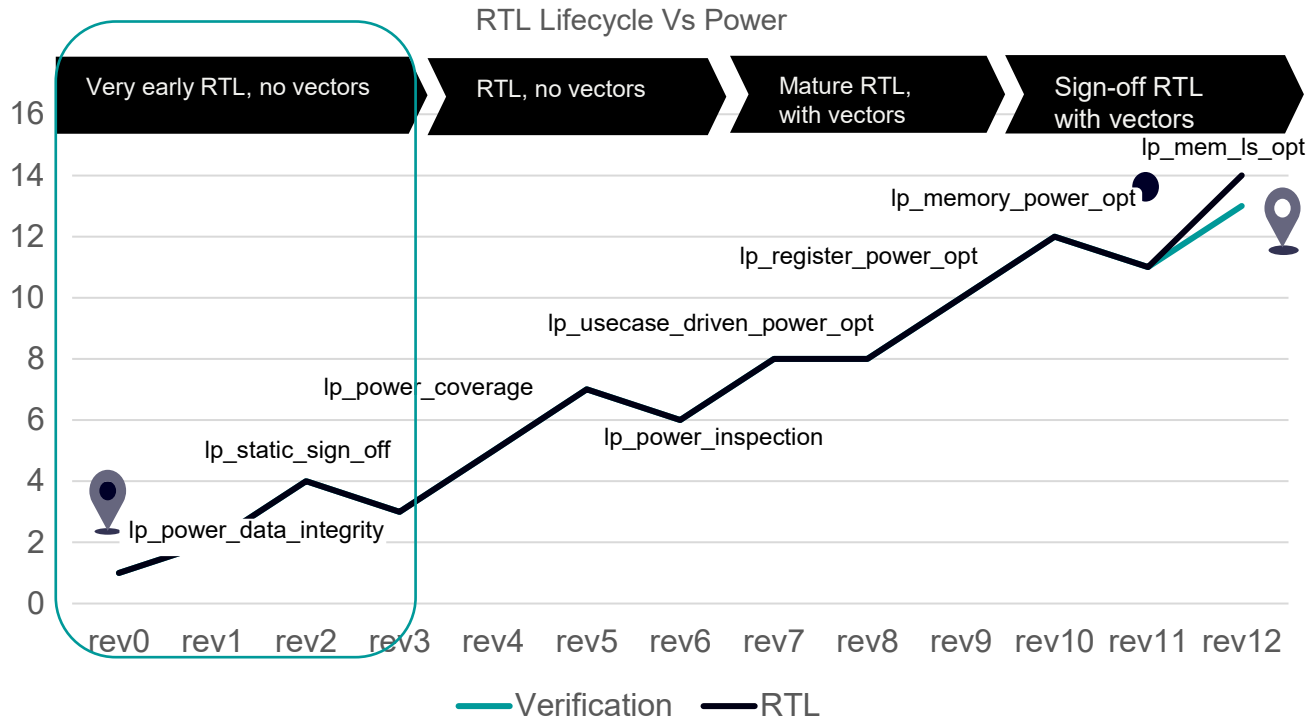
Different RTL stages, different power objectives – Apply the tool wisely



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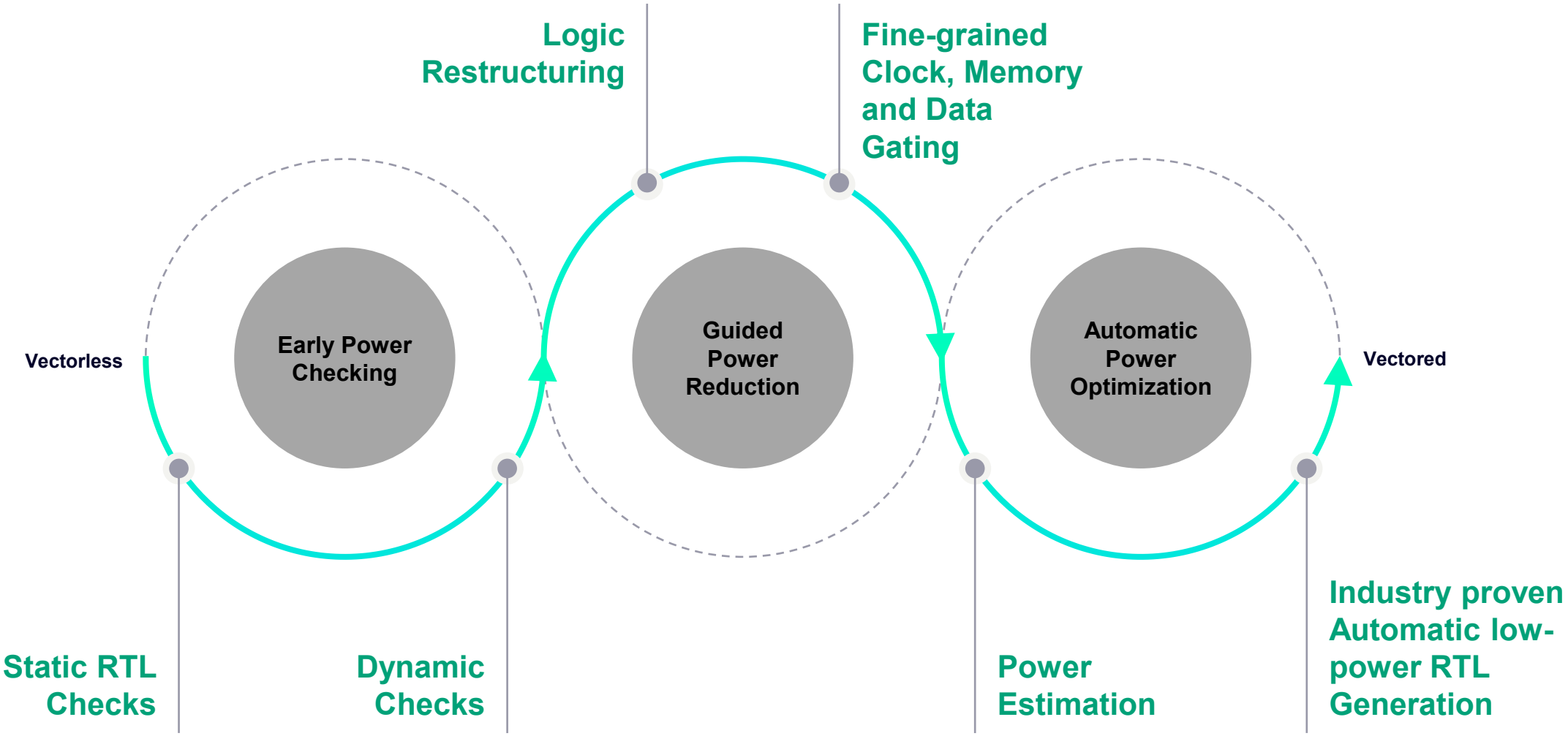
Comprehensive low-power optimization throughout the RTL design cycle



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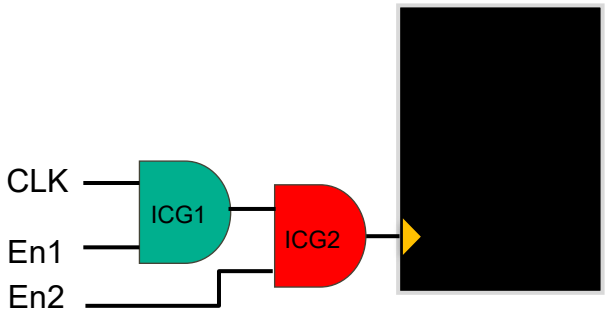
Early Design Checks

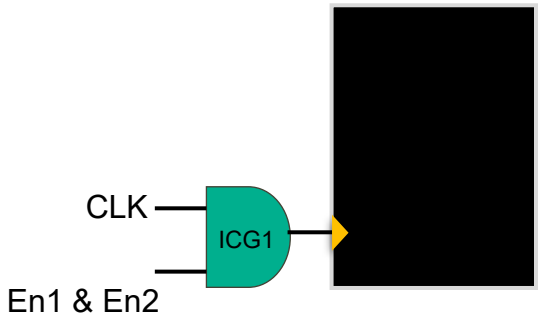
- Can be run without vectors
- Runs extremely fast
- Performs structural analysis of the RTL to find potential issues that can impact power downstream
- EDC metrics can be used to qualify IPs for lowpower

Early Design Checks	
Ungated Memories	NA
Ungated Macros	NA
Ungated Memory Inputs	NA
Floating Memory Data Outputs	NA
Memory Redundant Toggle Inputs	NA
Not Combinationally Enabled Flops	NA
Ungated Flops	NA
Ungated MUX Inputs	NA
Constant CGICs	NA
Functionally Redundant CGICs	NA
Structurally Redundant CGICs	NA
Ungated Operator Inputs	NA
Feedback MUX Registers	NA
FSM Info	NA
Coding Style Checks-01	1 Counters
Coding Style Checks-02	1 Counters
Coding Style Checks-03A	NA
Coding Style Checks-03B	NA

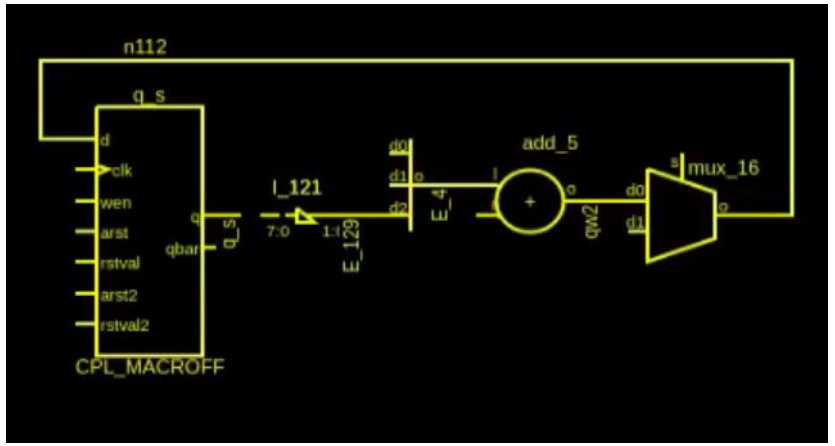
Early Design Checks
examples



(1) ICG1 does not drive FF directly



(1`) Merge two ICGs into one



Free running counters driving big logic

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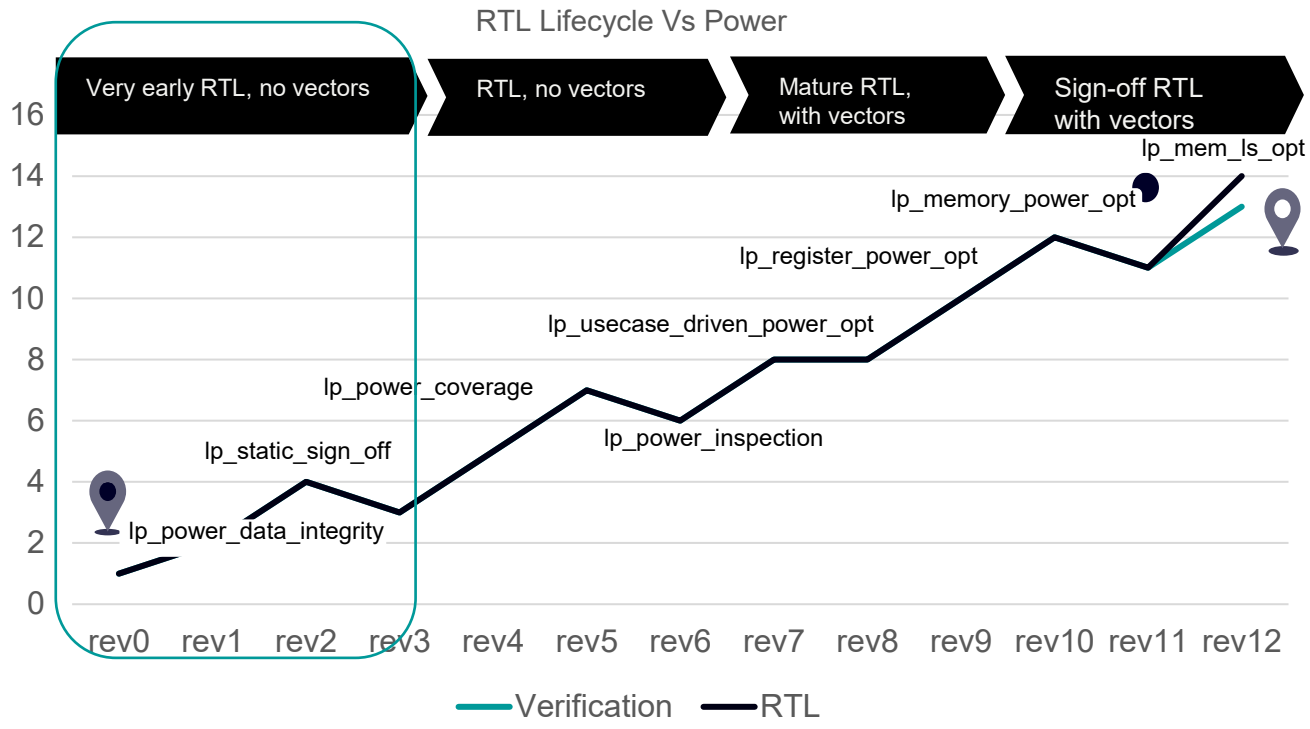
Different RTL stages, different power objectives – Apply the tool wisely



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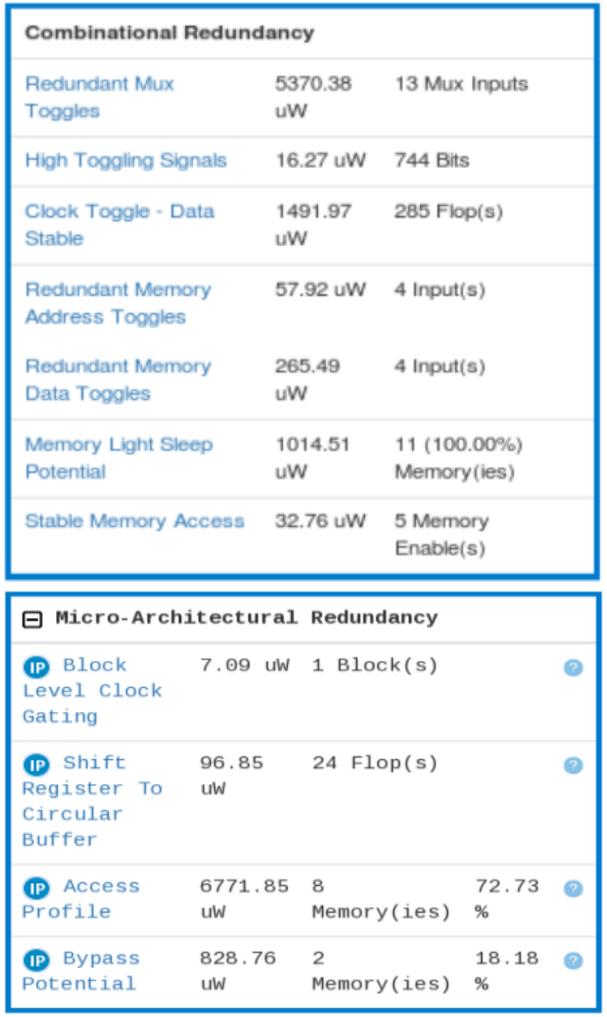
Combinational & Micro-architectural Redundancies

- Need RTL and input vectors
- Performs functional analysis of the waveform to find wasted toggles in the design that will waste power as a result
- Reports the analysis in different kinds of metrics around memories, registers, muxes etc



Combinational Redundancy

Redundant Mux Toggles	5370.38 uW	13 Mux Inputs
High Toggling Signals	16.27 uW	744 Bits
Clock Toggle - Data Stable	1491.97 uW	285 Flop(s)
Redundant Memory Address Toggles	57.92 uW	4 Input(s)
Redundant Memory Data Toggles	265.49 uW	4 Input(s)
Memory Light Sleep Potential	1014.51 uW	11 (100.00%) Memory(ies)
Stable Memory Access	32.76 uW	5 Memory Enable(s)

Micro-Architectural Redundancy

Block Level Clock Gating	7.09 uW	1 Block(s)	
Shift Register To Circular Buffer	96.85 uW	24 Flop(s)	
Access Profile	6771.85 uW	8 Memory(ies)	72.73 %
Bypass Potential	828.76 uW	2 Memory(ies)	18.18 %

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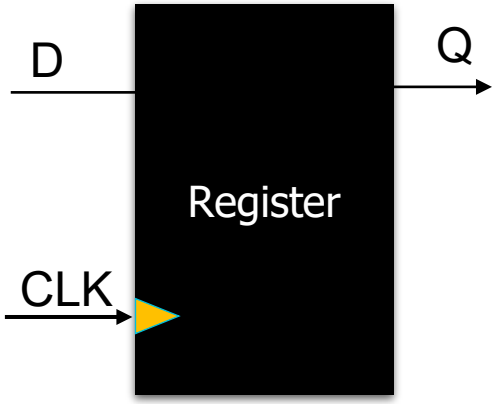
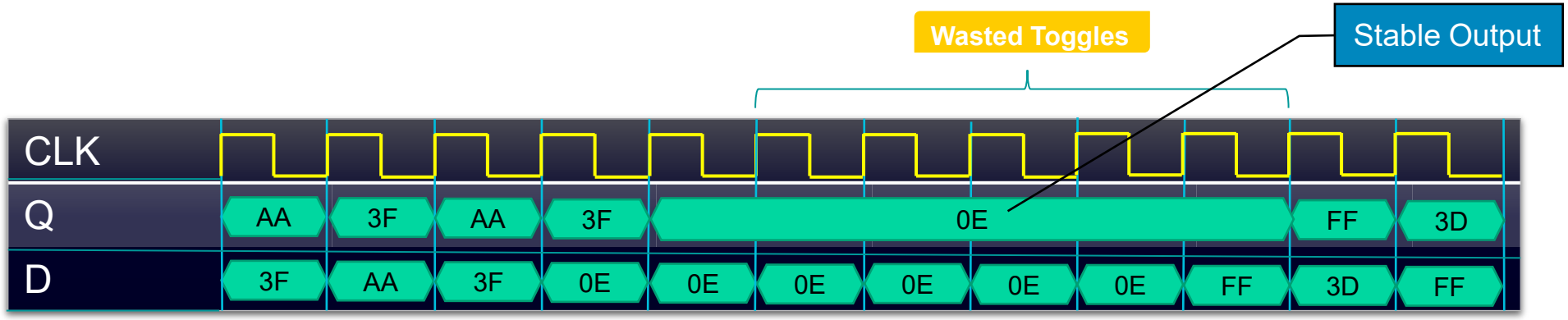
Combinational Redundancy

Clock Toggle Data Stable example





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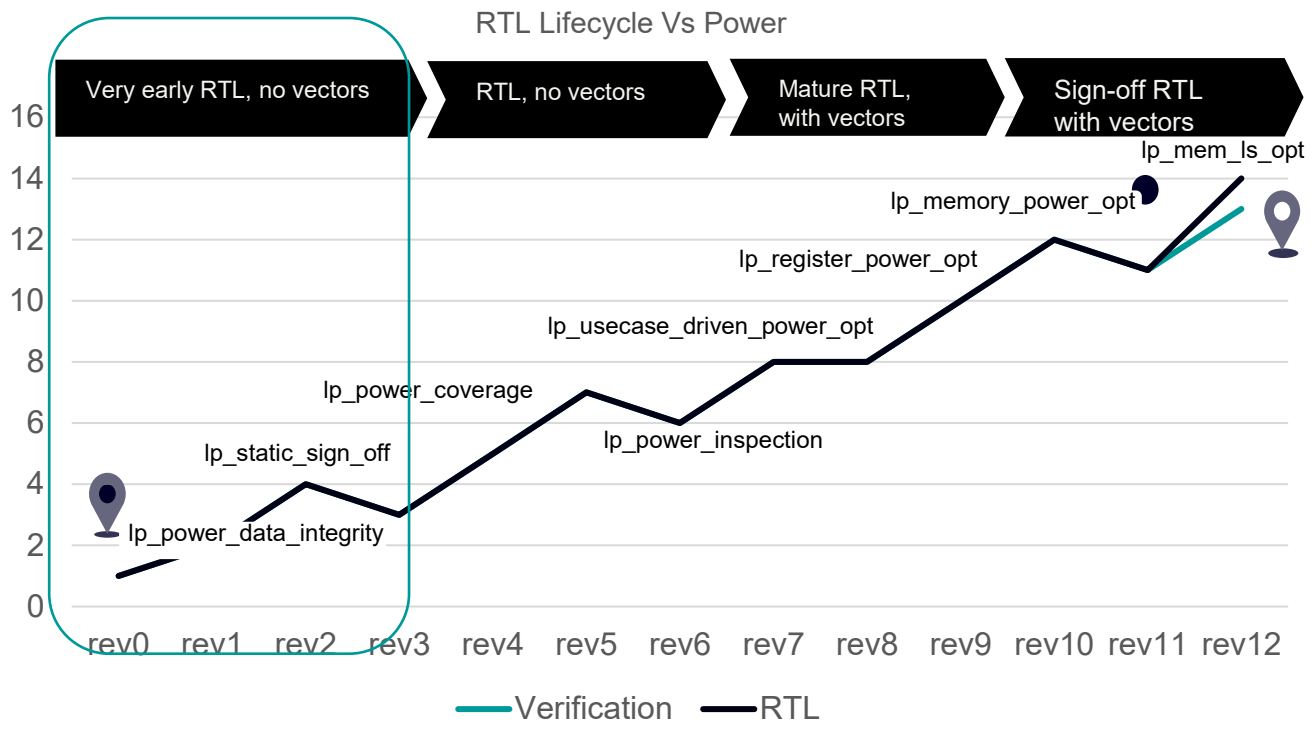
Different RTL stages, different power objectives – Apply the tool wisely



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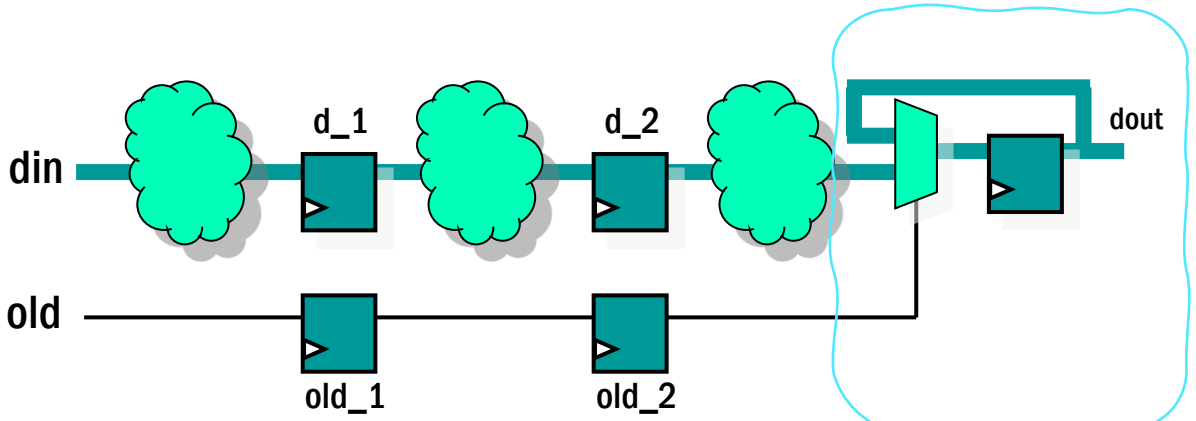
Multi-cycle Clock Gating

Observability based analysis

Low Power Synthesis
DC/RC



No Gating, Wasted Activity

Combinational Clock Gating

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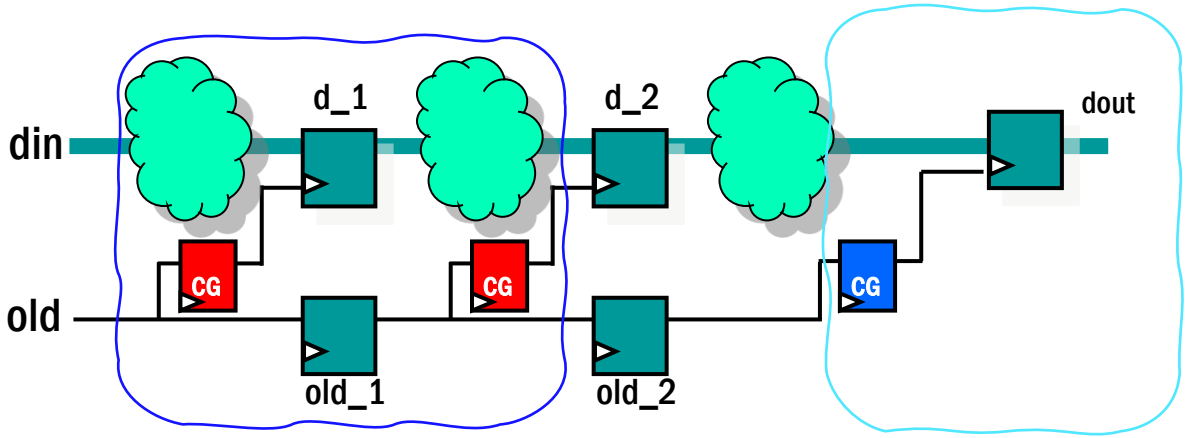

PowerPro Enhanced Gating

Combinational Clock Gating

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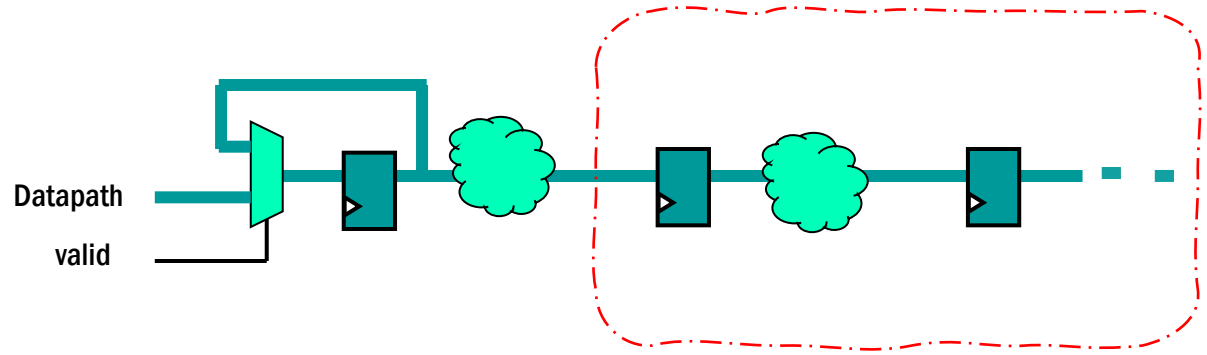
Multi-cycle Clock Gating

Stability based analysis

Low Power Synthesis
DC/RC



Combinational Clock Gating

No Gating, Wasted Activity

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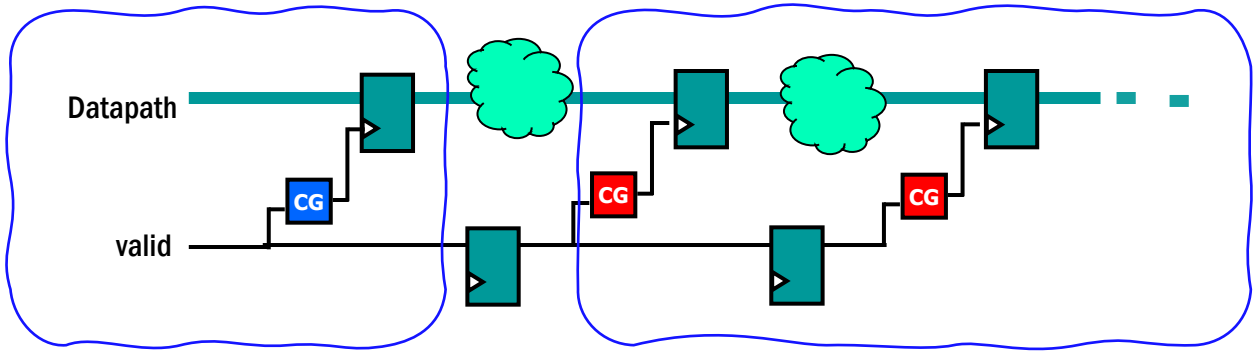

Combinational Clock Gating

PowerPro Enhanced Gating

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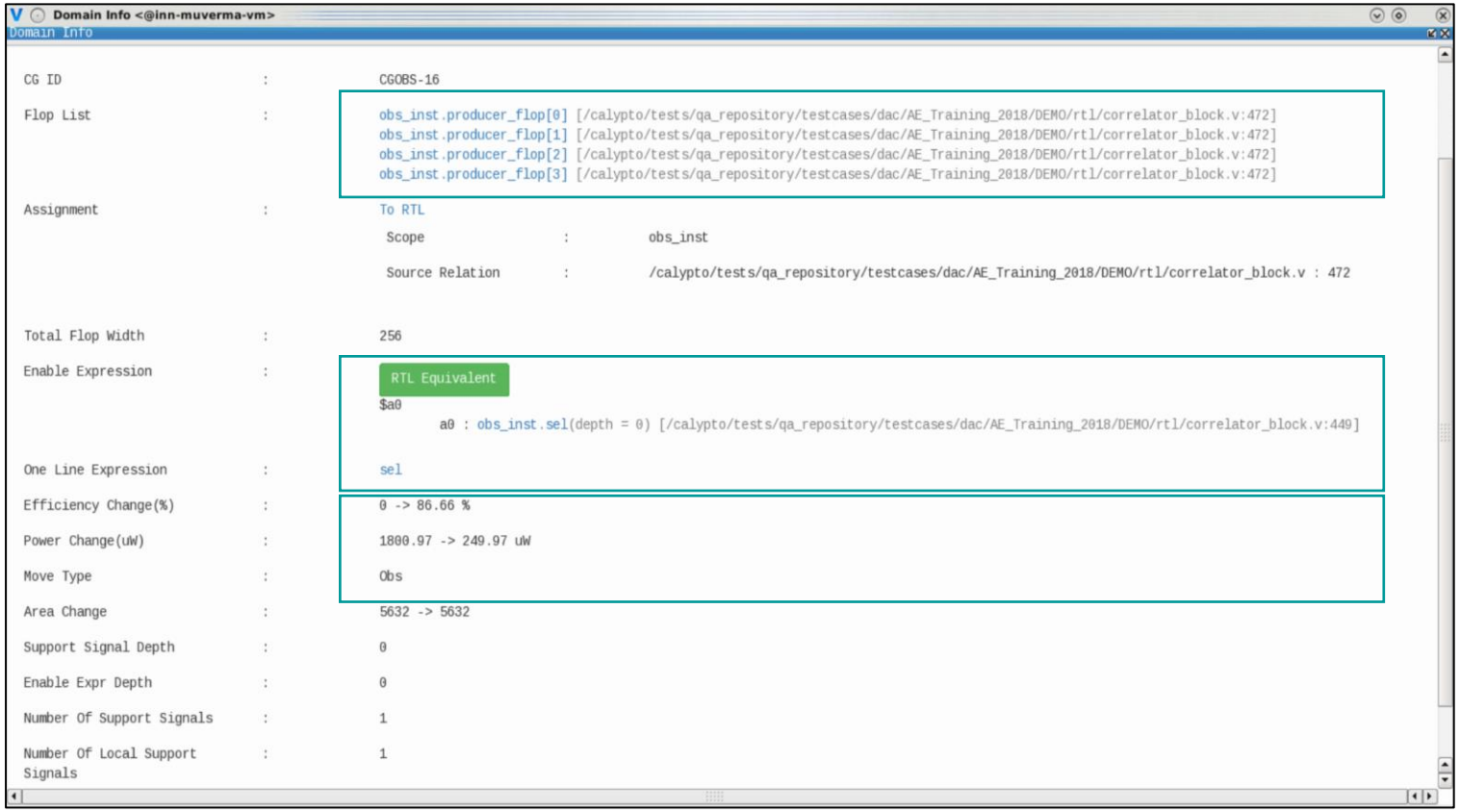
Example of Clock Gating Report

Complete details to understand, analyze and implement suggestions

- Contains all relevant information to implement this clock Gating suggestion from the tool
- Enable expression reported in a form where it can simply be “copy-pasted”
- Shows which signals contribute to the enable expression
- Shows the impact on power



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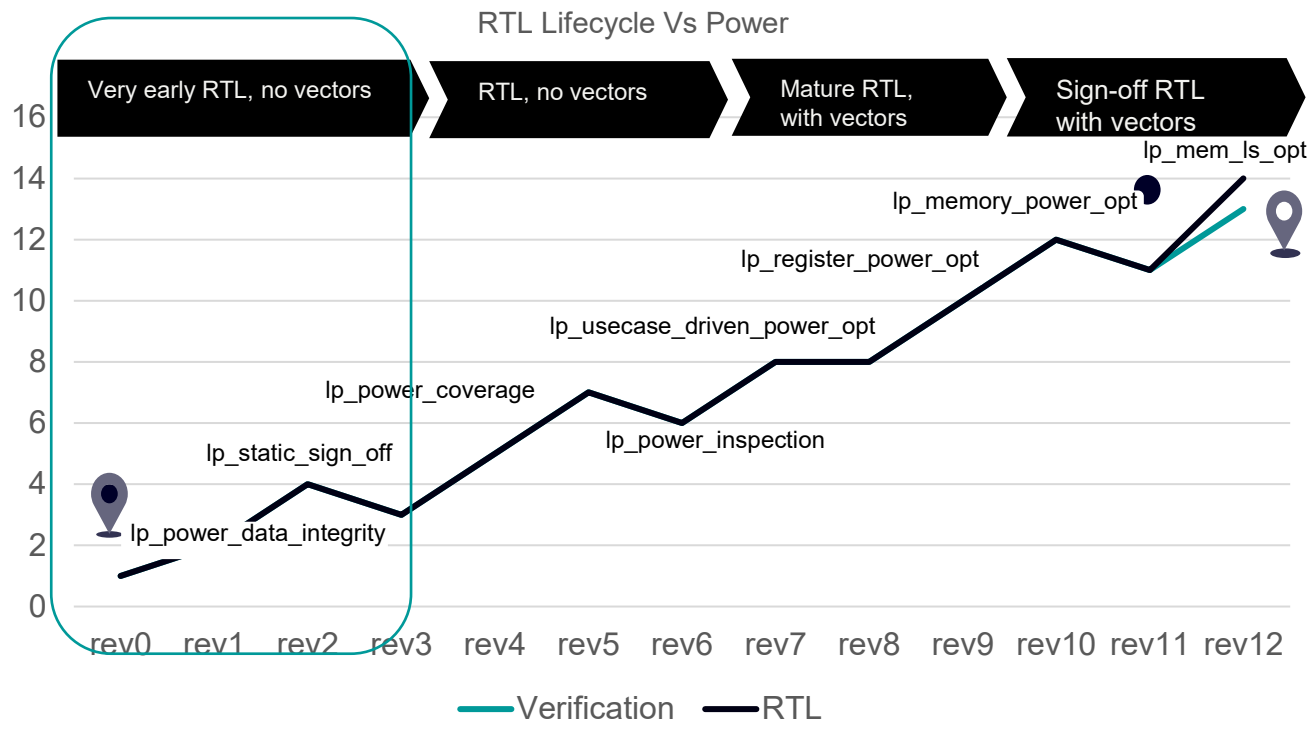

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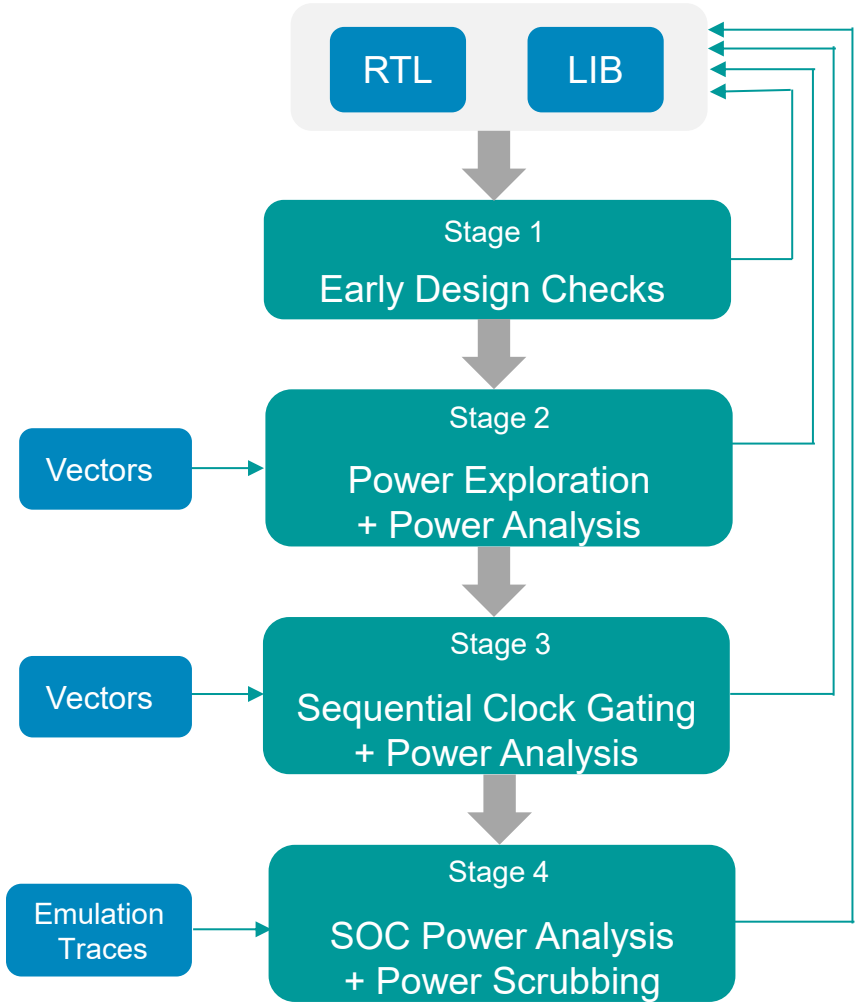
Full flow, IP to SOC Power Solution



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