Accellera Update

By Lu Dai, Accellera Chairman

DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

Lu Dai
Chairman
Accellera Systems Initiative

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Lu Dai is a Senior Director of Technical Standards at Qualcomm, spearheading semiconductor standards efforts and relationships with industry organizations. Lu was previously Senior Director of Engineering and led Qualcomm's SOC design verification team and front-end methodologies and initiatives. He was also the Design Verification Lead responsible for multiple generations of Premium Tier chips at Qualcomm, including the best-selling Snapdragon 800 that powers the Mars Perseverance rover and Ingenuity helicopter.

Prior to Qualcomm, Lu was the Design Verification Lead for Cisco's Gigabit Switching Business Unit where he worked on multiple generations of Cat4k ASICs.

Lu is the current Chair of Accellera and serves on the Board of Directors at RISC-V International and Si2.

Lu holds a Master's degree in Electrical Engineering from Cornell, and a Bachelor's in Electrical Engineering and Computer Science from UC Berkeley.

Accellera History

- Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modeling, and verification standards for use by the worldwide electronics industry.
- Accellera supports a mix of user and vendor standards and open interfaces development in the area of electronic design automation (EDA) and intellectual property (IP).
- Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera are contributed to the IEEE for formal standardization and ongoing governance.

- 1991: Open Verilog International (OVI) and VHDL International (VI) founded separately
- 2000: OVI and VI merged to form Accellera Organization
- 2009: Accellera merged with The SPIRIT Consortium
- 2011: Accellera merged with Open SystemC Initiative (OSCI) and changed its name to Accellera Systems Initiative
- 2013: Accellera acquired Open Core Protocol (OCP) standard, the intellectual property of the OCP International Partnership (OCP-IP)

Accellera Systems Initiative

Our Mission

To provide a platform in which the electronics industry can collaborate to innovate and deliver global Electronic Design Automation and IP standards that improve design and verification productivity for today's advanced integrated circuits and embedded systems. In addition, we strive to promote the widespread adoption of these standards.

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AMD
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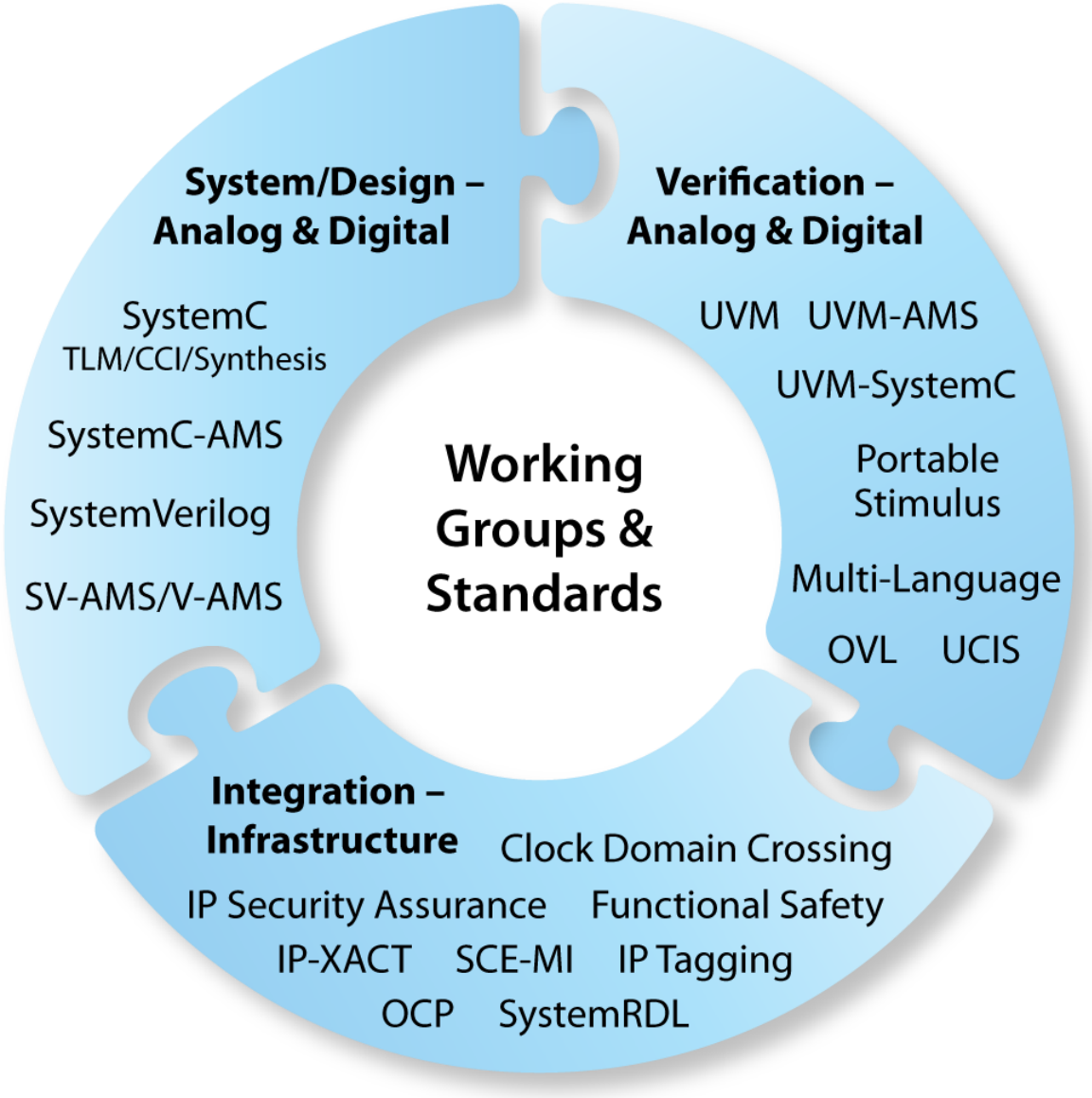
The Accellera Ecosystem



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Accellera Standards and Activities

Current Standards and Supplemental material

Standards

- Intellectual Property (IP) Tagging 1.0
- IP-XACT - Update of IEEE P1685 and Vendor Extensions
- Multi-Language (ongoing)
- Open Verification Library (OVL) 2.8.1
- Portable Stimulus 2.0
- Security Annotation for Electronic Design Integration 1.0
- Standard Co-Emulation Modeling Interface (SCE-MI) 2.3
- SystemVerilog-AMS (ongoing)
- SystemRDL 2.0
- SystemC Analog Mixed-Signal (AMS) 2.3
- SystemC Configuration, Control & Inspection (CCI) 1.0
- SystemC Core Language 2.3.3 (includes TLM 2.0)
- SystemC Synthesis 1.4.7
- Unified Coverage Interoperability Standard (UCIS) 1.0
- Universal Verification Methodology 2020-1.1
- Verilog-AMS (V-AMS) 2.4

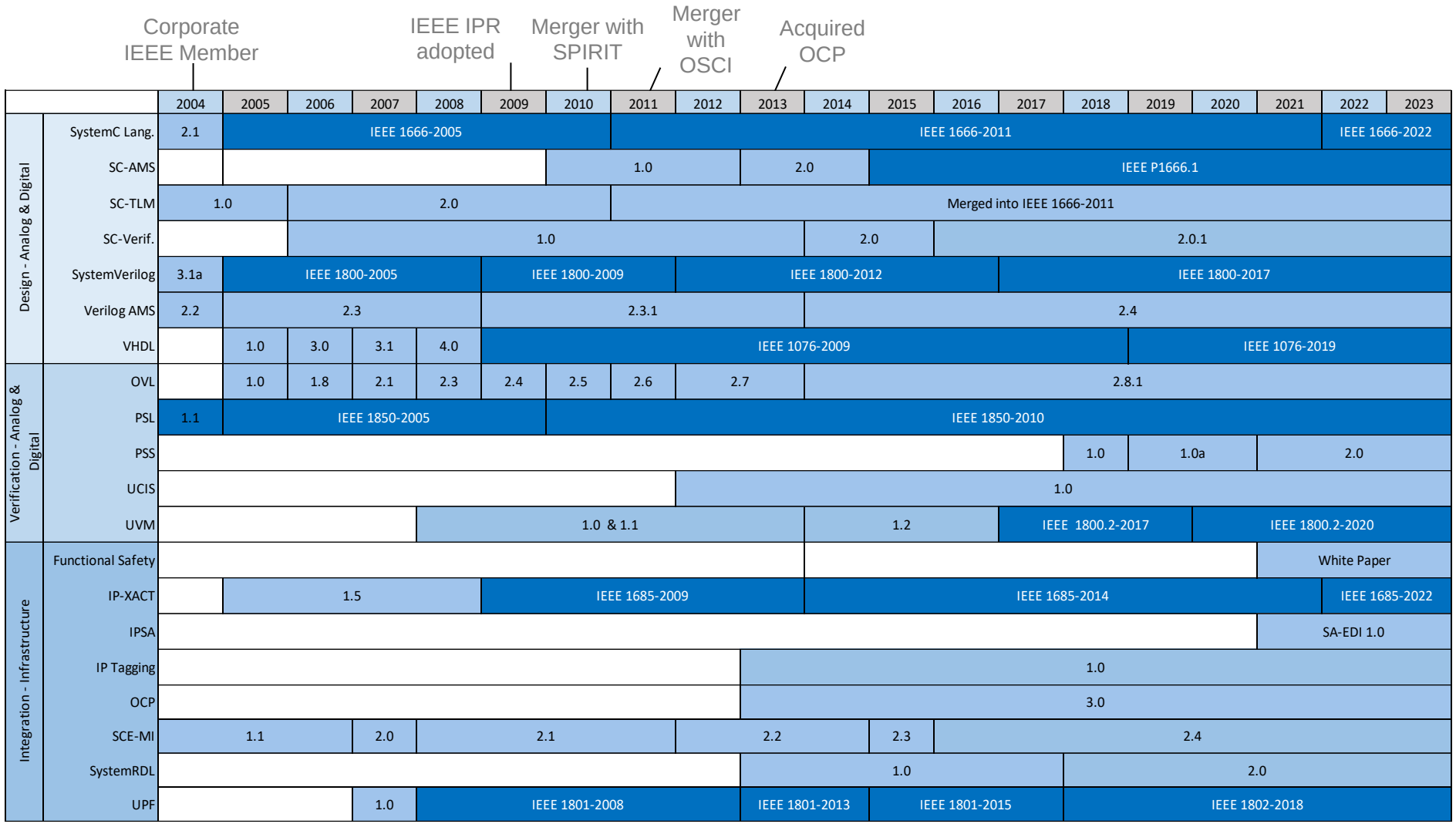
Supplemental material

- IP-XACT Users Guide
- SystemC AMS Users Guide and Application Examples
- SystemC CCI 1.0 Proof-of-Concept Kit
- SystemC Reference Implementation and Regression Test Suite 2.3.3
- SystemC Core Language and Examples
- SystemC Verification Library (SCV) 2.0.1
- UVM 2020-1.1 Reference Implementation
- UVM-SystemC Library 1.0-beta4

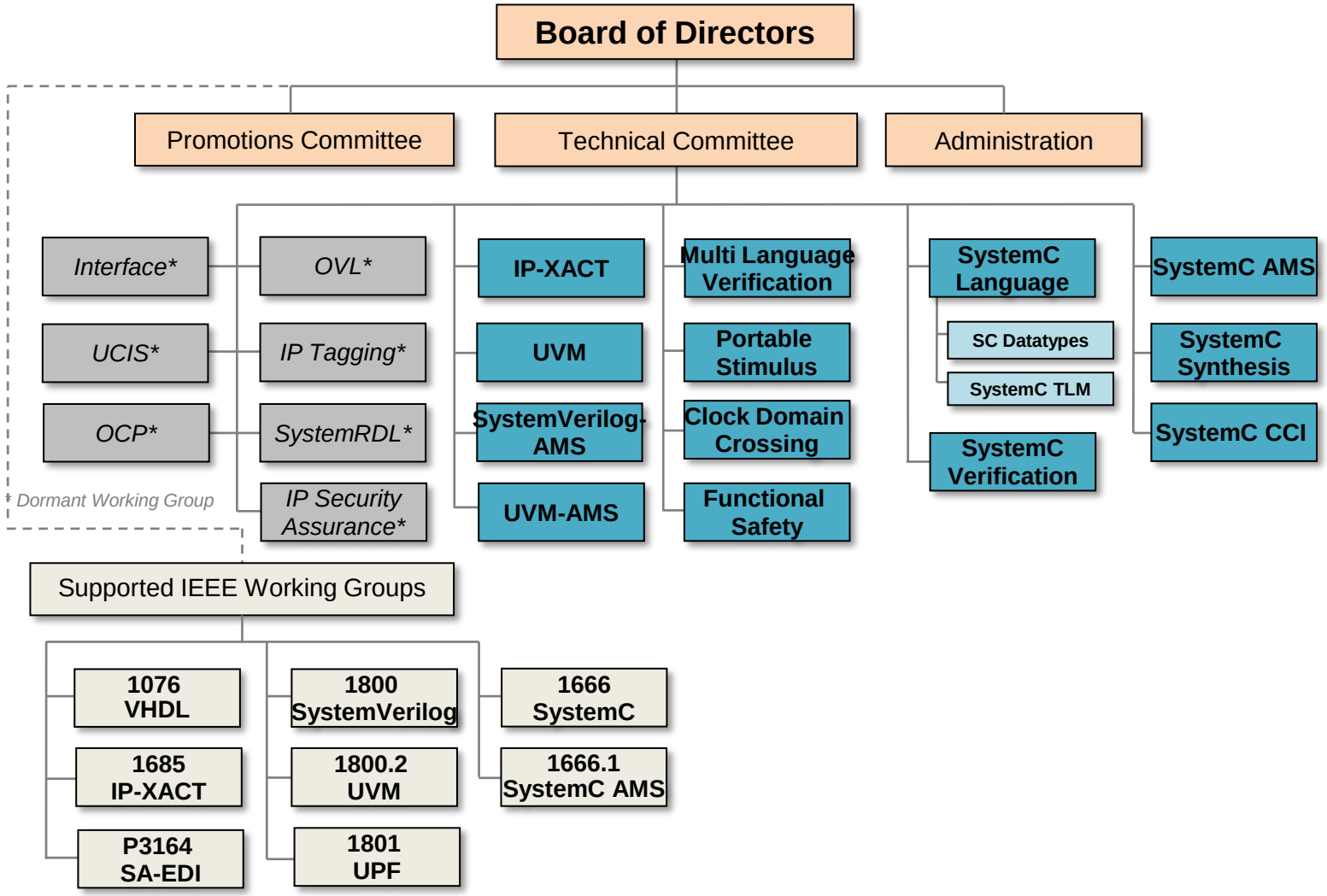
Whitepapers

- IP Security Assurance
- Functional Safety

Accellera Standards



Accellera Structure



Accellera News

- Working Groups
  - New Working Group to standardize Clock Domain Crossing
    January 2023
  - Input sought to explore Federated Simulation Standard development
    July 2023
- Supplemental material
  - Core SystemC Language and Examples
    December 2022
  - UVM 2020-2.0 Reference Implementation updated
    February 2023
- Awards
  - Stanley J. Krolikoski Scholarship for the Study of Electrical Engineering and Computer Science
    February 2023
  - Phil Moorby - 2023 Technical Excellence awardee
    March 2023

Accellera Newsletter June 2023

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IEEE Standards Access at No Charge

- Accellera relationship with the IEEE-SA
- Accellera will release 10 standards for 10 years under an extended IEEE Get program
- More than 165,000 downloads to date!

Download IEEE Standards
http://ieeexplore.ieee.org/Xplore/home.jsp - or find links to specific standards at - www.accellera.org/downloads/ieee

Accellera-IEEE Collaboration

IEEE

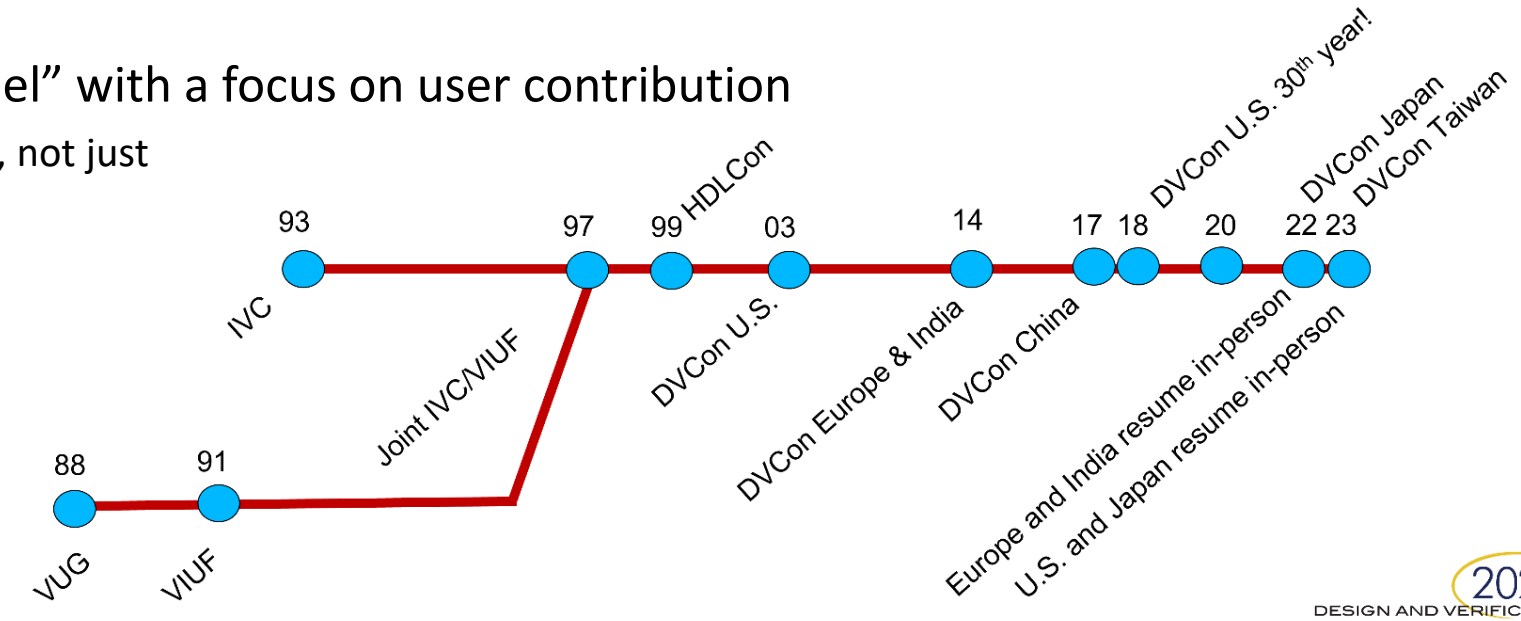
- VHDL or IEEE 1076 or IEC 61691-1-1
- Verilog or IEEE 1364 or IEC 61691-4
- Delay and Power Calculation System (DPCS/OLA: Standard Parasitic Exchange Format) or IEEE 1481
- Standard Delay Format (SDF) or IEEE 1497 or IEC 61523-3
- Open Model Interface (OMI) or IEEE 1499
- Open Compression Interface (OCI) or IEEE 1450.6.1
- Advanced Library Format (ALF) or IEEE 1603 or IEC 62265
- SystemC or IEEE 1666
- SystemC Analog/Mixed-Signal extensions or IEEE 1666.1
- IP-XACT or IEEE 1685
- SystemVerilog or IEEE 1800
- Unified Power Format (UPF) or IEEE 1801
- Universal Verification Methodology (UVM) or IEEE 1800.2
- Property Specification Language (PSL) or IEEE 1850 or IEC 62531

Accellera

- IP Security Assurance (Security Annotation for Electronic Design Integration (SA-EDI))
- Open Core Protocol (OCP)
- Open Verification Library (OVL)
- Portable Test & Stimulus Standard (PSS)
- Standard Co-Emulation-Modeling Interface (SCE-MI)
- Soft IP Tagging
- SystemRDL (System Register Description Language)
- Unified Coverage Interoperability Standard (UCIS)
- Verilog-AMS (Analog Mixed-Signal)

Accellera and DVCon History

- Accellera has been successfully sponsoring Design & Verification Conference & Exhibition in the US for 35+ years
- Original events had different names and were tied to VHDL International and Open Verilog International
- Eventually VHDL and Verilog-focused groups merged into a single conference and became DVCon in 2003
- Global expansion started in 2014: DVCon Europe, DVCon India, DVCon China, DVCon Japan, and DVCon Taiwan
- Every DVCon has a similar “Look & Feel” with a focus on user contribution
  - Papers written by and presented by users, not just papers about products paid by sponsors
  - Panel sessions on current hot topics
  - Tutorials related to relevant standards



Looking Forward

- Functional Safety Working Group
  - Gathering use cases and requirements for a standard
  - Data Model Whitepaper in final review
- IPSA Working Group Security Annotation for Electronic Design Integration Standard
  - Contributed to the IEEE for the development of the P3164 draft standard
- Portable Stimulus Working Group
  - DVCon U.S. 2023 tutorial, including use cases and material to be included in 2.1, now available for download
  - 2.1 in final stages of development
- New Working Group to define Clock Domain Crossing standard
- Federated Simulation Proposed Working Group

Portable Stimulus Info

Proposed Working Group Formed

- Input sought to explore a *Federated Simulation Standard* development
- Industry interest sought in developing a standardized communication interface to enable virtual modeling, simulation, and integration interoperability throughout the product life cycle.

Avionics

VISTAS / VHTNG

Space

SMP2

Semis

SystemC
TLM
IP-XACT

Automotive

openADx
openDRIVE
openSCENARIO
openCRG
openPASS

Mechatronics

FMI / FMU

How to bring these industries and simulation approaches together?

Proposed Working Group Formed

- Communication standard plans to facilitate the creation of a distributed and orchestrated (“federated”) multi-domain simulation framework
- First meeting will be held in-person
  - September 25 & 26, 2023 in Toulouse, France
  - Will discuss applications, uses cases, requirements, and expectations of the standard
  - Organizations and participants are invited to present 3-4 slides to share their industrial application and requirements.
  - Register at accellera.org/activities/pwg

More information & register

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Proposed Working Group Formed

- Charter
  - Cross-industry collaboration to improve the interoperability of product and environment simulation based on co-ordination between existing and new open standards
- Scope
  - Develop a standard (API) and open infrastructure to enable cross-industry interoperability of simulation frameworks
- Purpose of Proposed Working Group
  - Identify industry interest and requirements for a standard / API covering addressing interoperability of simulation
- Tasks of the Proposed Working Group
  - Collect industry requirements for a standardization initiative
  - Identify additional Working Group participants
  - Clarify relations & dependencies to existing standards
- Stakeholders
  - Companies active in different industry/product segments (e.g., Semiconductors, Automotive, Avionics, Space, …)
  - Companies active in different stages of the value chain (Tier2, Tier1, OEM) are invited

New Working Group

- Clock Domain Crossing (CDC) Working Group formed January 2023
- Will define a standard CDC collateral specification to ease SOC integration
- The CDC Working Group will address the current incompatibility of collateral generated by different CDC verification tools, which will help to greatly improve productivity.

Join Accellera to participate in this new WG! For more information go to www.accellera.org

More CDC information

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New Working Group

- Scope
  - To develop a standard format to capture CDC/RDC/Glitch intent.
  - Enable interoperability of CDC collateral generated by different CDC verification tools.
  - Focus on the effort to produce a formal Language Reference Manual (LRM).
- Background
  - SoC teams cannot reuse IP-level CDC collateral in the SoC environment if both teams use different CDC verification tools.
  - Causing a CDC verification problem when the SoC teams source IP from IP providers that use a different tool for their own CDC verification.
  - To perform holistic SoC-level verification, additional resources are needed to reconverge the IP with the verification tool used by the SoC team.
  - Redoing IP-level CDC verification is time consuming and labor intensive.
  - Standardization on CDC collateral will bring significant benefits to not only product companies, but also IP design houses, EDA tool companies, and the entire ecosystem.

Thank you to our Accellera Global Sponsors

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