

SYNOPSYS[®]

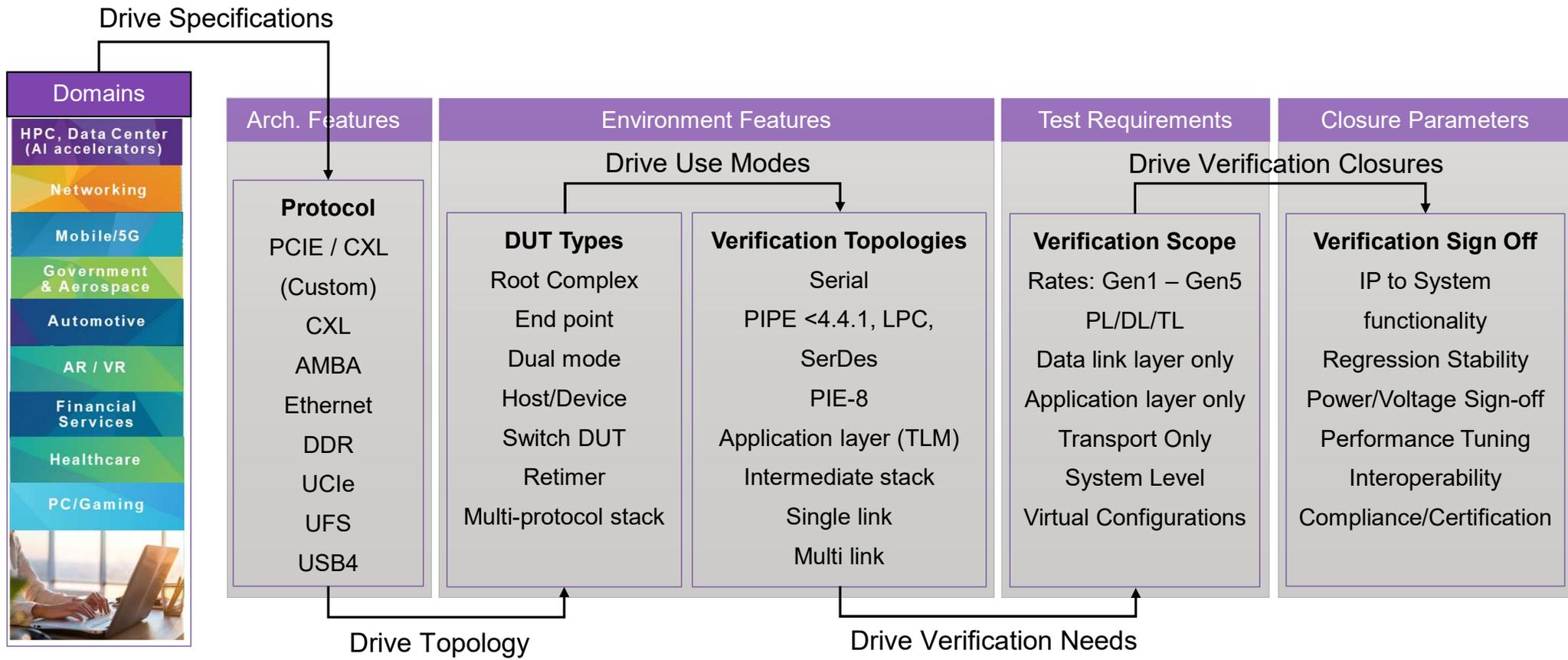
The Growing Need for End-to-end Protocol Verification for IP to Multi-die Systems

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Synopsys

Agenda

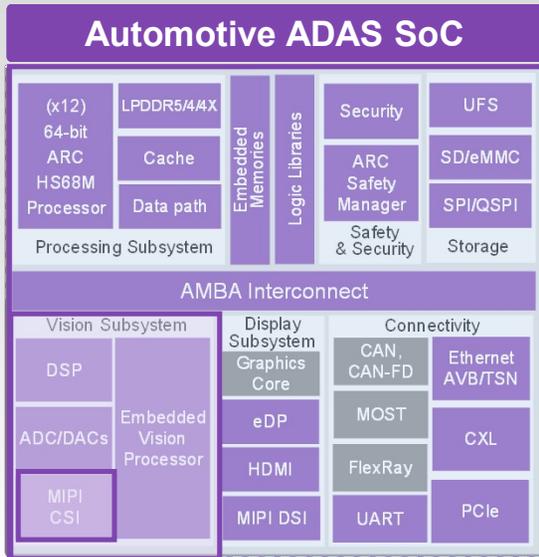
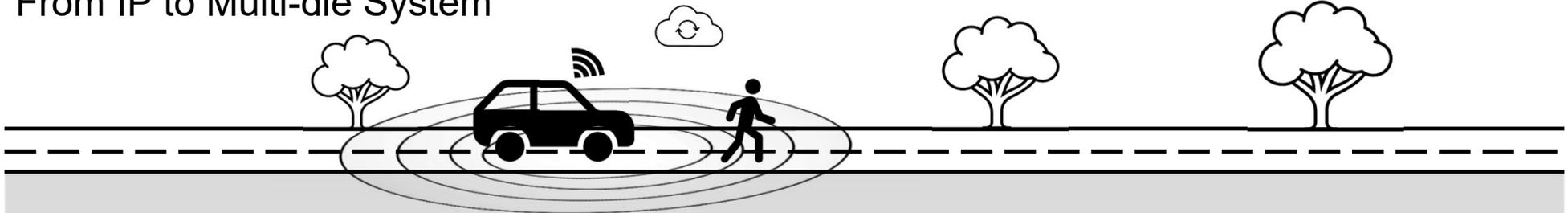
- Drivers for Protocol Verification
- Protocols Verification Journey
- Objectives at Each Use Case
- Protocol Solutions for Each Use Case
- Case Study – Automotive SoC
- Summary
- Demo – PCIe Gen6 Validation using Physical Gen6 Cards

Protocol Verification Drivers



Protocol Verification Journey

From IP to Multi-die System



System Scenario Verification

Real-life scenario-based system validation using Virtual and Hardware-based System Protocol Solutions in Emulation and Prototyping

Sub-system Application Verification

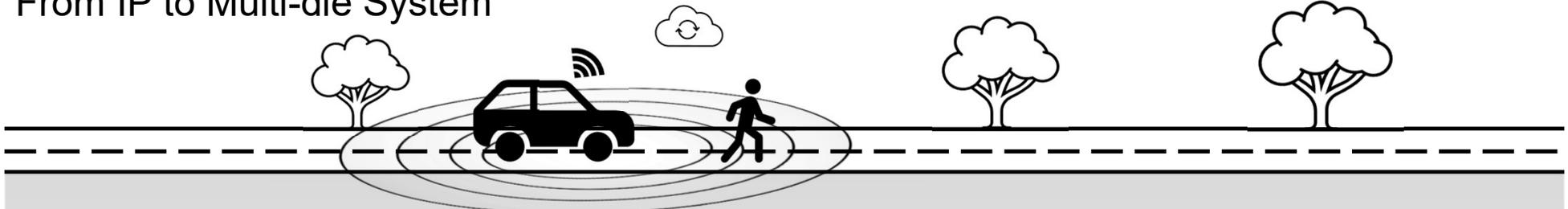
Application-driven subsystem verification and performance benchmarking using VIPs, Transactors, Virtual and Hybrid protocol solutions in Simulation, Emulation and Prototyping

Protocol IP Verification

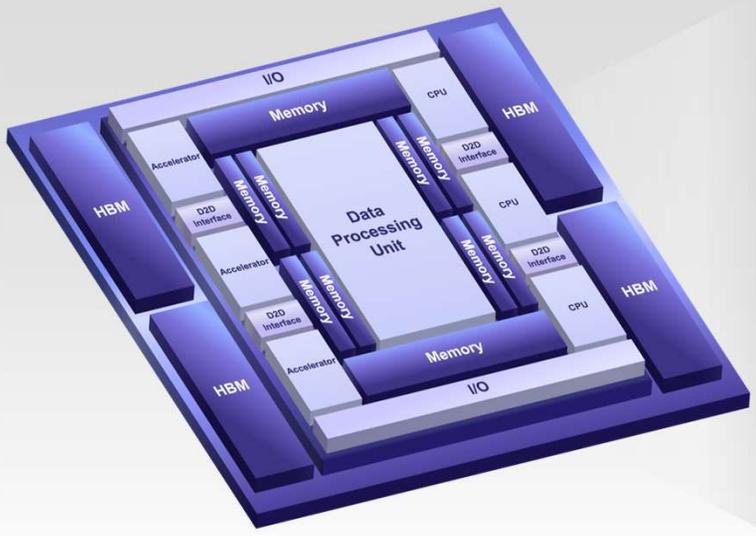
Coverage driven protocol verification using protocol Verification IPs and Test Suites in Simulation

Protocol Verification Journey

From IP to Multi-die System

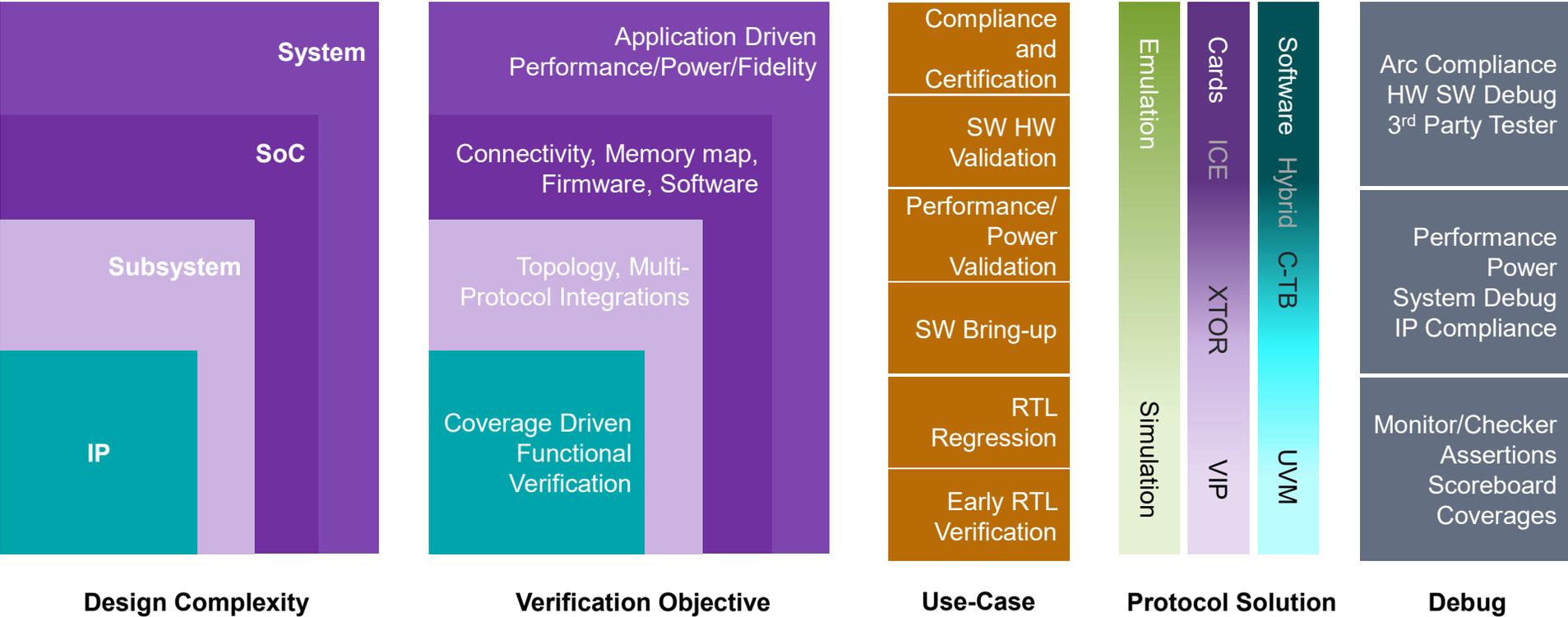


Multi-Die System Integration and Verification



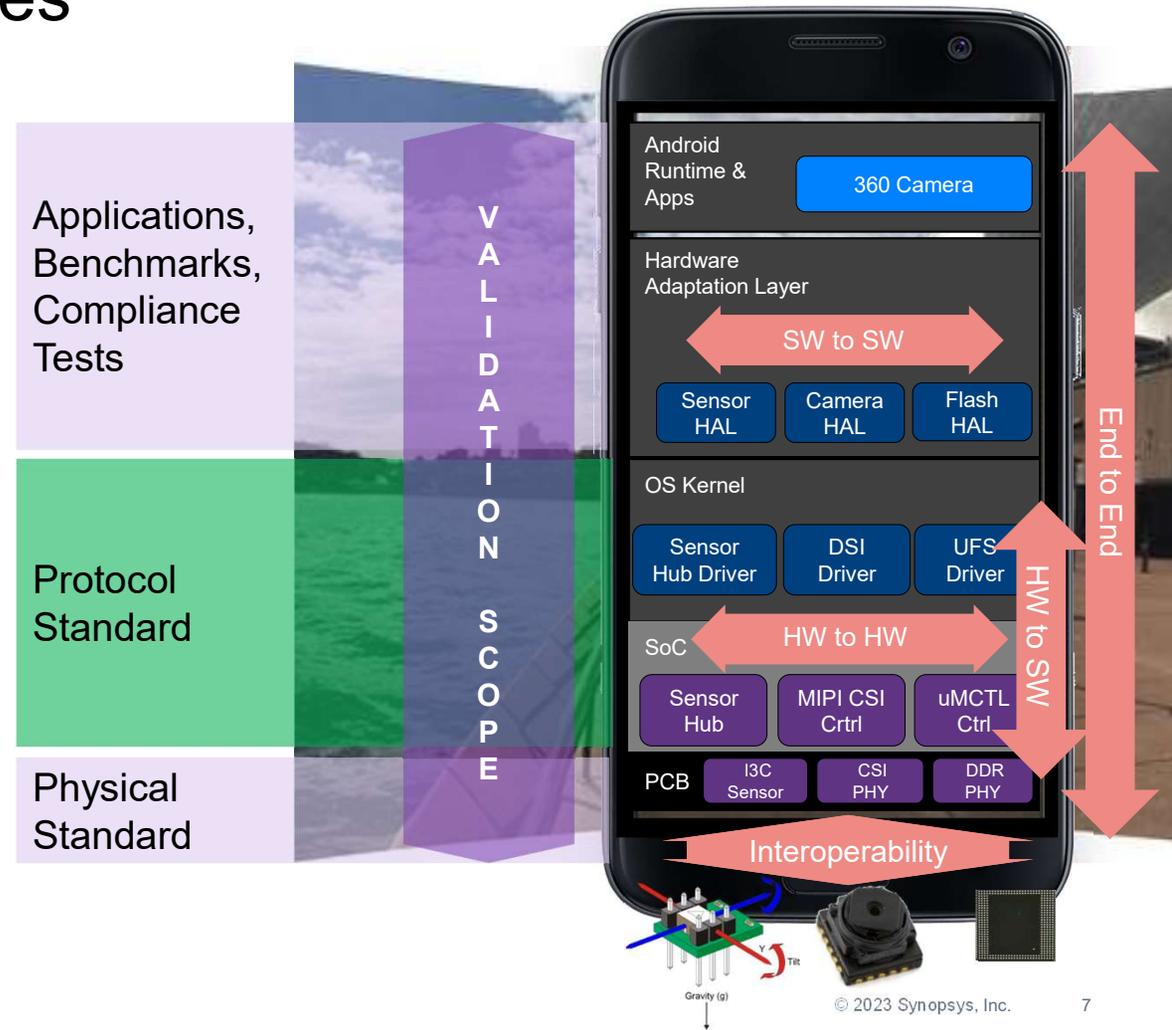
Heterogeneous system integration	Power & thermal management	System pathfinding
Die-to-die connectivity	Software development & modeling	Capacity/performance for system verification
System signoff analysis	Hierarchical Test & Repair	Reliability & Security
System yield	Memory utilization & coherency	

Protocol Verification Objectives



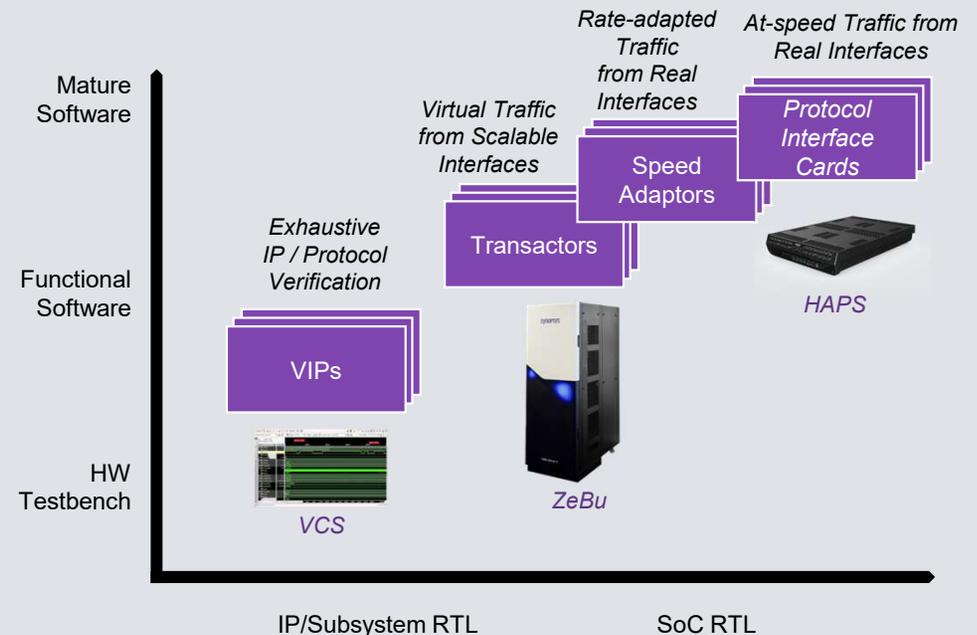
System Validation Objectives

- Protocols in context of IP to system validation against real software and hardware
- Validating system components for
 - **Horizontal** (HW to HW, SW to SW)
 - **Vertical** (SW to HW, HW to Peripheral)
 - **End-to-end** system scenarios (Benchmarks, Compliances and Certification)



Protocol Solution Across Use Cases

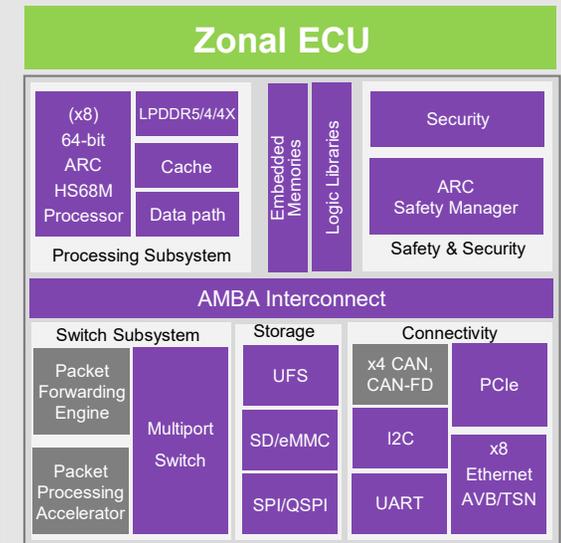
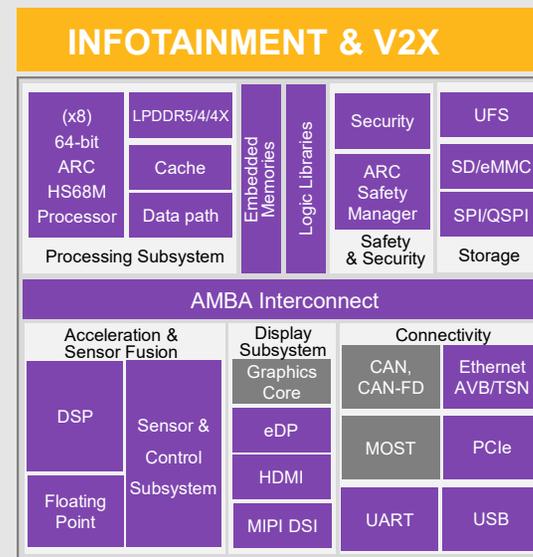
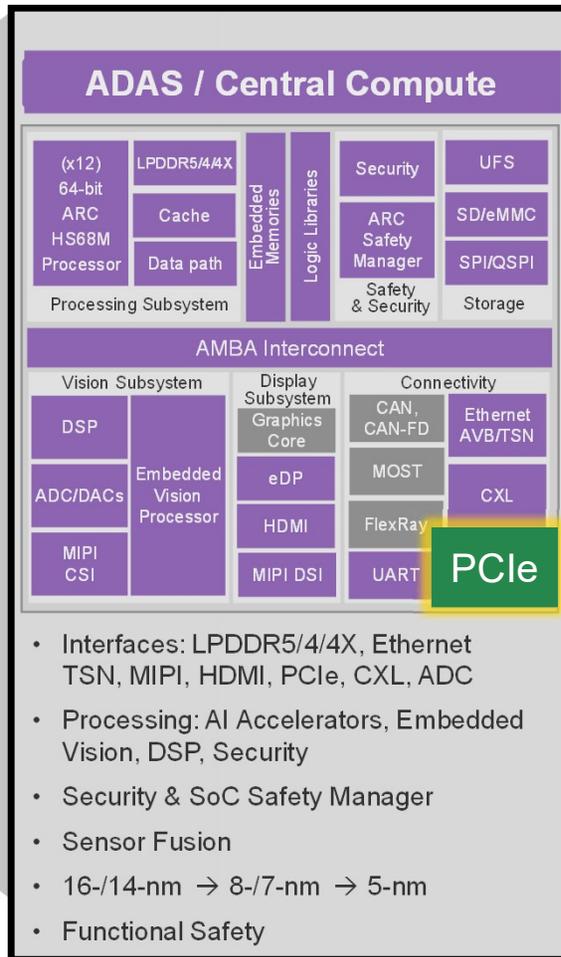
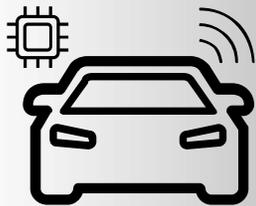
- Getting ahead in the game (TTM) with industry-first protocol verification solutions
- Drive best-in-class QoR with solutions leveraging silicon proven IPs
- Ensure interoperability with broadest eco-system partners
- Shift-left post-silicon use-cases with hybrid and virtual technologies



Automotive SoC Case Study

IP to System-level Closure

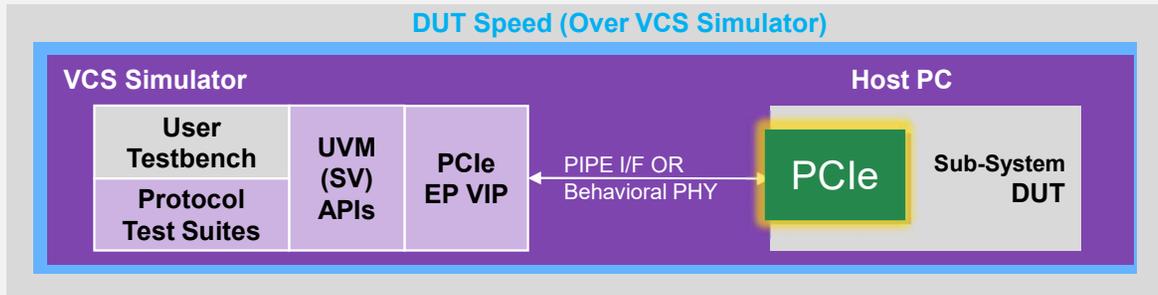
Automotive SoC Architectures



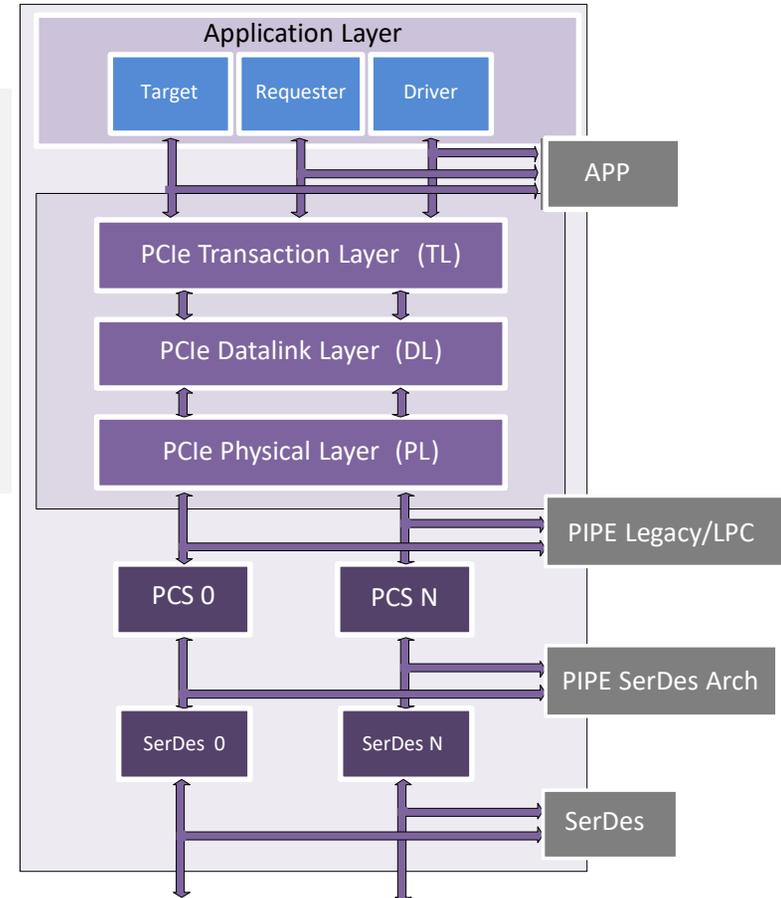
Early RTL Verification

PCIe Example

Verification IP



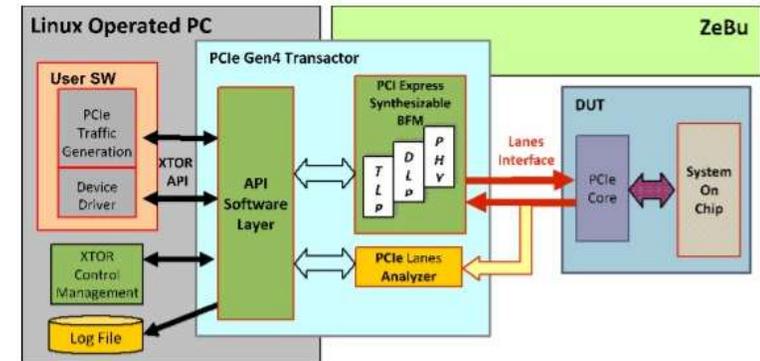
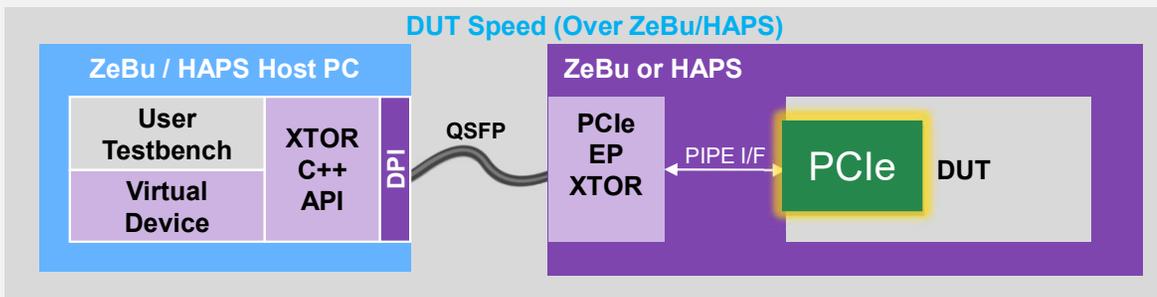
- Behavioral models for Protocols/PHYs
- Connects to DUT through PIPE I/F or PHY I/F
- Complete setup runs on Host PC at DUT speed
- Thorough protocol implementation and checkers (preserves protocol sequence)
- **Key Requirements** – Specification-mapped verification plan, PCIe EP VIP, Test Suites, Highest debug productivity, multiple RTL-turns a day



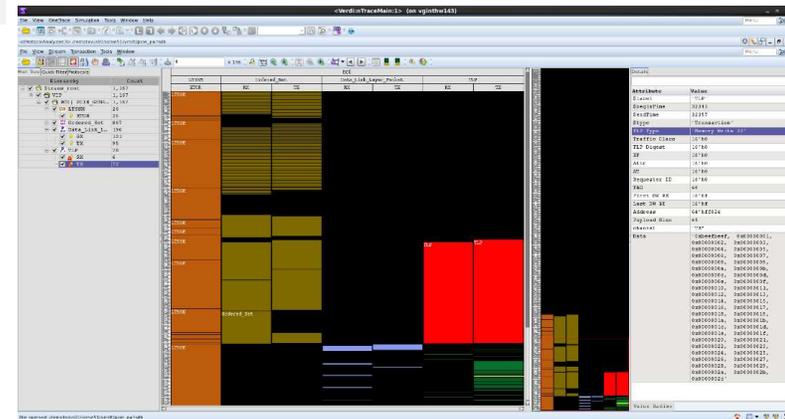
RTL Regression / SoC Bring-up

PCIe Example

Transactors (XTOR)



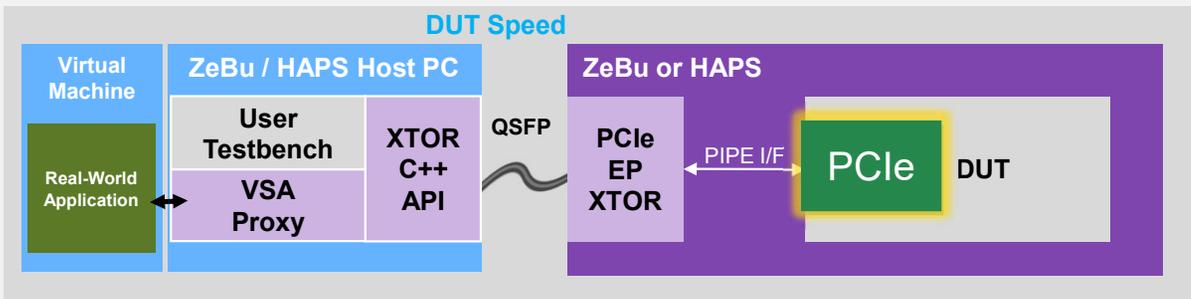
- DUT PHY IP replaced by a XTOR lane or PHY model
- Connects to DUT through PIPE I/F or PHY I/F
- No real-world devices needed
- Virtual device models, running on Host PC, for application and long payloads
- Runs at Multi-MHz DUT speed, preserves protocol sequence
- **Key Requirements** – Simulation speed, high debug, transactional payloads, few RTL-turns



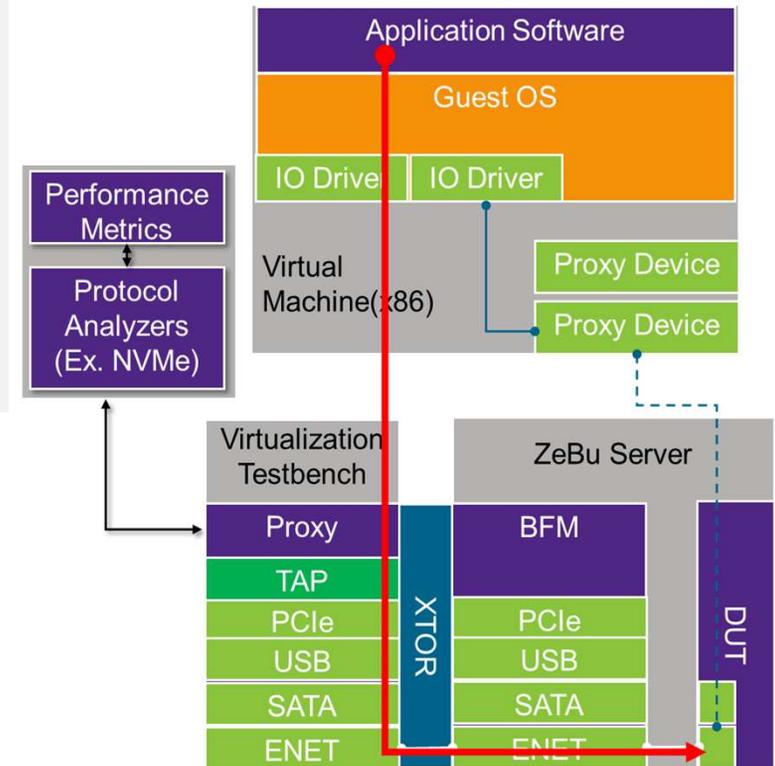
Software Bring-up

PCIe Example

Virtual System Adaptors (Virtual Host Solution)



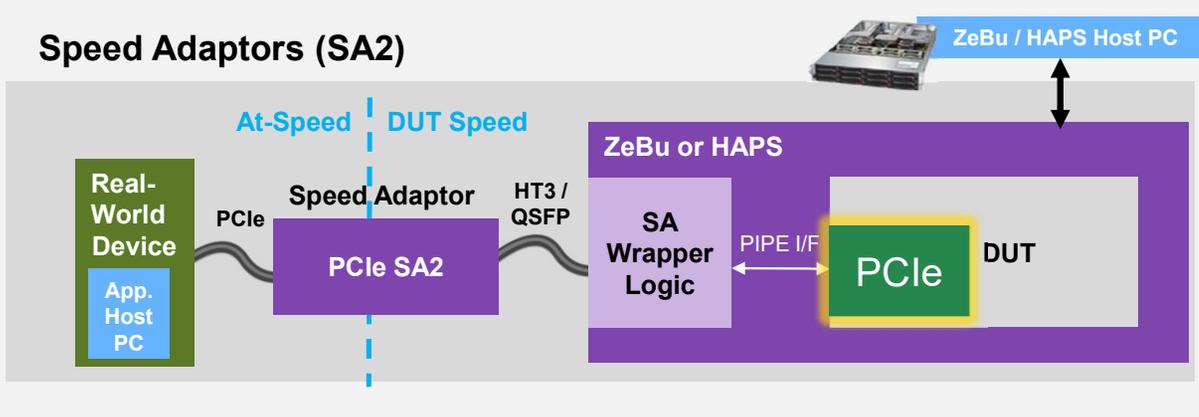
- DUT PHY IP replaced by a XTOR lane or PHY model
- Connects to DUT through PIPE I/F or PHY I/F
- Real-world applications over Virtual Machine(QEMU) running on host PC
- Full setup runs at Multi-MHz DUT speed, preserves protocol sequence
- **Key Requirements** – Simulation speed, system flow debug, software debuggers support, application platform support, rare RTL turns



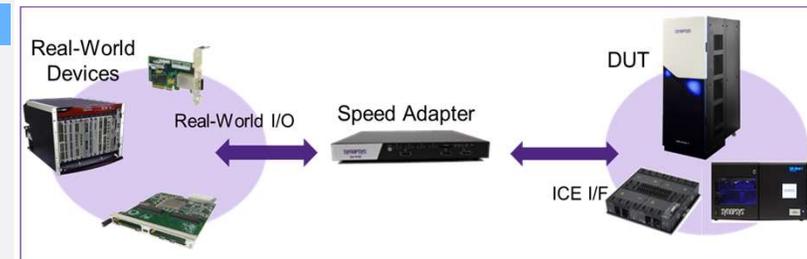
Hardware Software Validation

PCIe Example

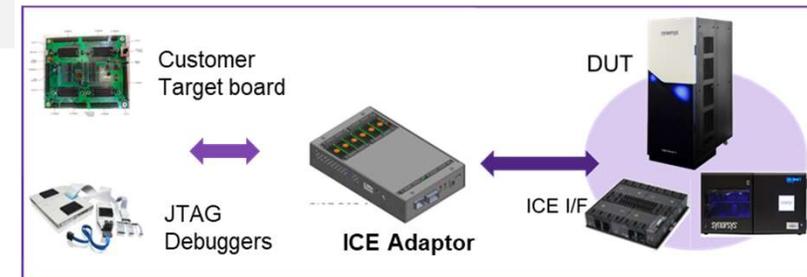
Speed Adaptors (SA2)



- DUT PHY IP replaced by a speed adaptor wrapper logic
- Real-world devices connect to the speed adaptor
- DUT runs at Synopsys ZeBu / HAPS speed
- Speed adaptor performs rate adaptation from DUT speed to at-speed
- **Key Requirements** – High-fidelity real-world connection, application-level hardware and software debuggers, almost no RTL turns



Speed Adaptors

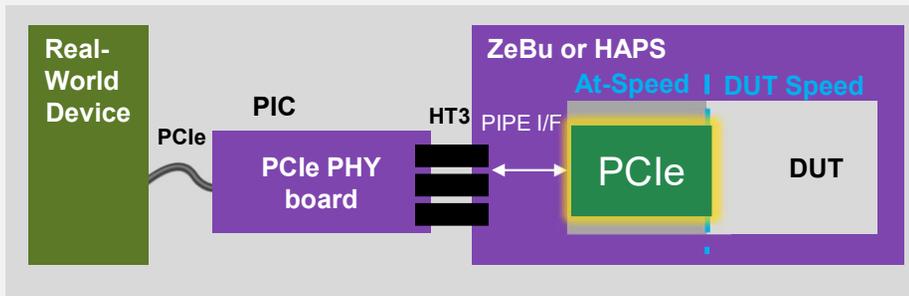


In-circuit Adaptors (At-speed Adaptors)

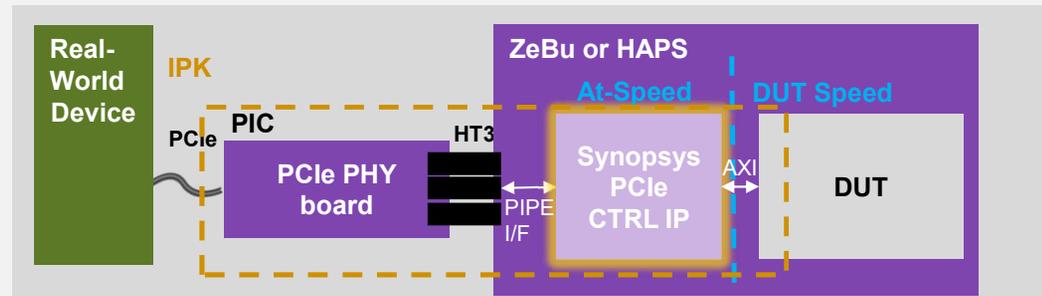
Compliance and Certification

PCIe Example

Protocol Interface Card (PIC)



IP Prototyping Kit (IPK)



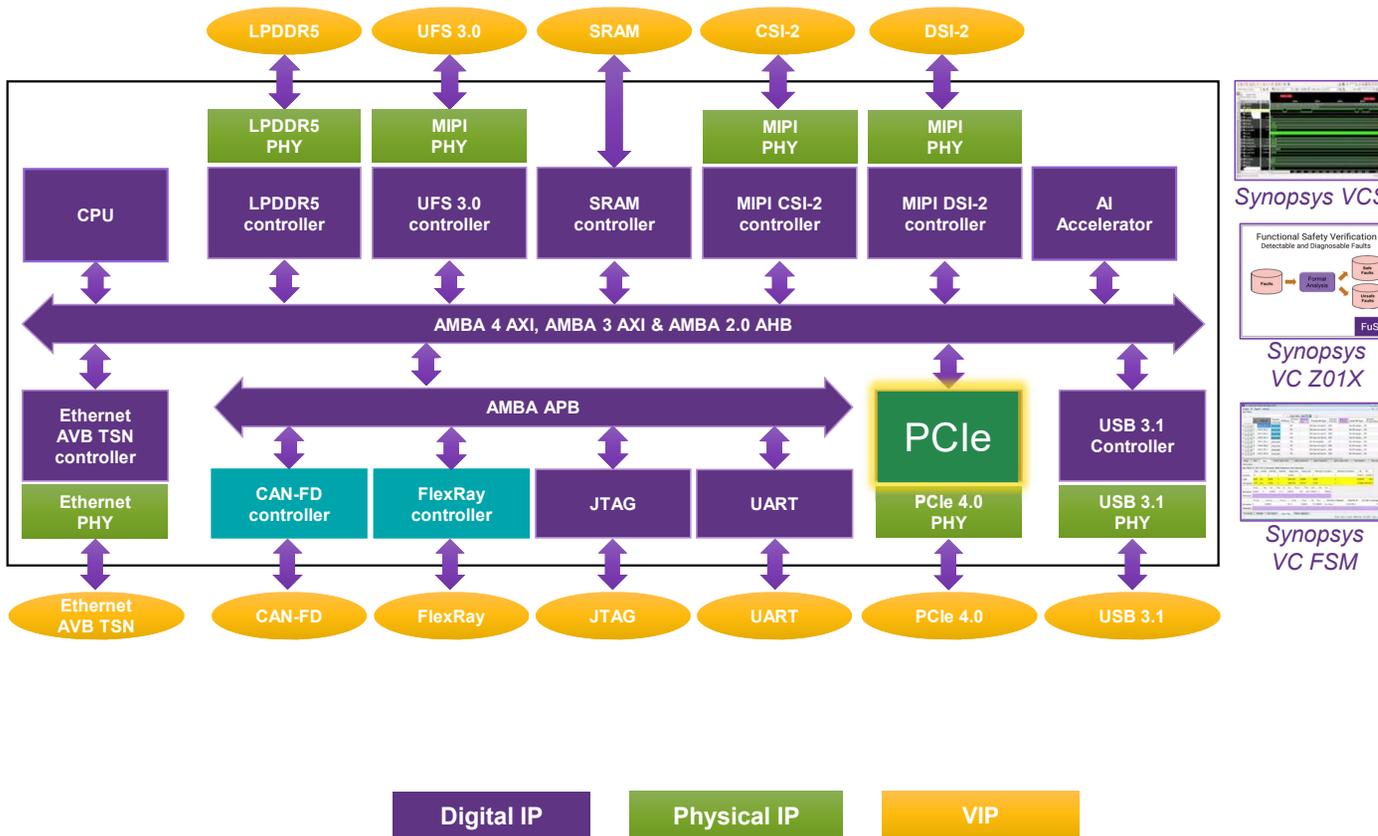
- Card with protocol connector connecting with customer IP or Synopsys IP Reference Kit
- May have a PHY chip or PHY+CTRL chip or Synopsys PHY Board
- Direct connect protocol interface to prototype
- At-speed to DUT speed rate adaptation in the PCIe CTRL or Synopsys PCIe CTRL
- **Key Requirements** – High-fidelity real-world connection, at-speed connection to post-silicon compliance and certification hardware and software, no RTL turns



HAPS PCIe 4.0 EP FIREFLY
 PCIe Gen4x16 Endpoint to Firefly adapter
 5x Firefly connector - 1x PCIe x16 finger
 2x 12-Pin PMOD connector

Functional Safety RTL Verification of ADAS SoC

SoC Level Objective



Synopsys VCS



Synopsys VC Z01X

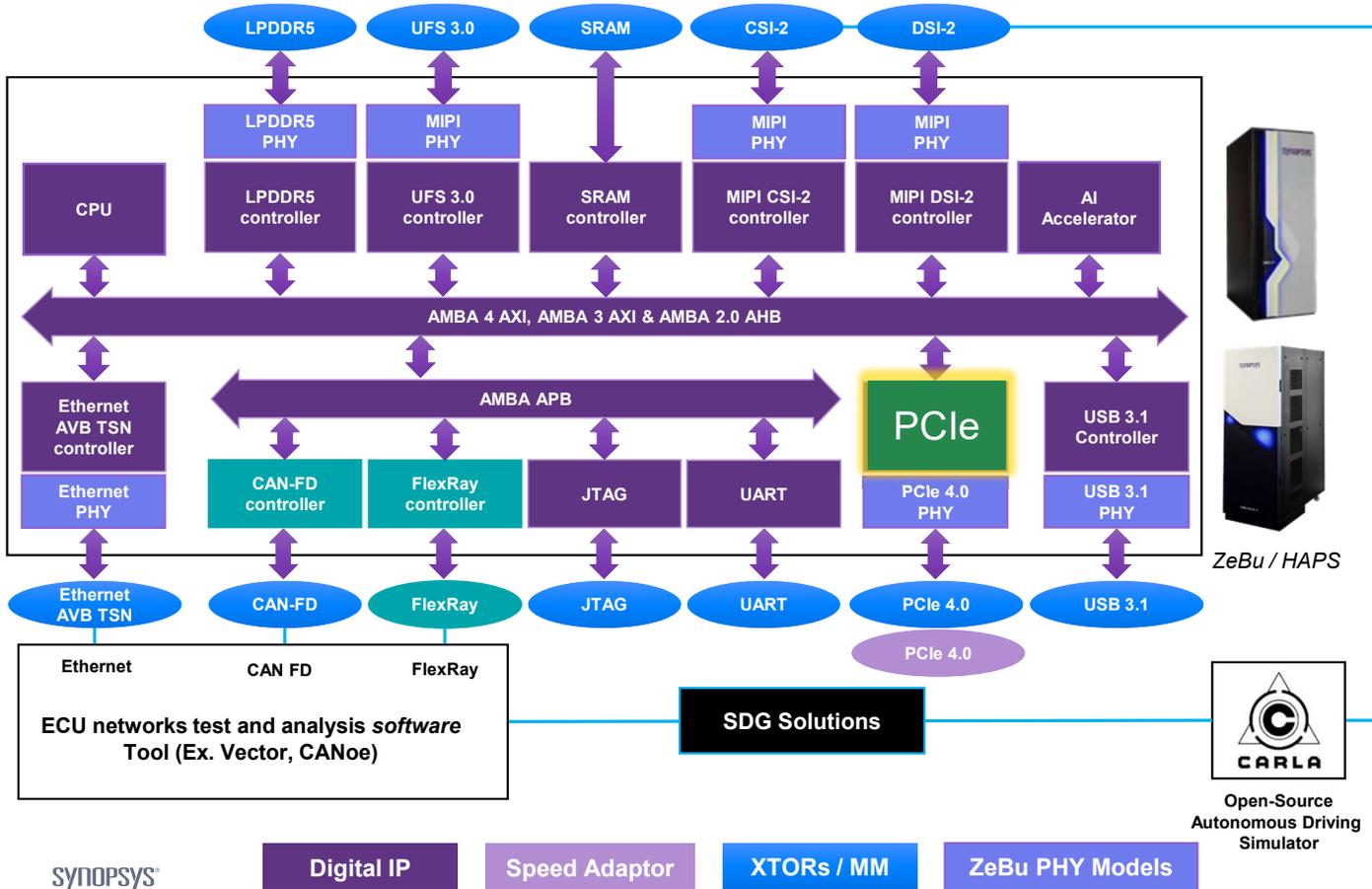


Synopsys VC FSM

- Verification IP
 - Ethernet AVB TSN
 - Flash, LPDDR5, SRAM
 - FlexRay, CAN-FD, JTAG, UART
 - MIPI CSI-2, MIPI DSI-2, PCIe 4.0, USB 3.1, UFS 3.0
- Automotive Specific Use Case
 - Functional Safety Verification with Synopsys VC Z01X
 - Functional Safety Manager for Scalable and collaborative Failure Modes and Effect Analysis (FMEA) and Failure Modes, Effects and Diagnostic Analysis (FMEDA) solution

SW/HW Validation of ADAS SoC

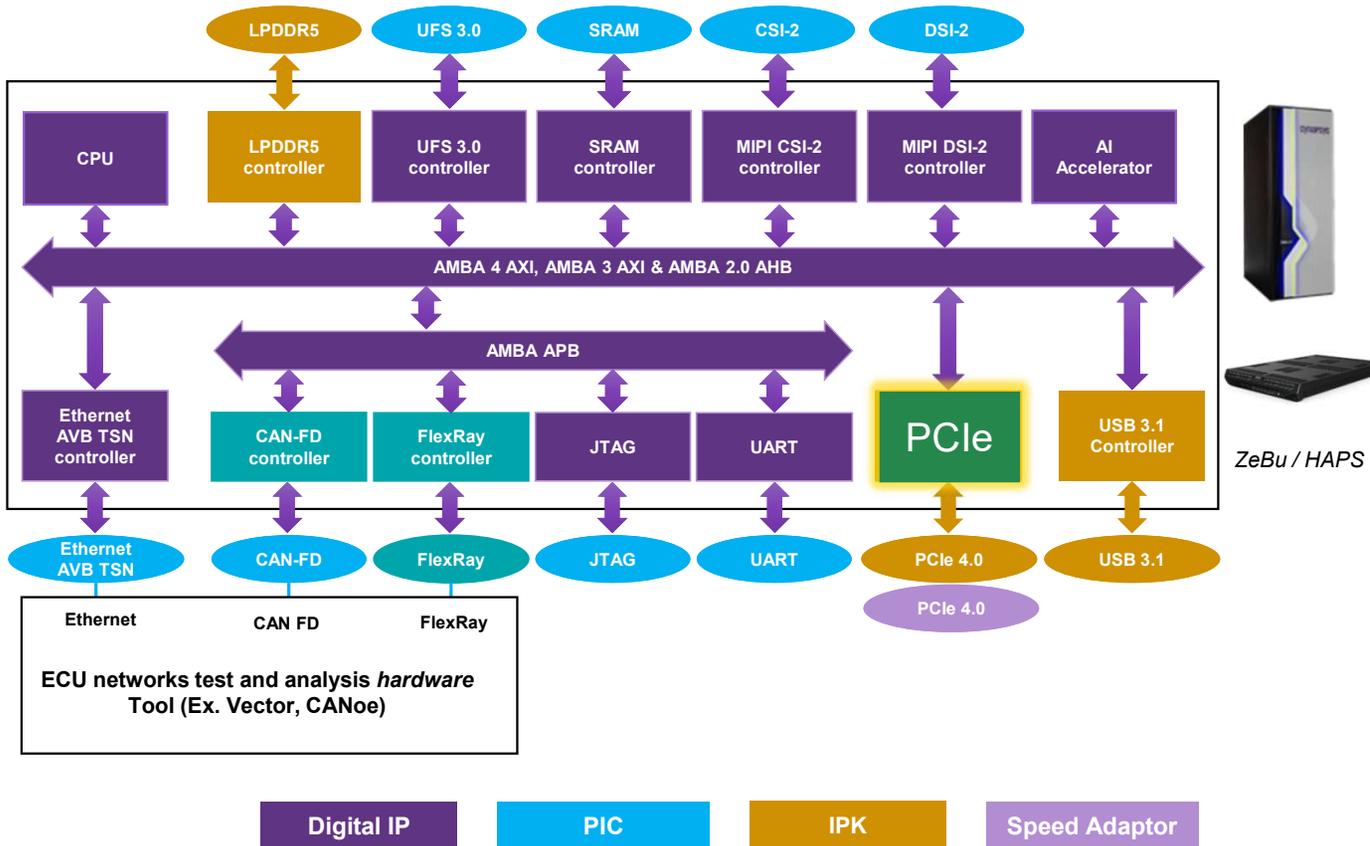
System Level Objective



- Transactors
 - CAN-FD, Ethernet AVB TSN
 - MIPI CSI-2, MIPI DSI-2, USB 3.1, PCIe 4.0, UFS 3.0, JTAG, UART
- Memory Models
 - Flash, LPDDR5, SRAM
- Speed Adaptor
 - PCIe 4.0
- Automotive Specific Use Cases
 - RTL Functional Safety Verification
 - OEM partners SW/HW Validation with ZeBu Cloud
 - Ethernet, CAN, FlexRay Analysis and Testing with VECTOR CANoe
 - Closed loop SoC Performance Analysis (Autonomous driving simulation)

Compliance and Certification of ADAS SoC

Interoperability Objective



- Protocol Interface Cards
 - CAN-FD, Ethernet
 - MIPI CSI-2, MIPI DSI-2
 - UFS 3.0, SRAM, JTAG, UART
- Speed Adaptor
 - PCIe 4.0
- IP Prototyping Kits
 - PCIe 4.0, LPDDR5, USB3.1
- Automotive Specific Use Cases
 - @speed Compliance and Certification for Automotive Ethernet, CAN-FD and FlexRay with VECTOR CANoe + Network Interfaces

Summary

- Protocol verification changes objectives at each stage of product design cycle
- Prevailing IP Re-use, increasing software content, aggressive TTM and shortening product lifecycle leading to aggressive system verification, hardware/software validation, compliance and interoperability requirements
- End-to-end cohesive solutions essential for objective driven protocol verification

DEMO – Industry's only solutions to validate PCIe Gen6 using real Physical Cards!

PCIe 6.0 End-to-End HAPS-100 Prototype Demo



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Thank You

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