2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

SAN JOSE, CA, USA
FEBRUARY 27-MARCH 2, 2023

Verification 2.0 – Multi-Engine, Multi-Run AI Driven Verification

Matt Graham – Verisium Product Engineering

cadence®

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Agenda

- EDA 2.0 and Verification 2.0
- What **is** AI?
- AI Opportunities in Verification
- Multi-Engine, Multi-Run AI-Driven Verification Solutions
- Real World Impact of AI-Driven Verification Solutions

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EDA 2.0 and Verification 2.0

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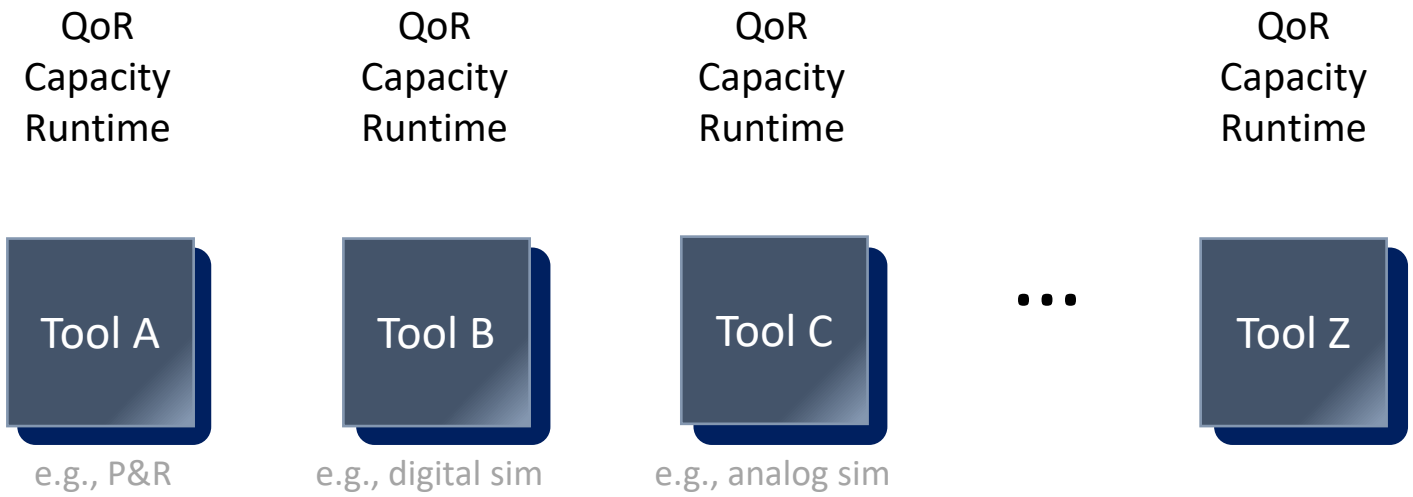
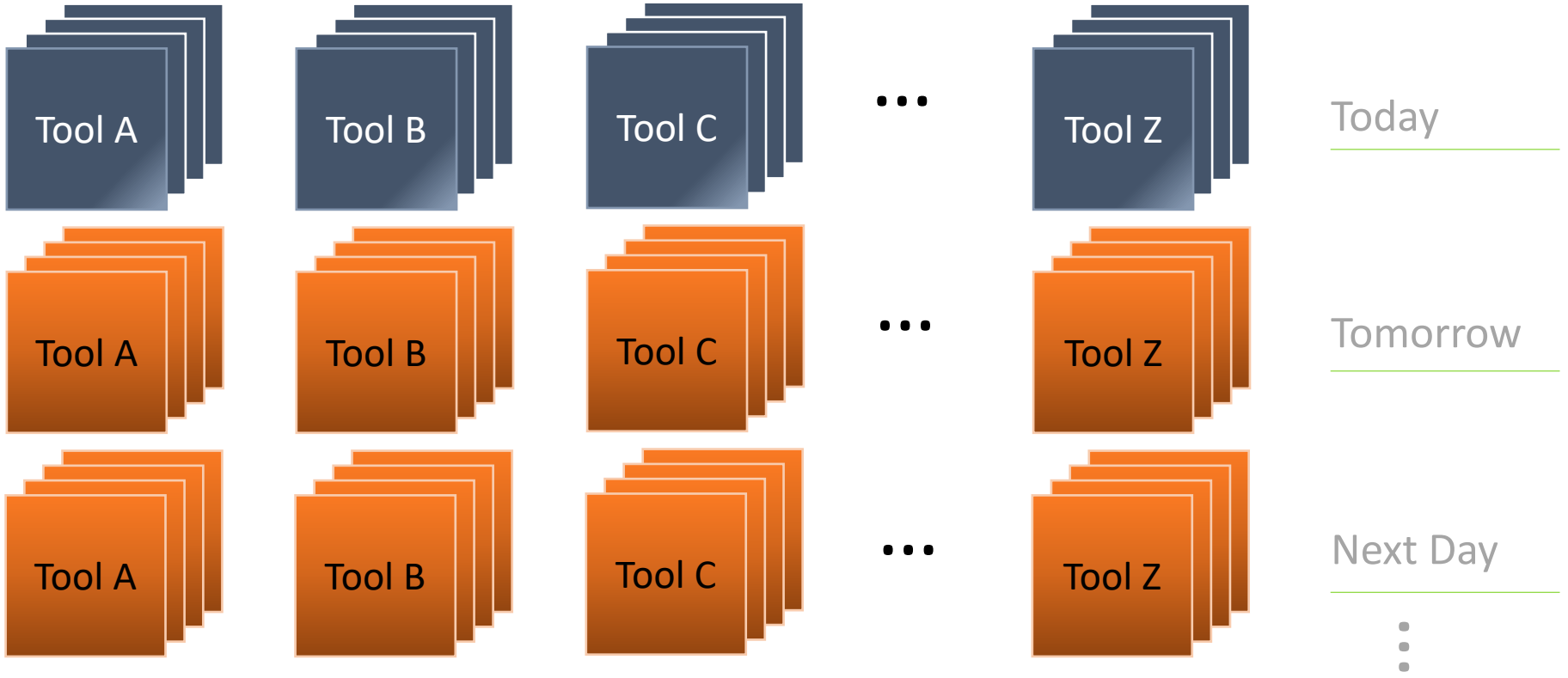
A Generation of EDA 1.0



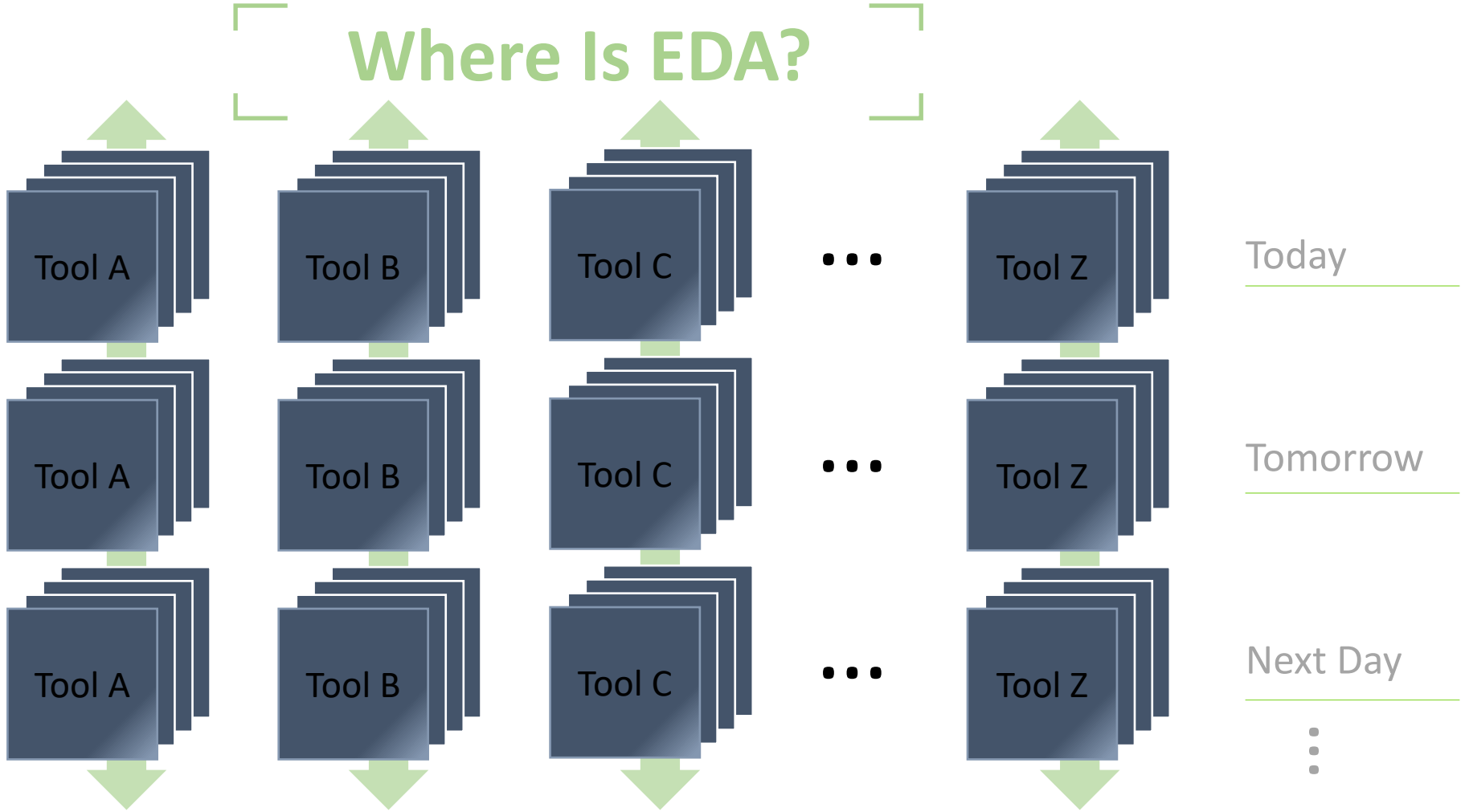
User’s Perspective

User's Perspective

Meet PPA Goals,
Meet Verification Quality Goals



User's Perspective



An Opportunity Exists - EDA 2.0

AI-Driven Design and Verification

Big Data Platform

Optimize PPA
Maximize coverage
Increase productivity

Tool A	Tool B	Tool C	Tool Z	**Today**
Tool A	Tool B	Tool C	Tool Z	**Tomorrow**
Tool A	Tool B	Tool C	Tool Z	**Next Day**

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What is AI?

Artificial Intelligence, Machine Learning and Big Data

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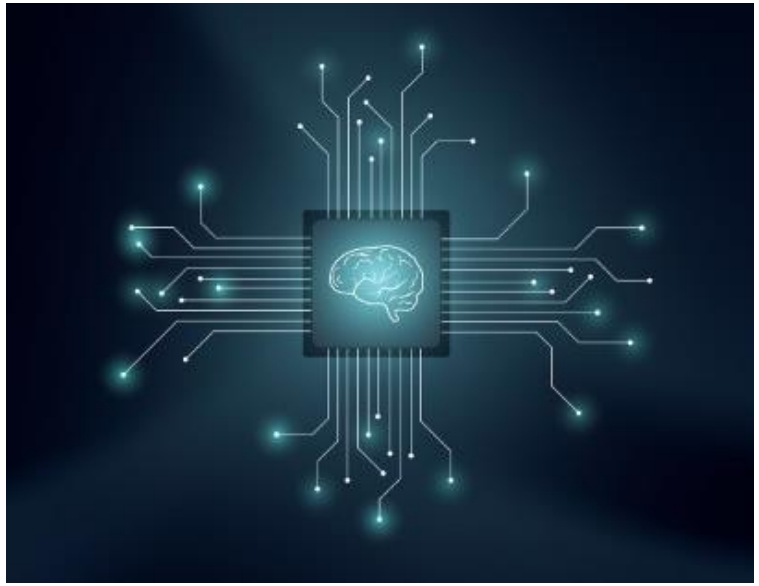
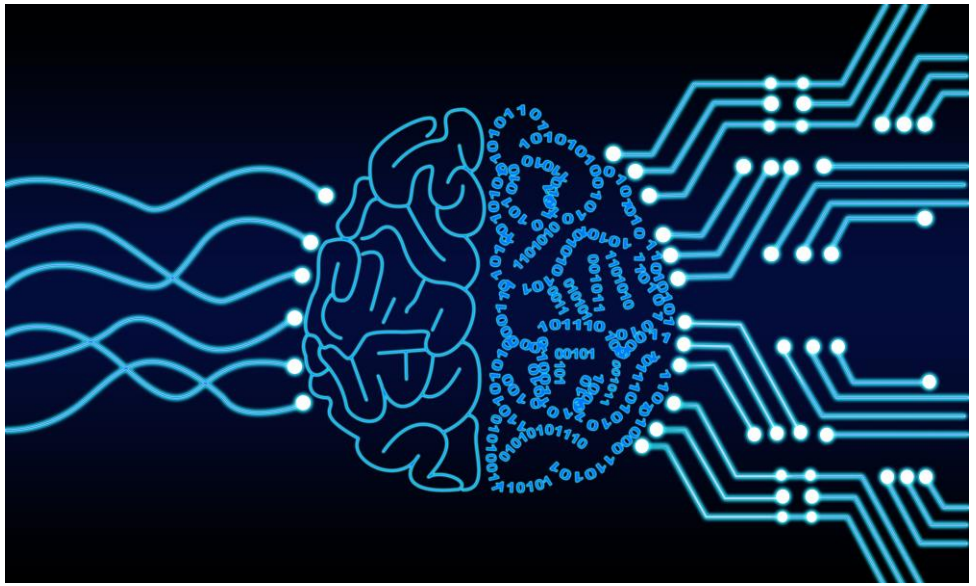
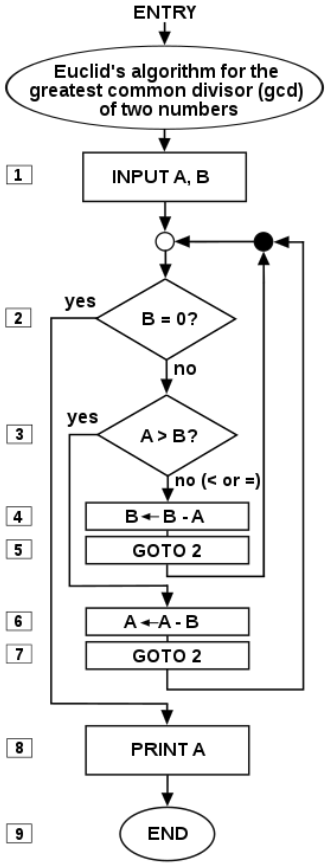
Artificial Intelligence

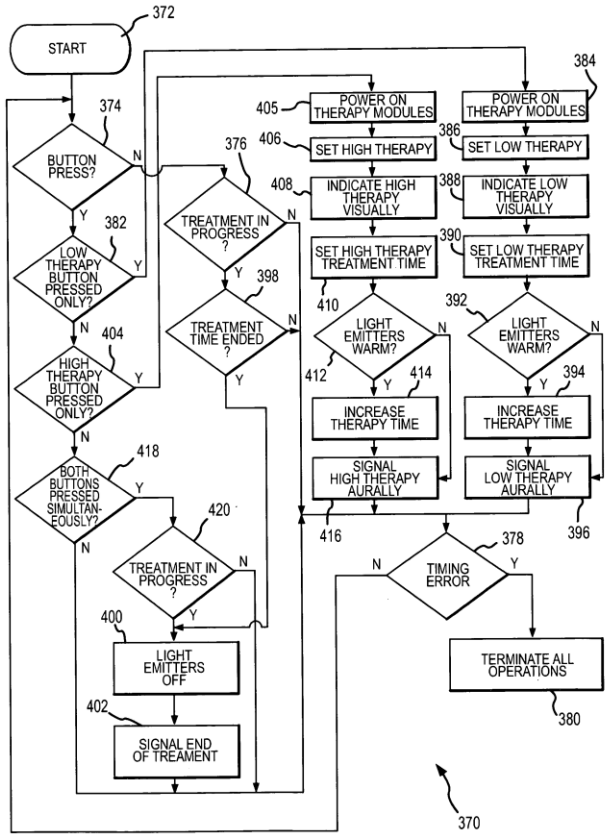




Intelligence demonstrated by machines, as opposed to natural intelligence, displayed by animals including humans

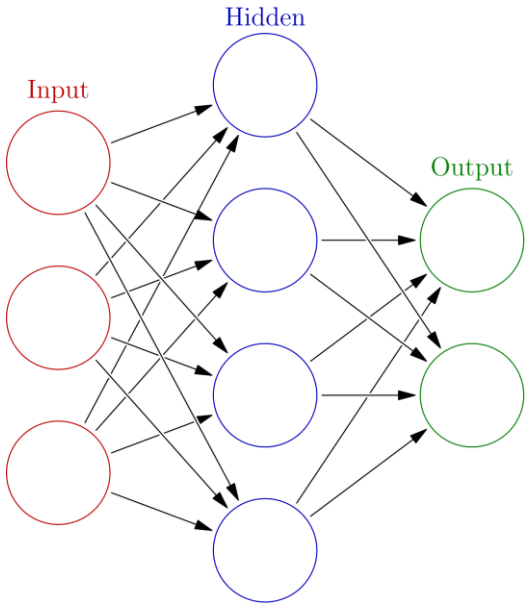
Algorithm

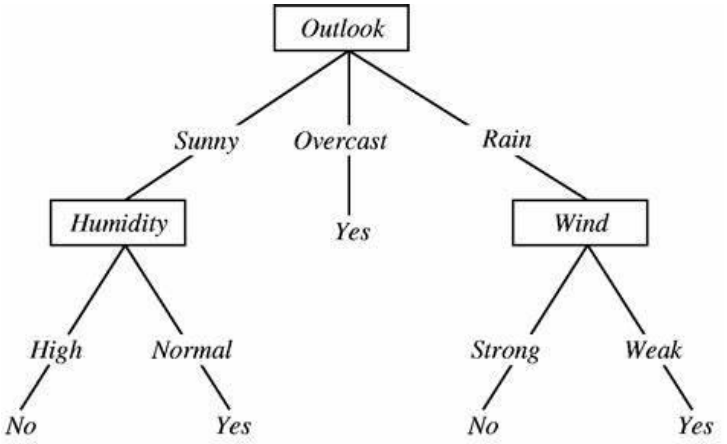


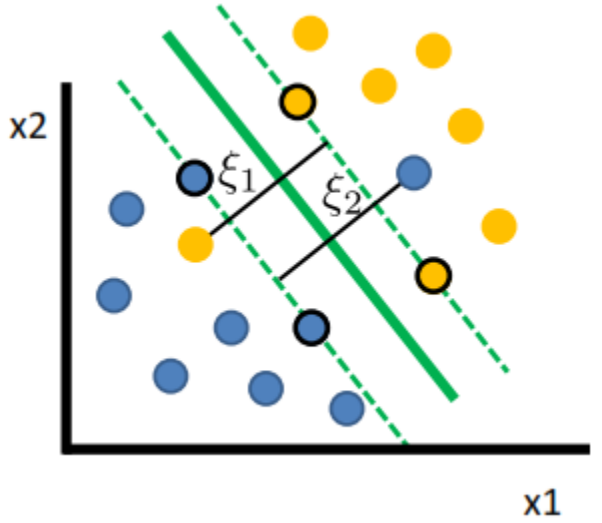


- A finite sequence of well-defined instructions, typically used to solve a class of specific problems or to perform a computation

Machine Learning





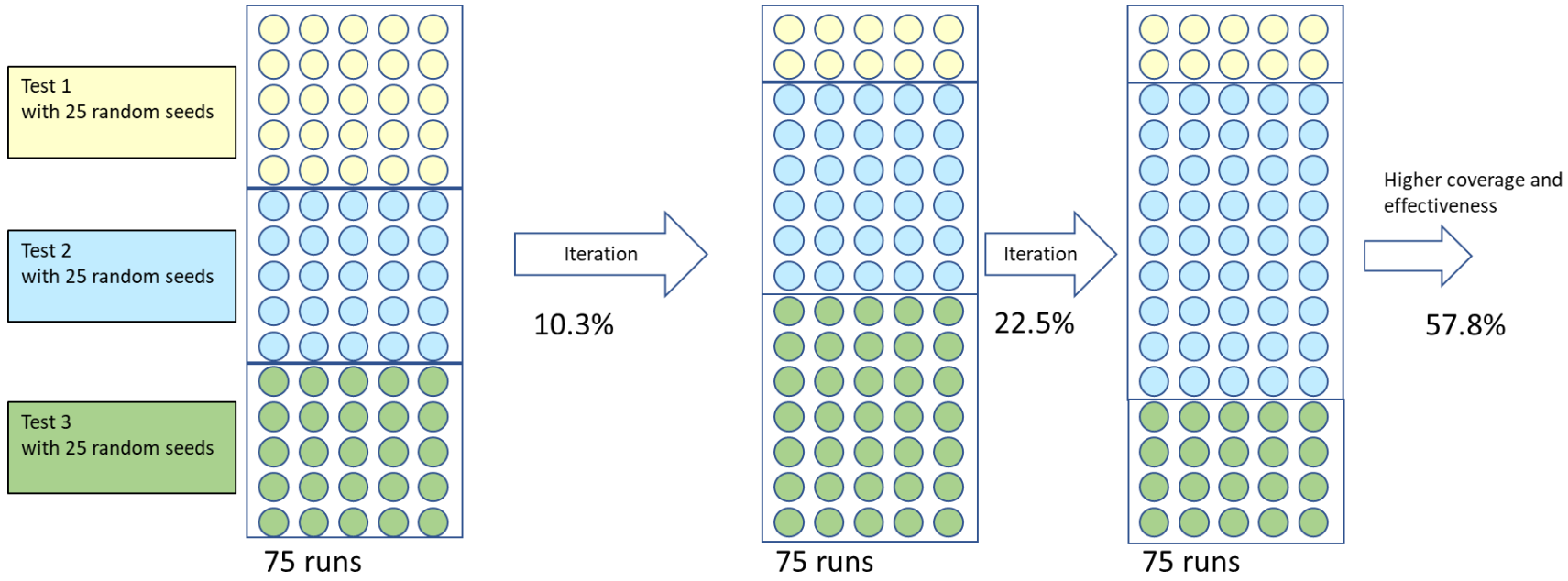


Machine learning (ML) is the study of **computer algorithms** that can **improve automatically** through **experience** and by **use of data**. It is seen as a part of artificial intelligence.

Artificial Neural Networks, Decision Trees, Support-Vector Machines, Genetic Algorithms

Machine Learning or Automation?

Verisium™ Manager Verification Management Test Weight Optimization



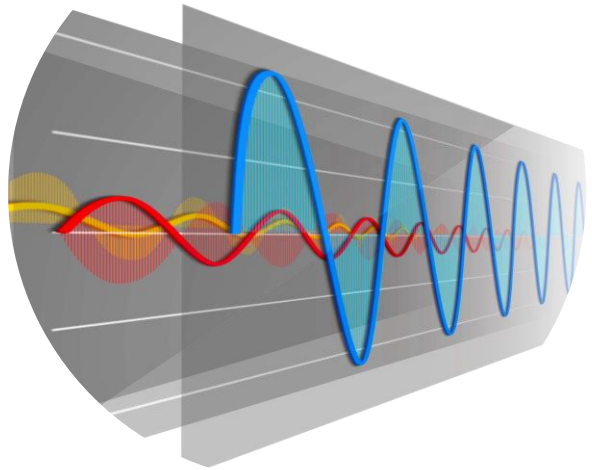
Automated ✓

Algorithmic ✓

Learning ✗

Practical AI in Engineering

- Improve the tool results.
- Replace all the engineers.
- Make the engineers more efficient.



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AI Opportunities in Verification

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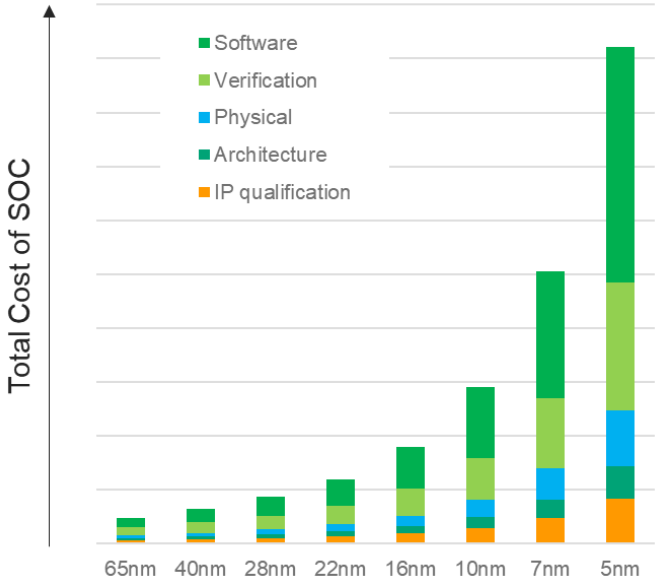
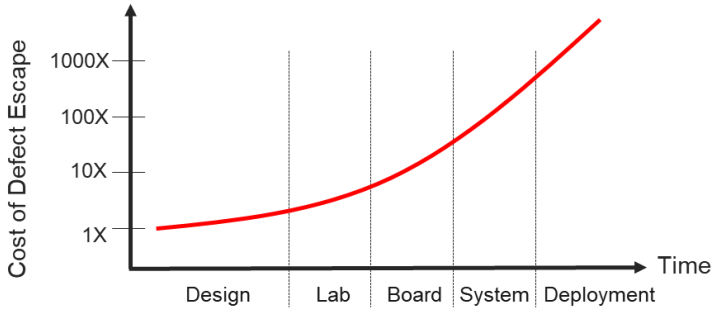
Automation = Throughput

Exponential Challenge

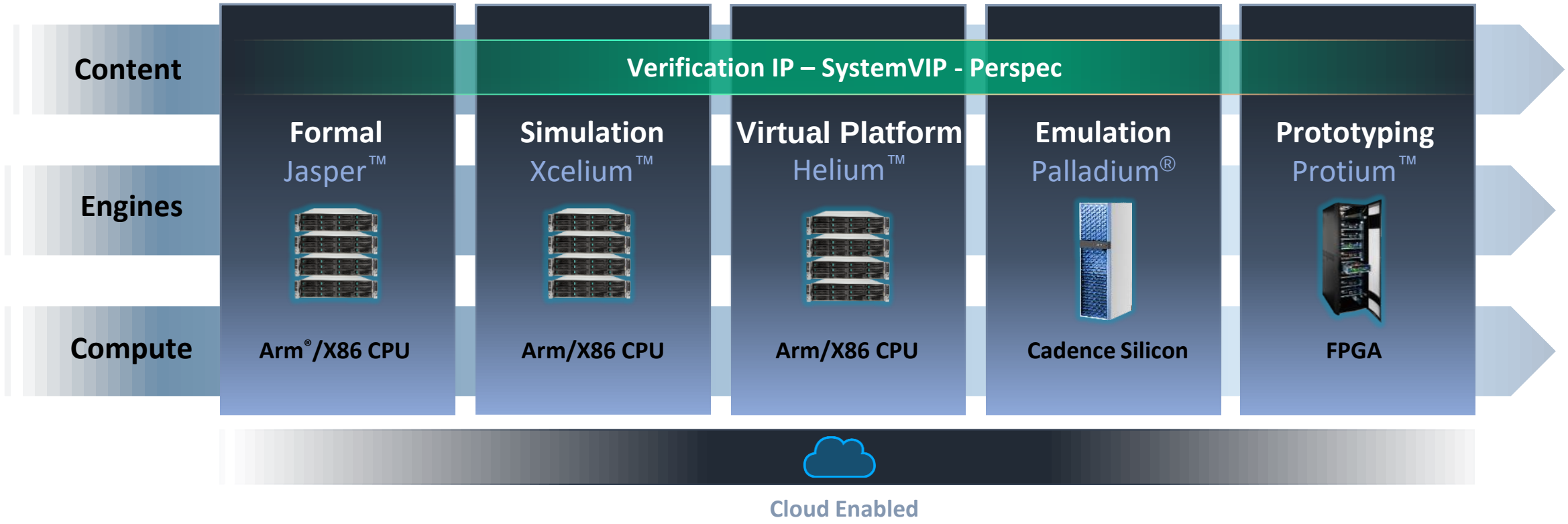




ROI Mindset: Bug closure per $ per day

VERIFICATION THROUGHPUT

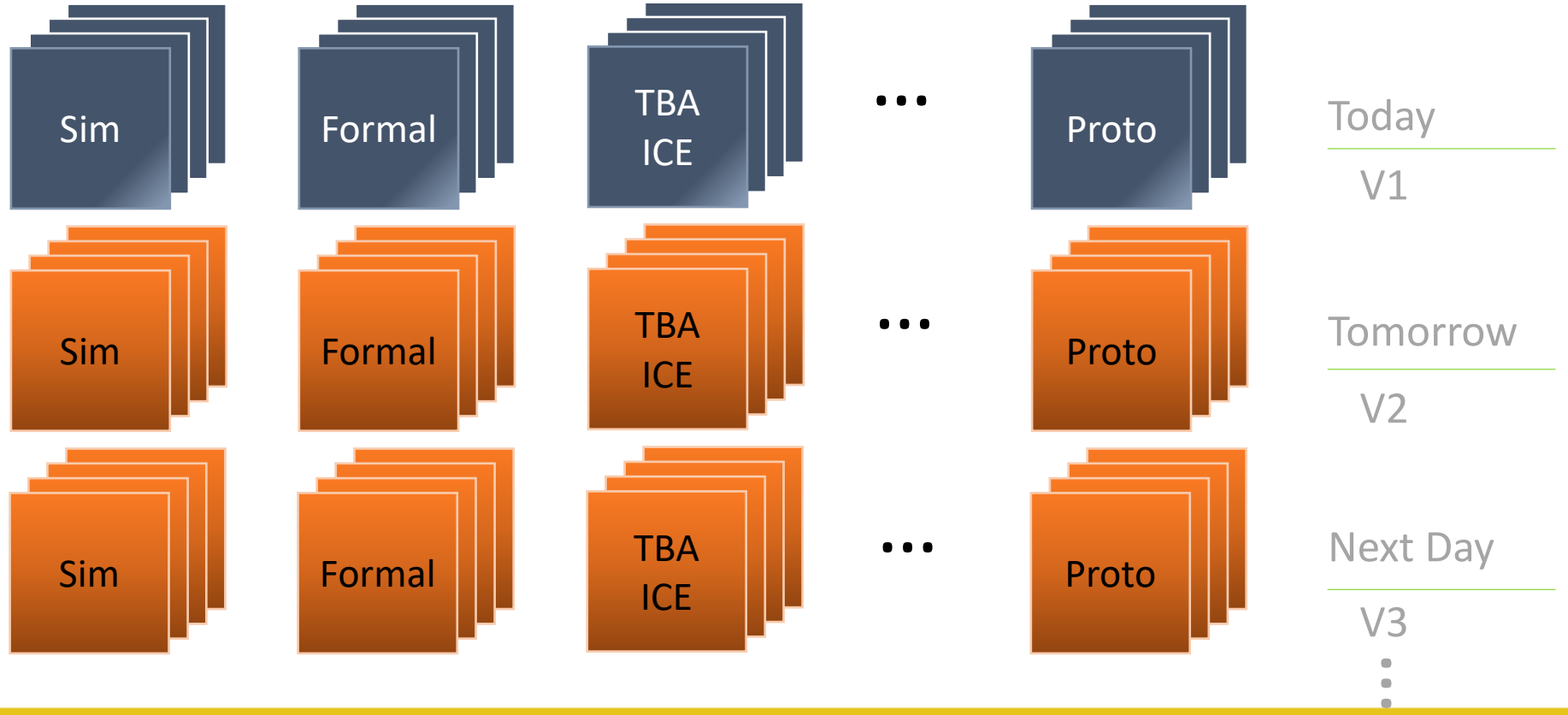
Verification Work Horses



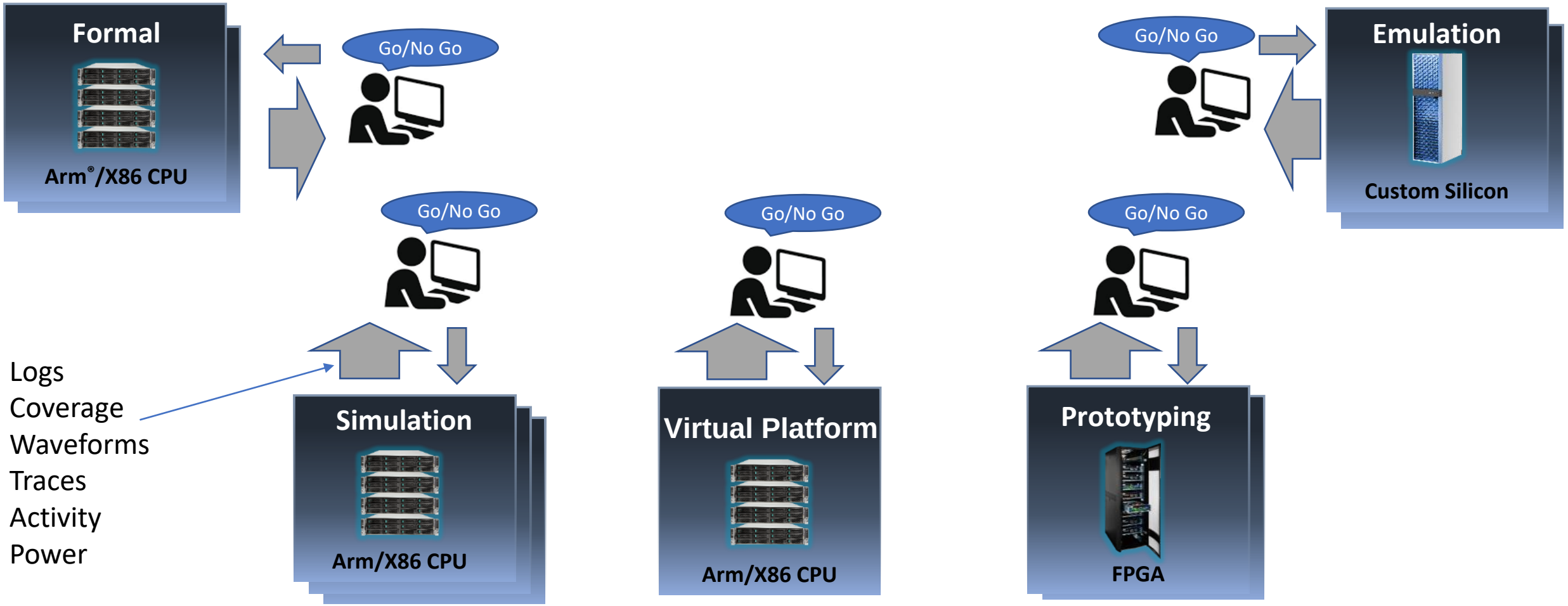
Verification Team Perspective

Meet Verification Quality Goals

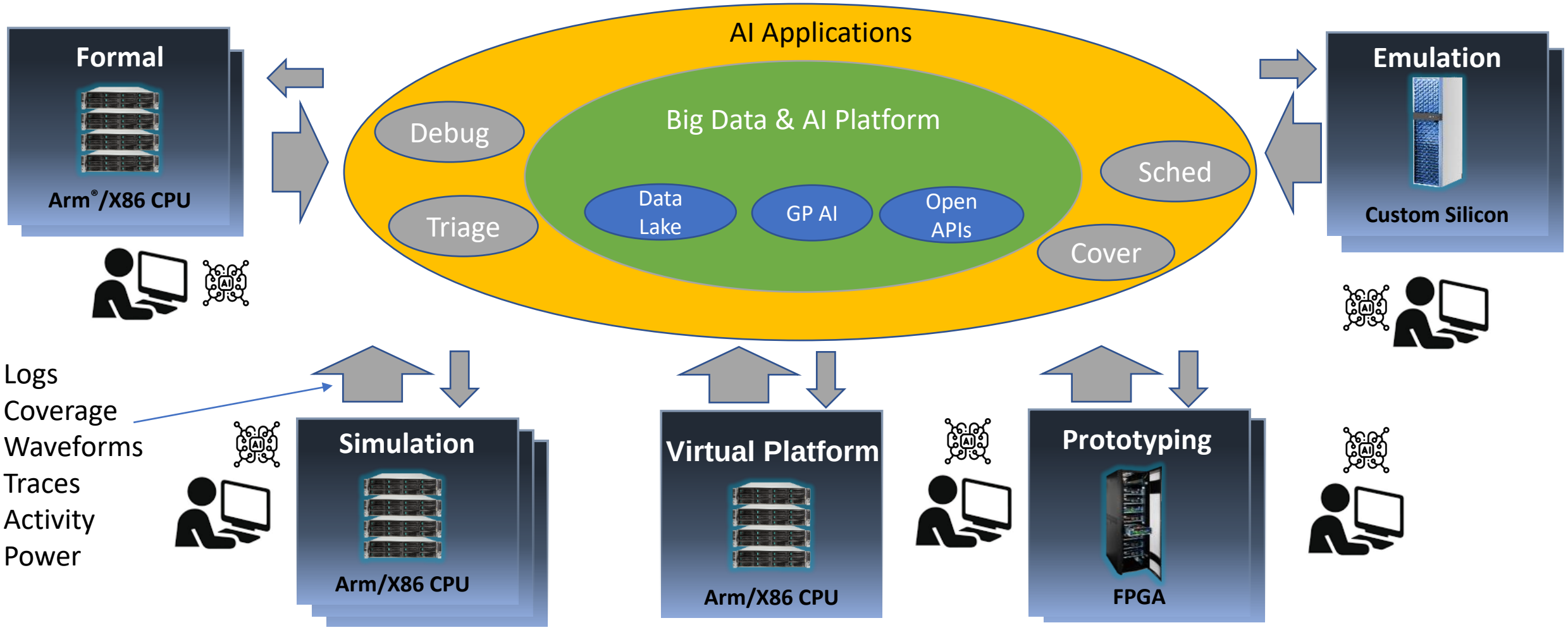
Find bugs - Close coverage



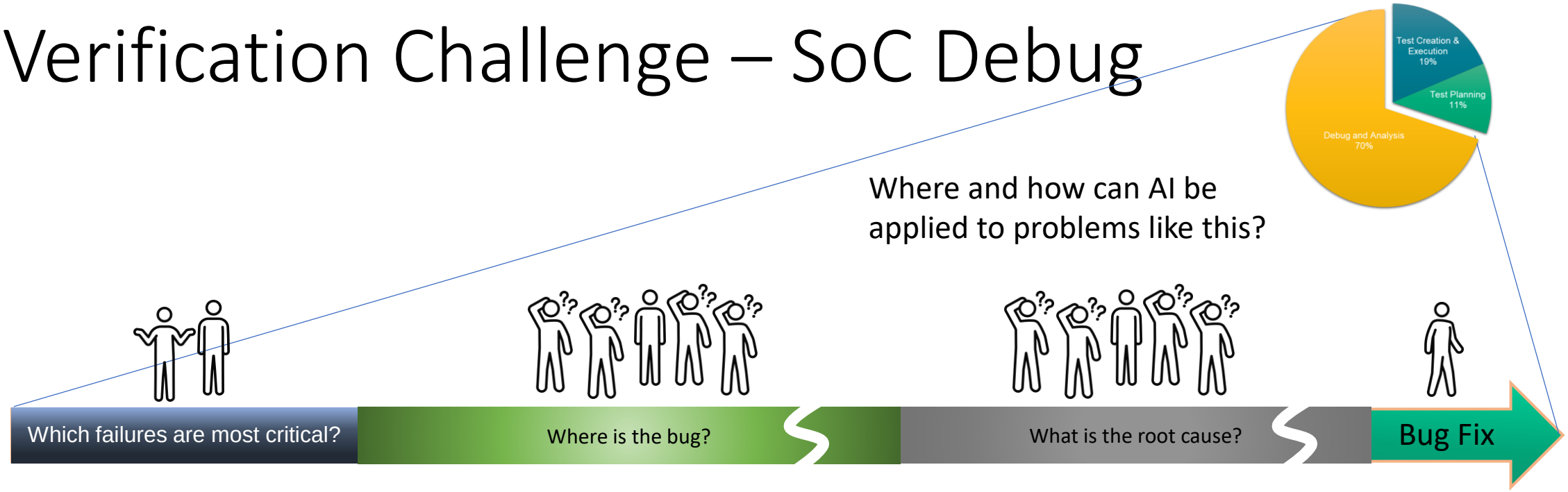
Many Experts, Many Domains, Massive Data.



Big Data & AI Opportunity



Verification Challenge – SoC Debug



- SoCs integrate of hundreds of IP
- Each of the IP is constantly changing, evolving, improving
- Week to week, SoC-level testing results in a number of test failures
- Determining the root cause of the failure requires dozens of engineers and multiple weeks

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Multi-Engine, Multi-Run AI Driven Verification Solutions

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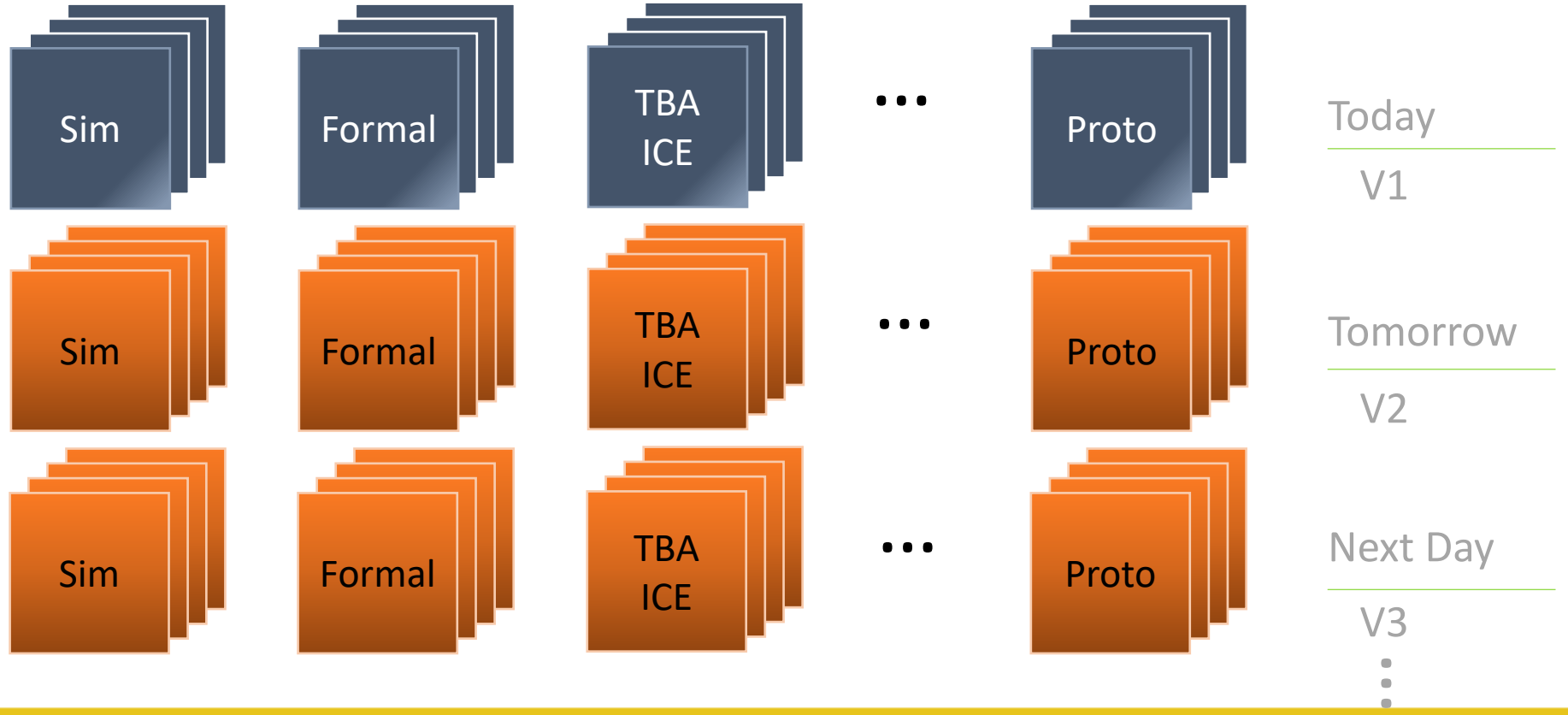
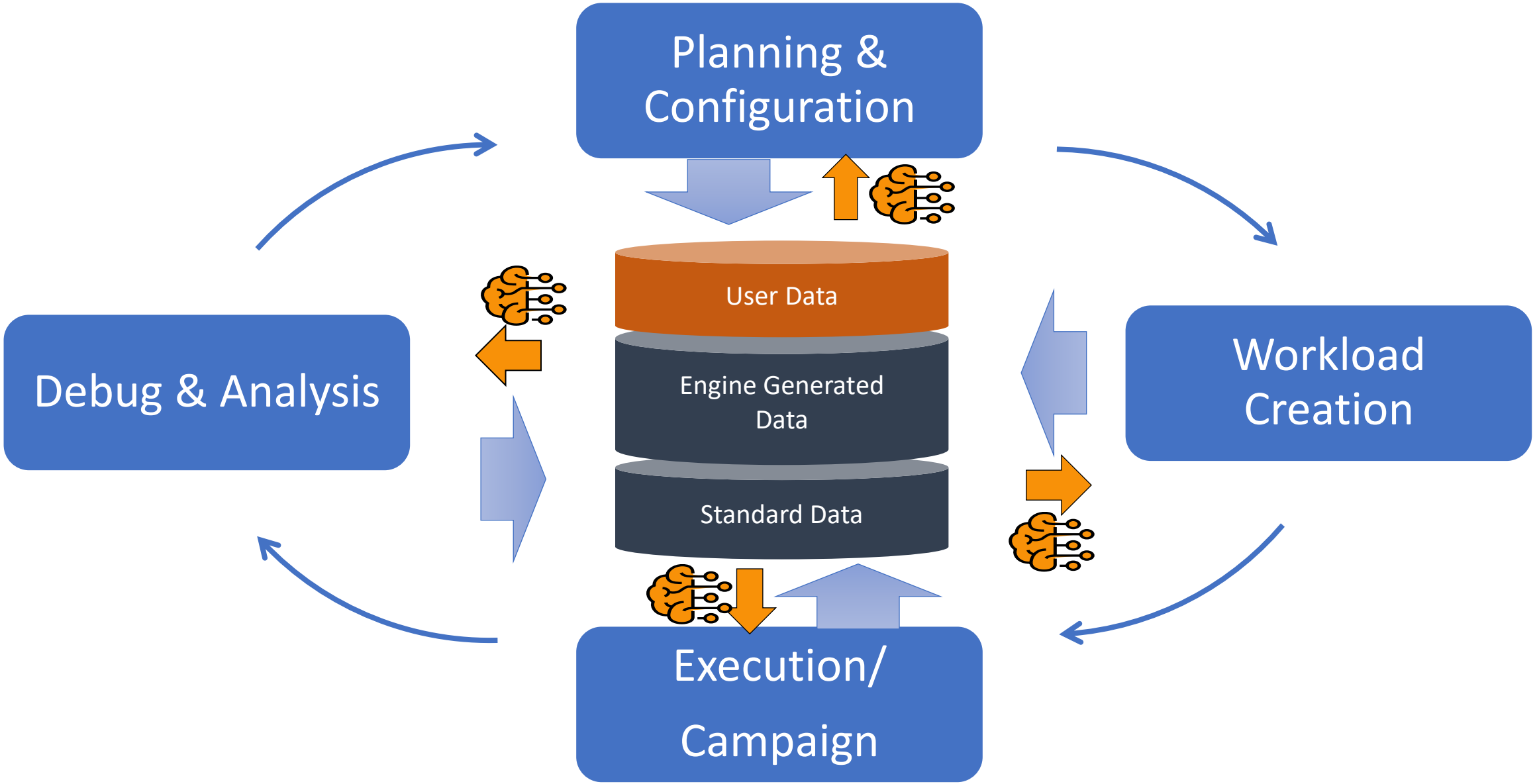
Multi-Engine, Multi-Run Verification

Meet Verification Quality Goals

Find bugs - Close coverage




Planning & Configuration
Workload Creation
Execution/ Campaign
Debug & Analysis
User Data
Engine Generated Data
Standard Data

Opportunities for ML in Simulation

Regression Compression

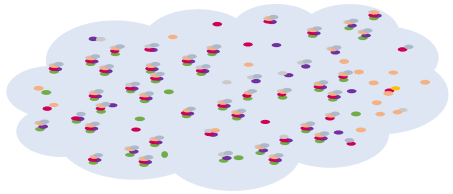
Bins Covered	CPU Time
393226	10052 cpuH

Original Regression

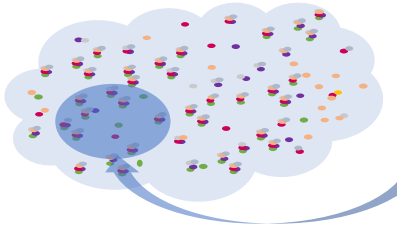
Bins Covered	CPU Time	Regain	Compression
390528	1950 cpuH	99.3%	5.1x

ML Regression

Targeted Regression

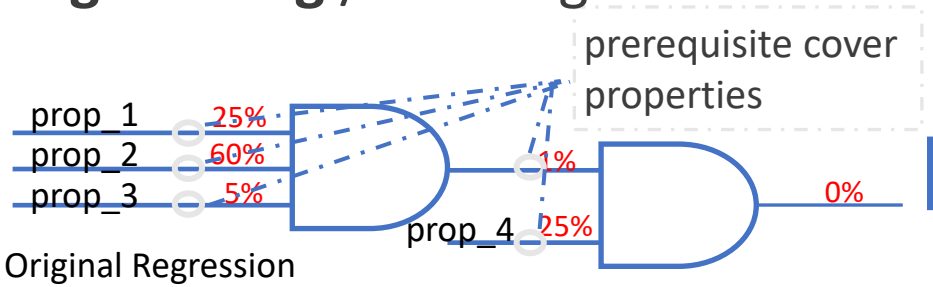


Original regression for full design

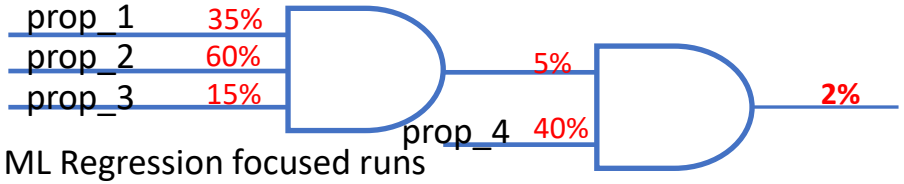


Augmenting runs from ML

Bug Hunting / Coverage Closure



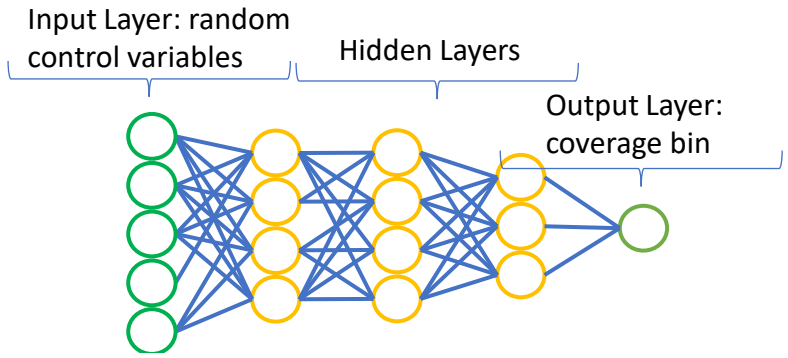
Original Regression

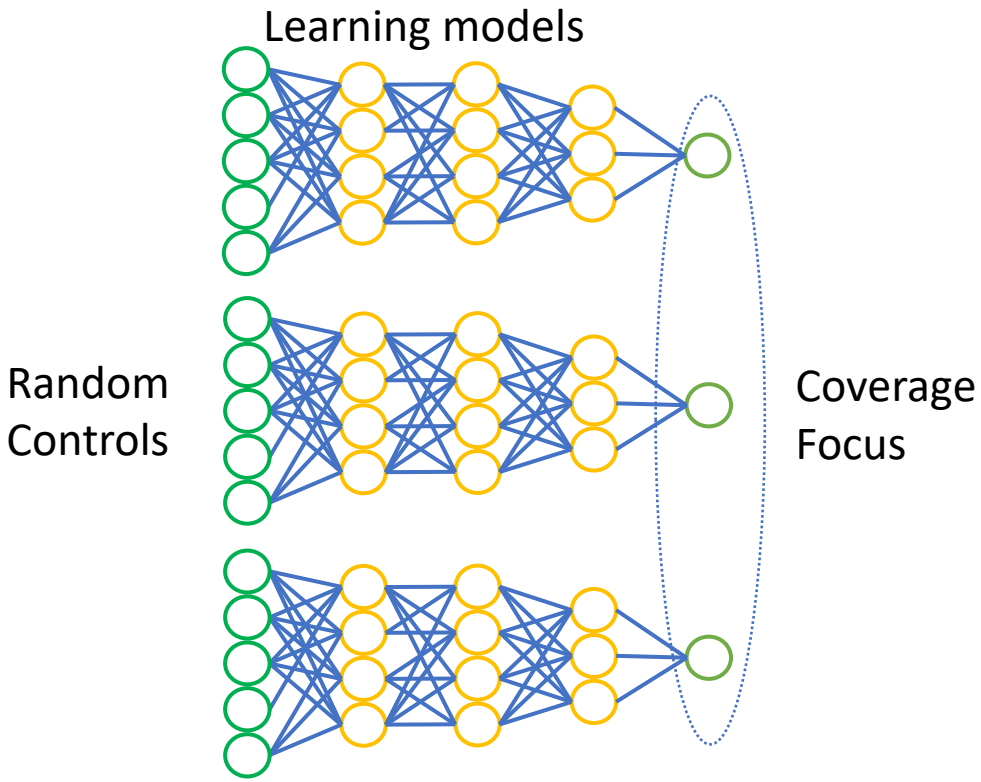


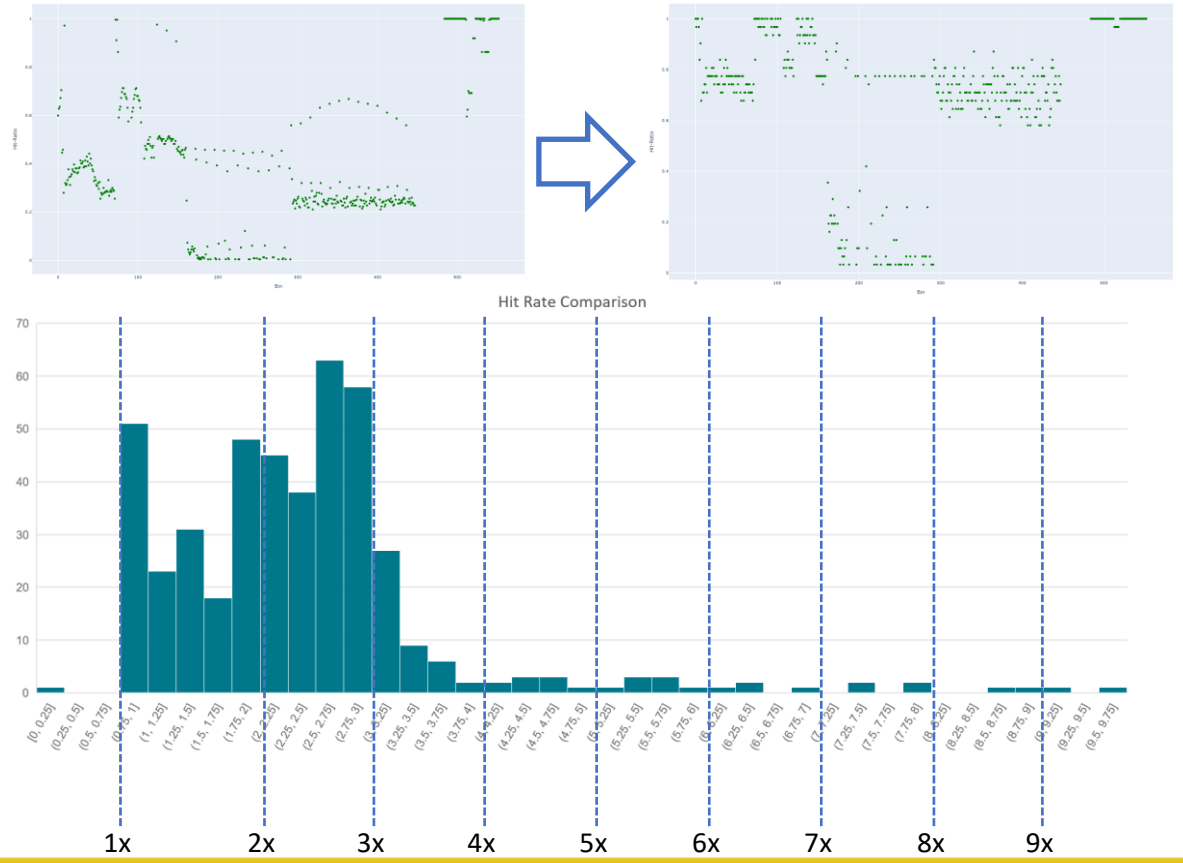
ML Regression focused runs

ML for Coverage Closure

- Synthesize tests to more efficiently hit coverage

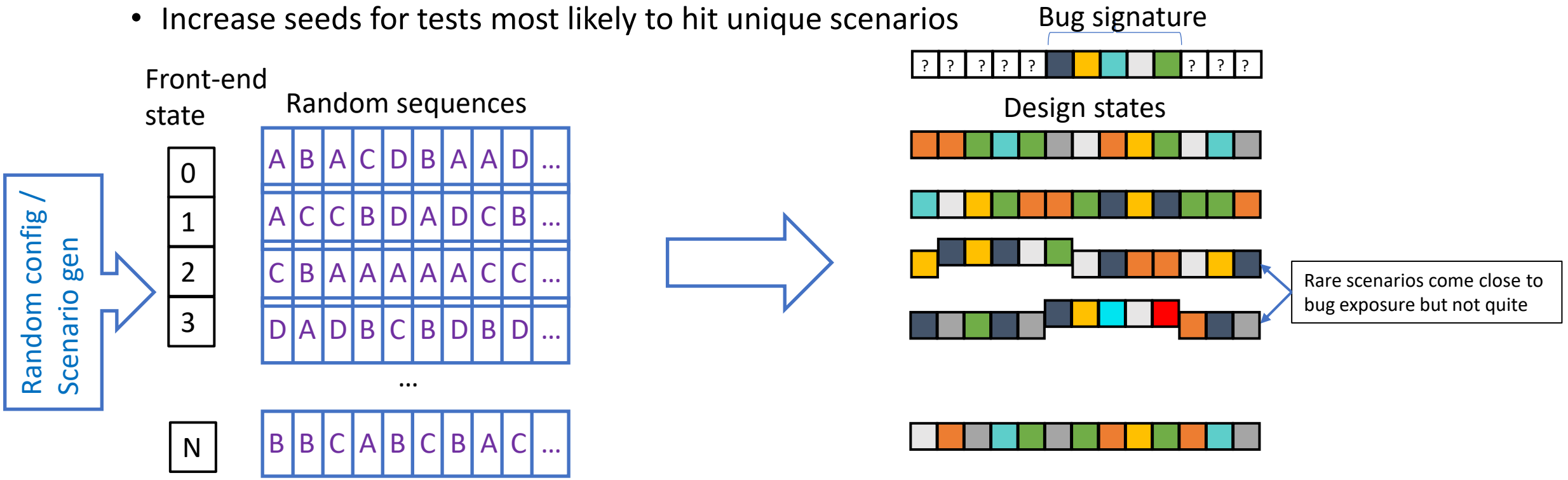






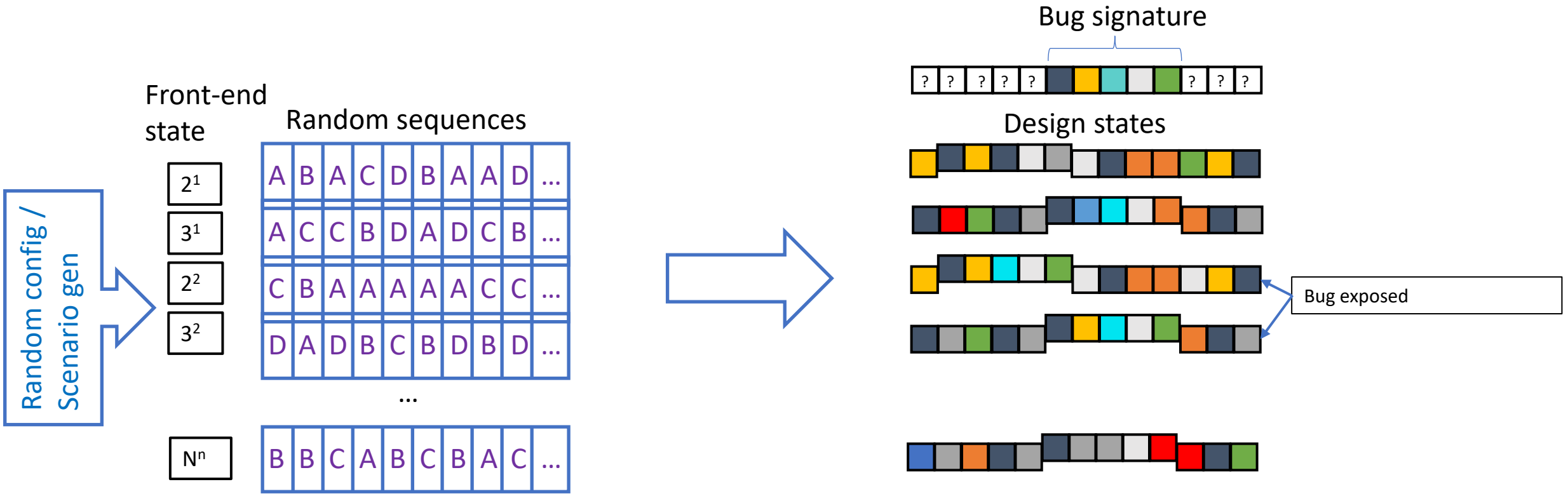
Machine Learning for Bug Hunting

- Typical bug-hunting using randomized testbenches
  - Once bug rate reaches some low threshold
    - Fill CPU resources with random runs
    - Increase seeds for tests most likely to hit unique scenarios



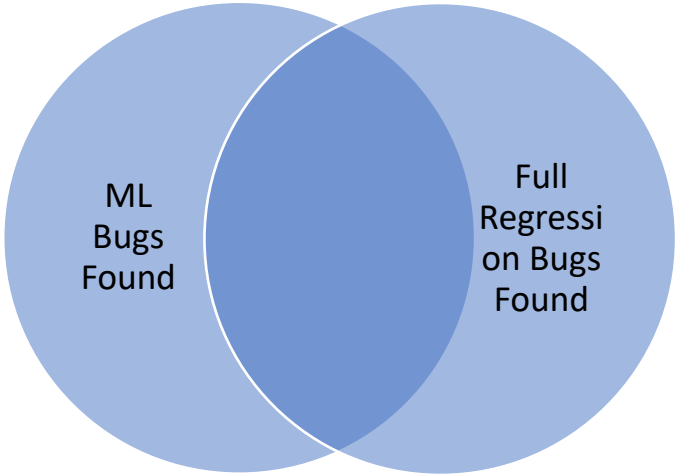
Machine Learning for Bug Hunting (con't)

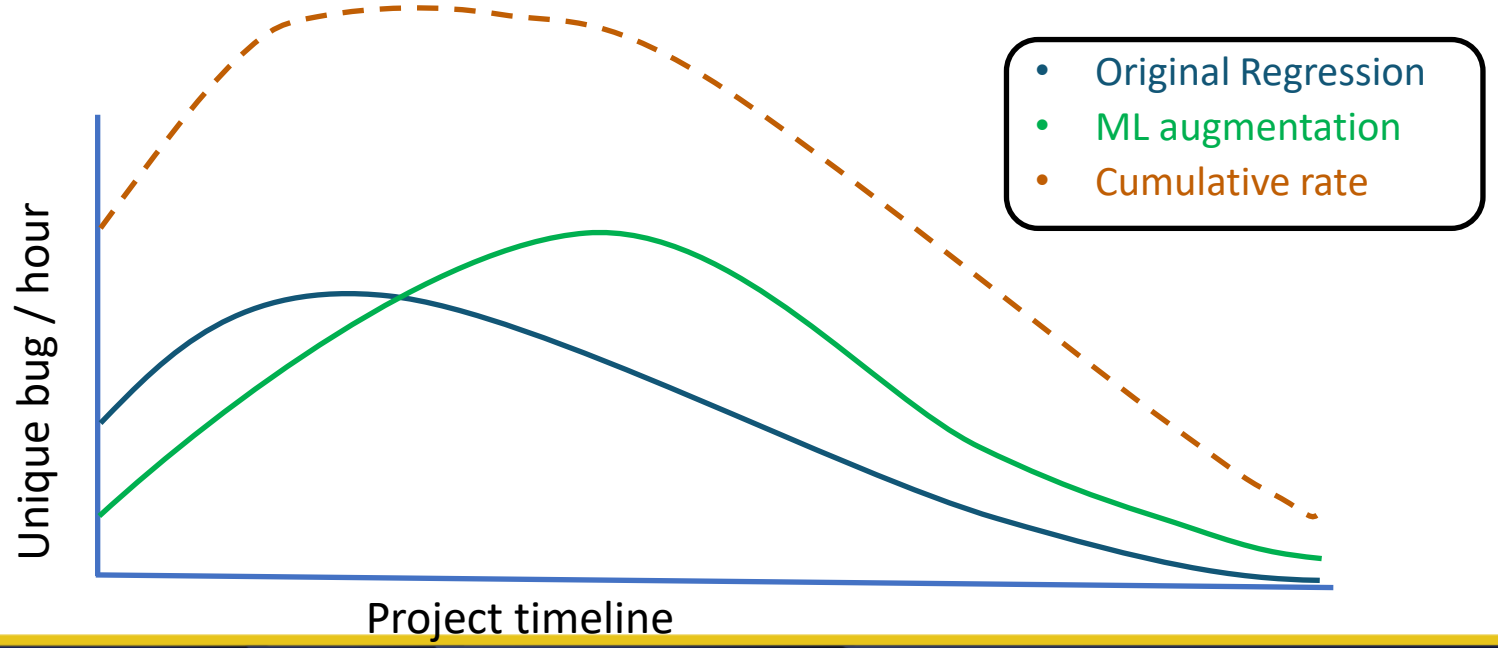
- Machine Learning bug hunting using randomized testbenches
  - Focus on front-end states that magnify more rare conditions



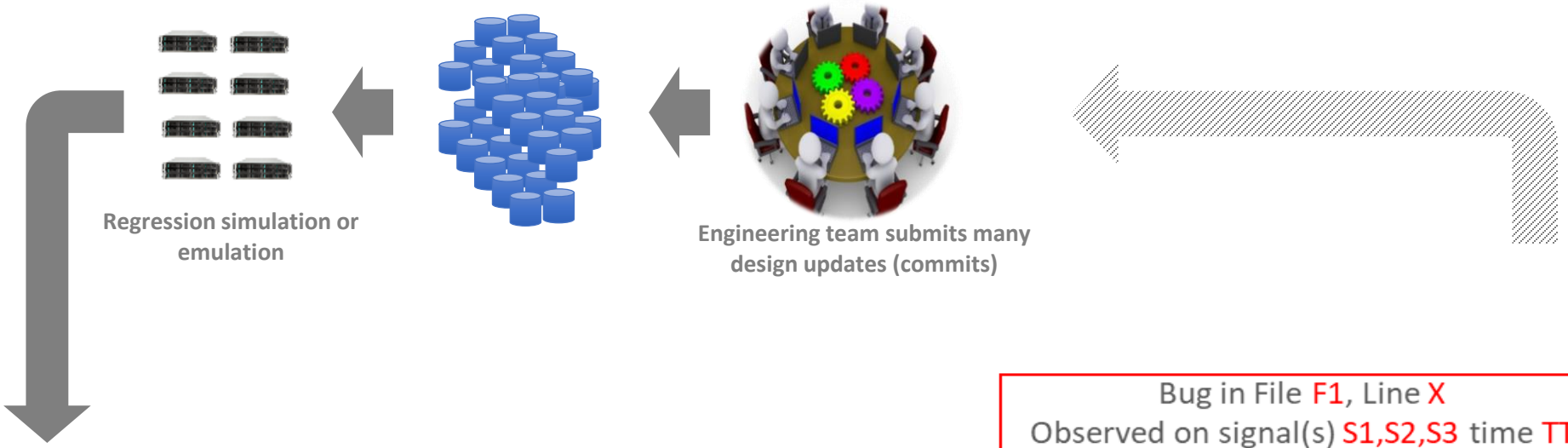
Machine Learning for Bug Hunting (con't)

- Augment full regression with ML-generated runs
  - The ML-generated regression will create higher percentage of more rare scenarios
  - The bug rate of the ML runs (unique signature / cpuH) will typically be higher than the full regression
  - Use in conjunction with the full regression until the full regression no longer finds new bug signatures

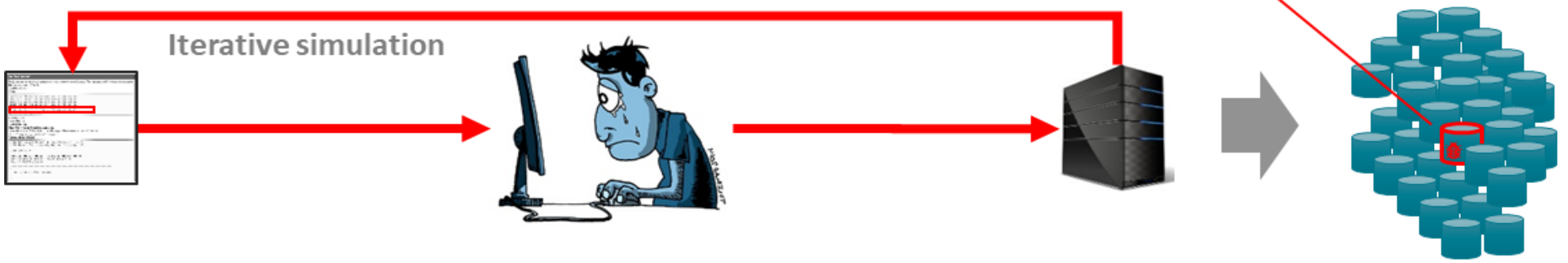




AI Opportunity for Regression Debug



Bug in File F1, Line X
Observed on signal(s) S1,S2,S3 time TT

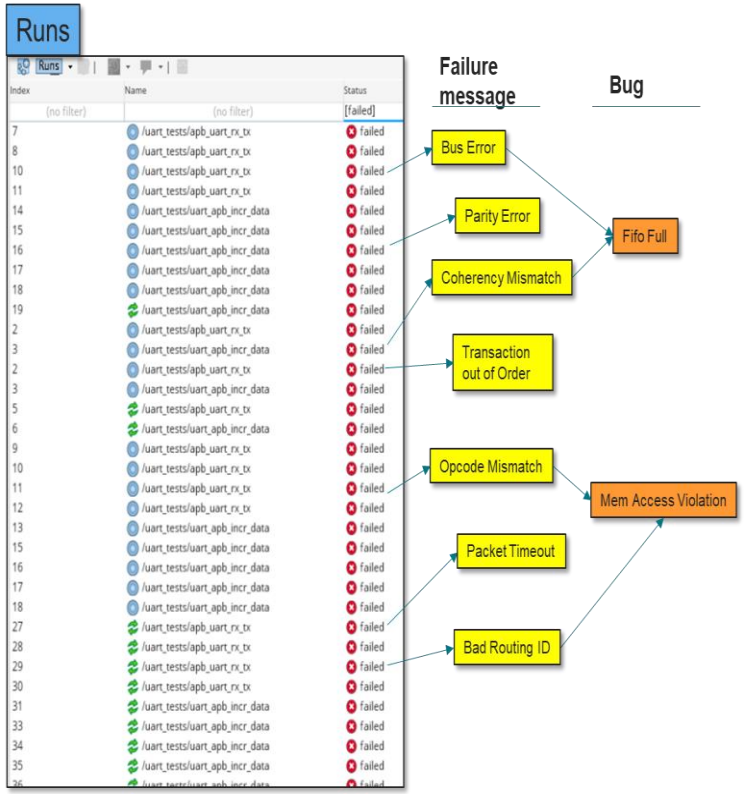


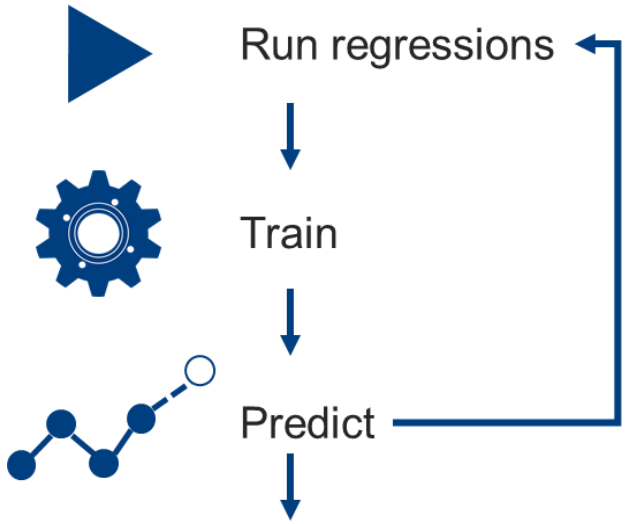
Debugging test failures in regression results

Failure Root cause found

Automated ML Bucketing of Regression Failures

- Problem Statement
  - Manual failure analysis of regression is very costly and inefficient
- Solution
  - Automate the failure analysis/classification





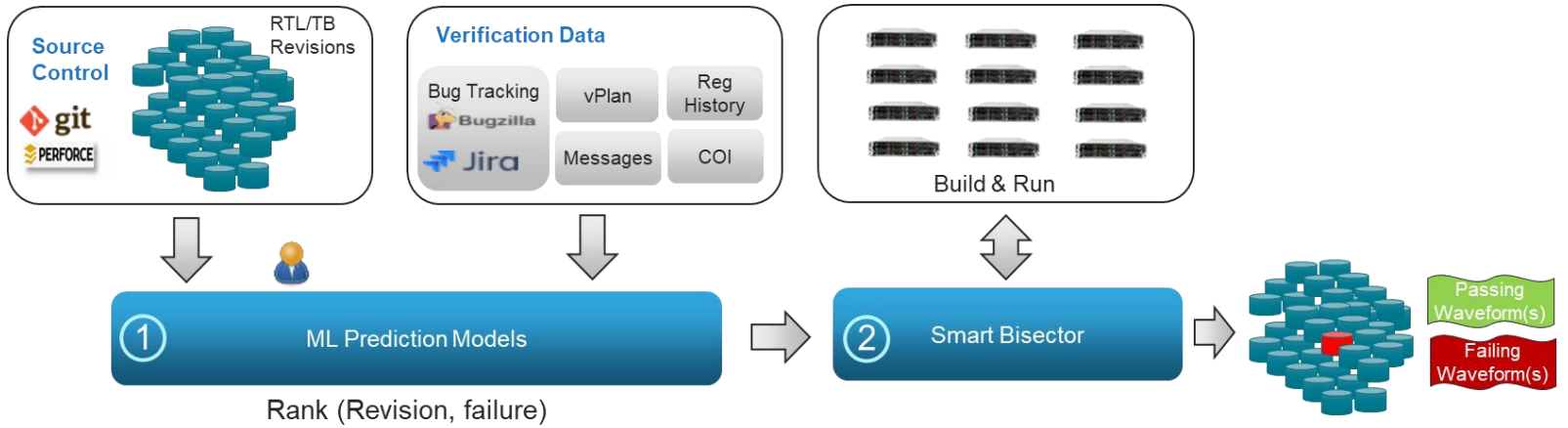
Bug: FIFO Full

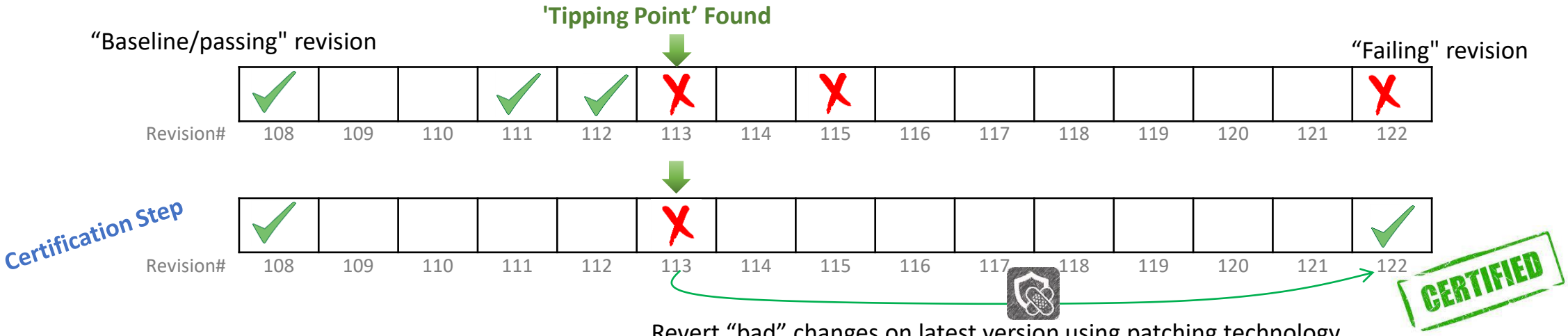
```
Test3: Bus error
Test27: Parity Error
Test51: Mismatch
```

Bug: Mem Access Violation

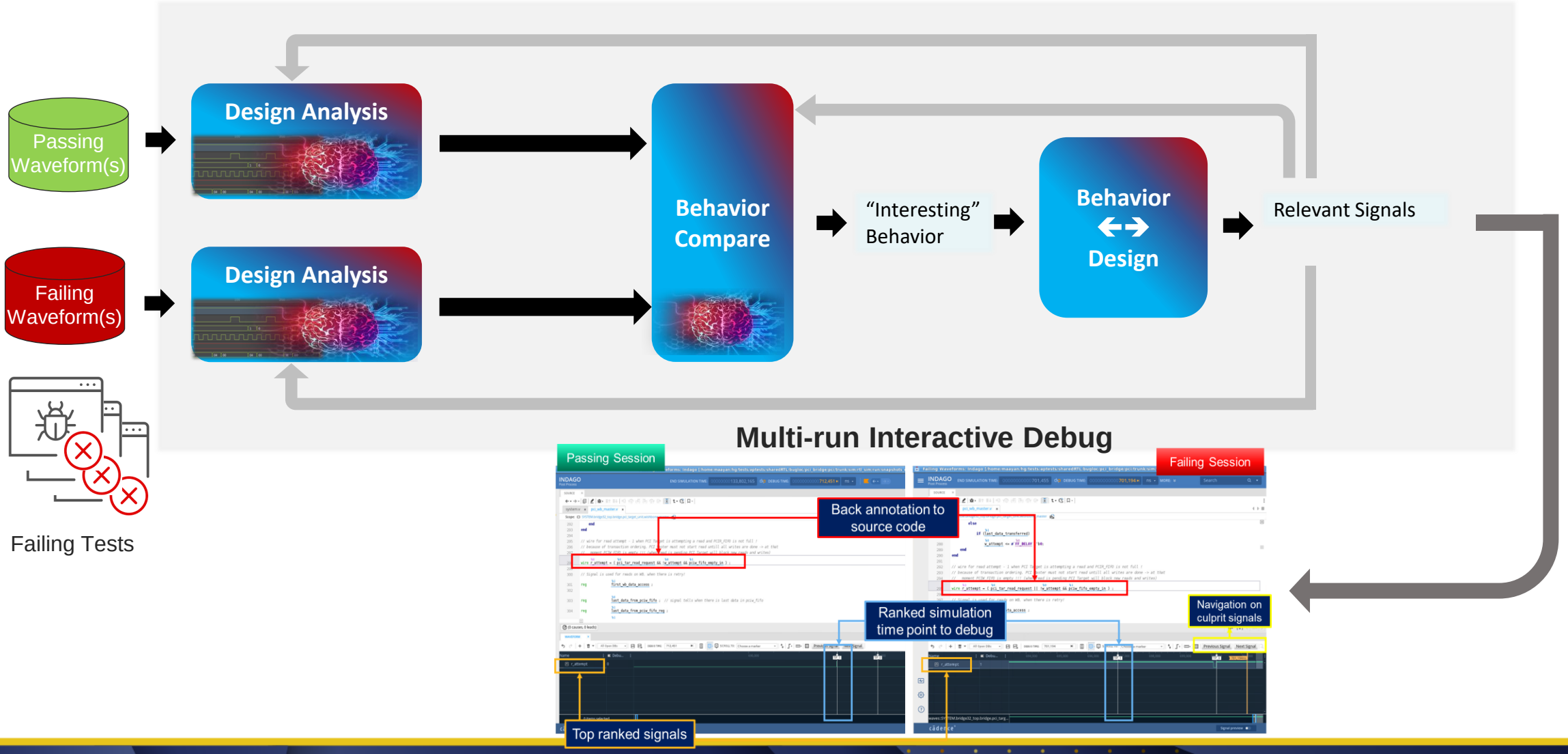
```
Test16: Wrong Opcode
Test27: Packet Timeout
Test51: Bad Routing ID
```

Automatically Identify the Bad Change Set





Automated Deep Waveform Analysis



AI Design Analysis

Identify and rank semantic changes between two RTL versions

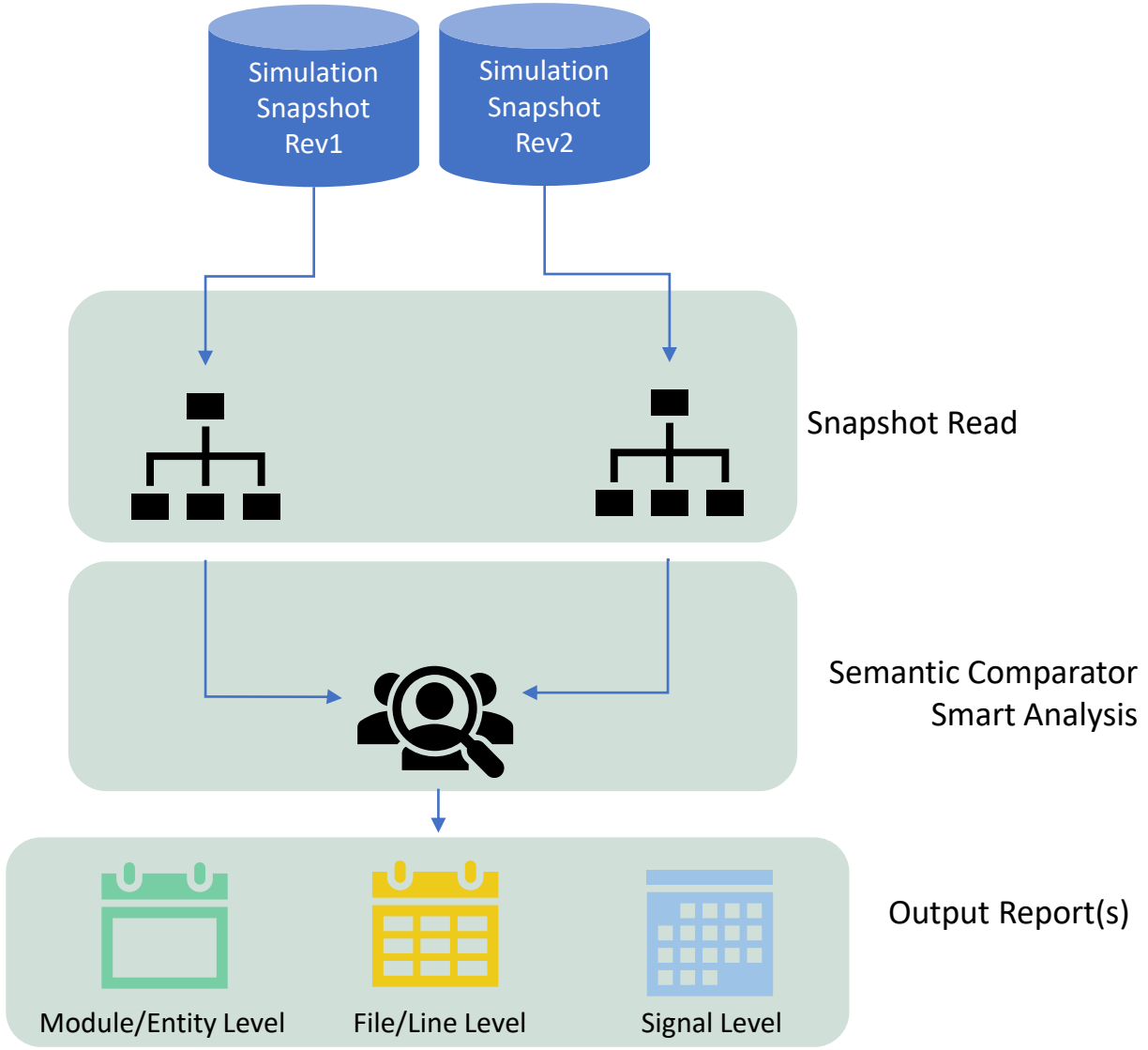
Ignore harmless changes

Rank “complexity” of genuine logic changes

```
module cg (d, clk);
 input d, clk;
 reg orig;
 reg clone;
 reg g_latch;
 wire w = orig ^ d;
 wire gclk = clk & g_latch;

 always @(clk or w)
   if (~clk) g_latch <= w;

 always @(posedge gclk)  clone <= d;

 always @(posedge clone) orig <= d;

 fd : assert property (
      @(posedge clk) orig == clone
 );
Endmodule
```

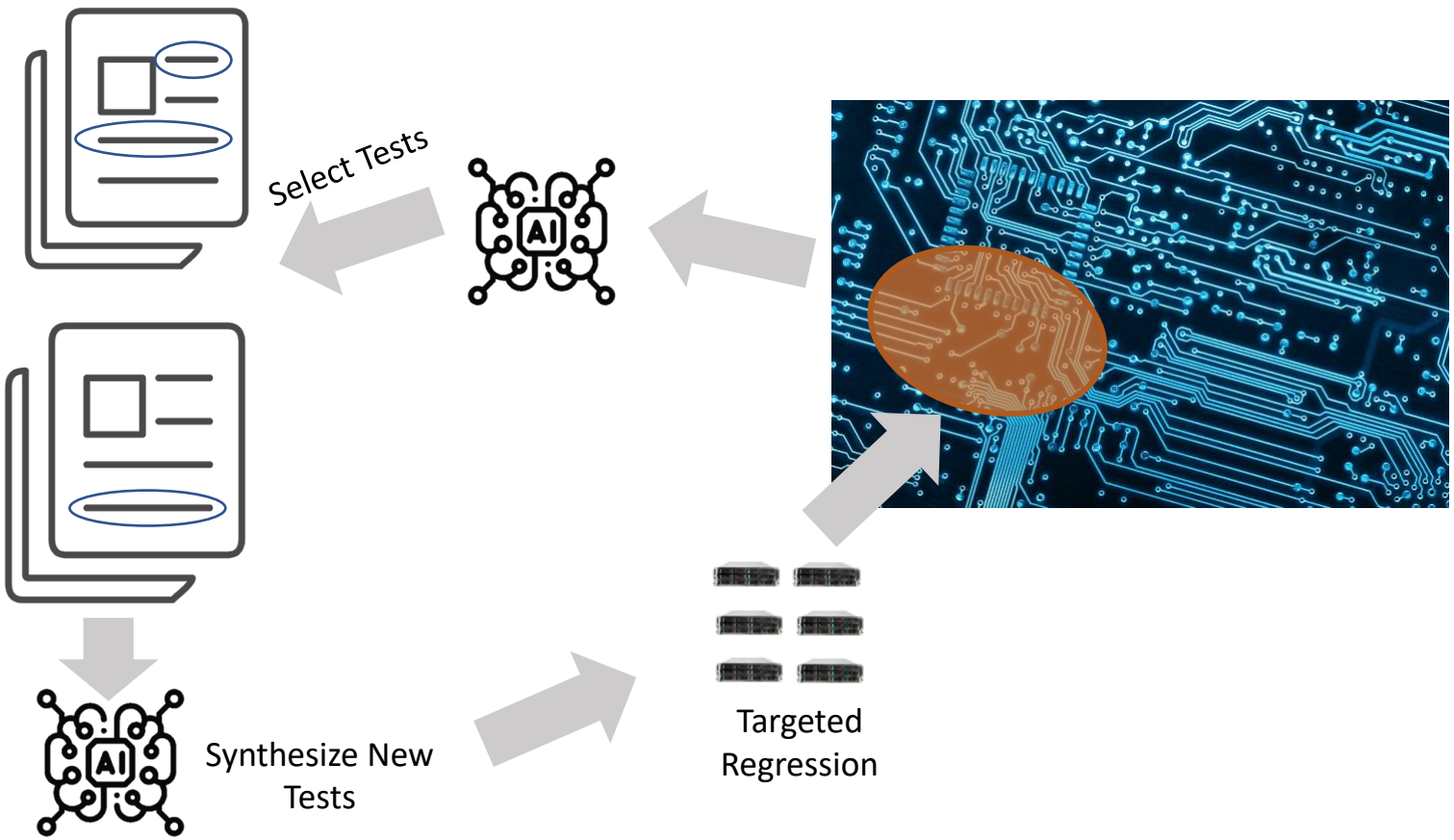
?

```
module cg (d, clk);
 input d, clk;
 reg orig, clone, g_latch;

 // Comments …
 wire w = orig ^ d;
 wire gclk = clk & g_latch;

 always @(clk or w)
   if (clk) g_latch <= w;

 always @(posedge gclk)
     clone <= d;

 always @(posedge clone)
     orig <= d;

 fd : assert property (
      @(posedge clk) orig == clone
 );
endmodule
```

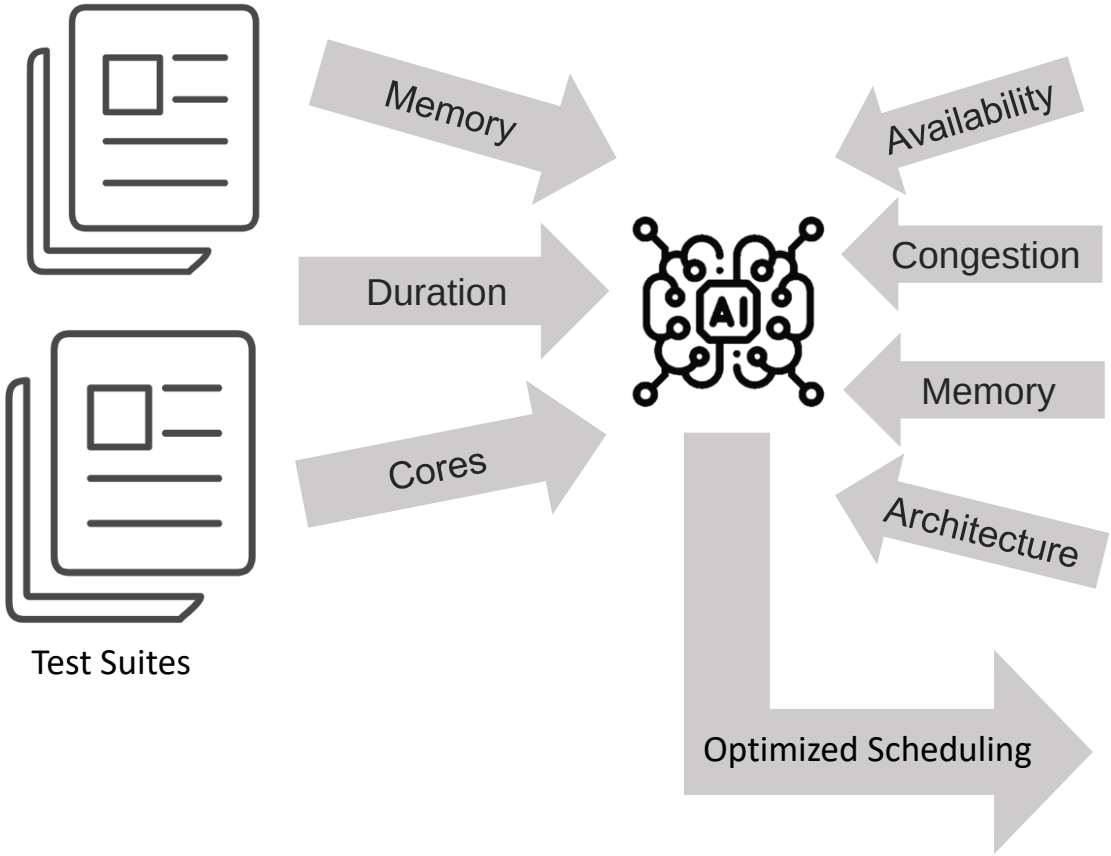


AI Opportunity for Workload Optimization

- Automatically identify target features
  - Disruptive changes
  - Low coverage
  - High bug potential
- Select or synthesize stress tests
  - Optimize regression time and resource.



AI Opportunity for Resource Optimization



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Real World Impact of AI Driven Verification Solutions

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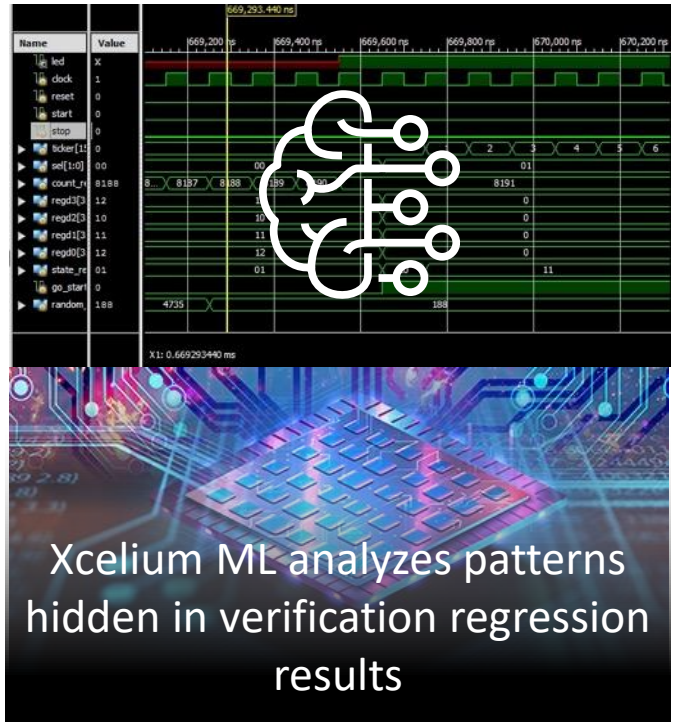
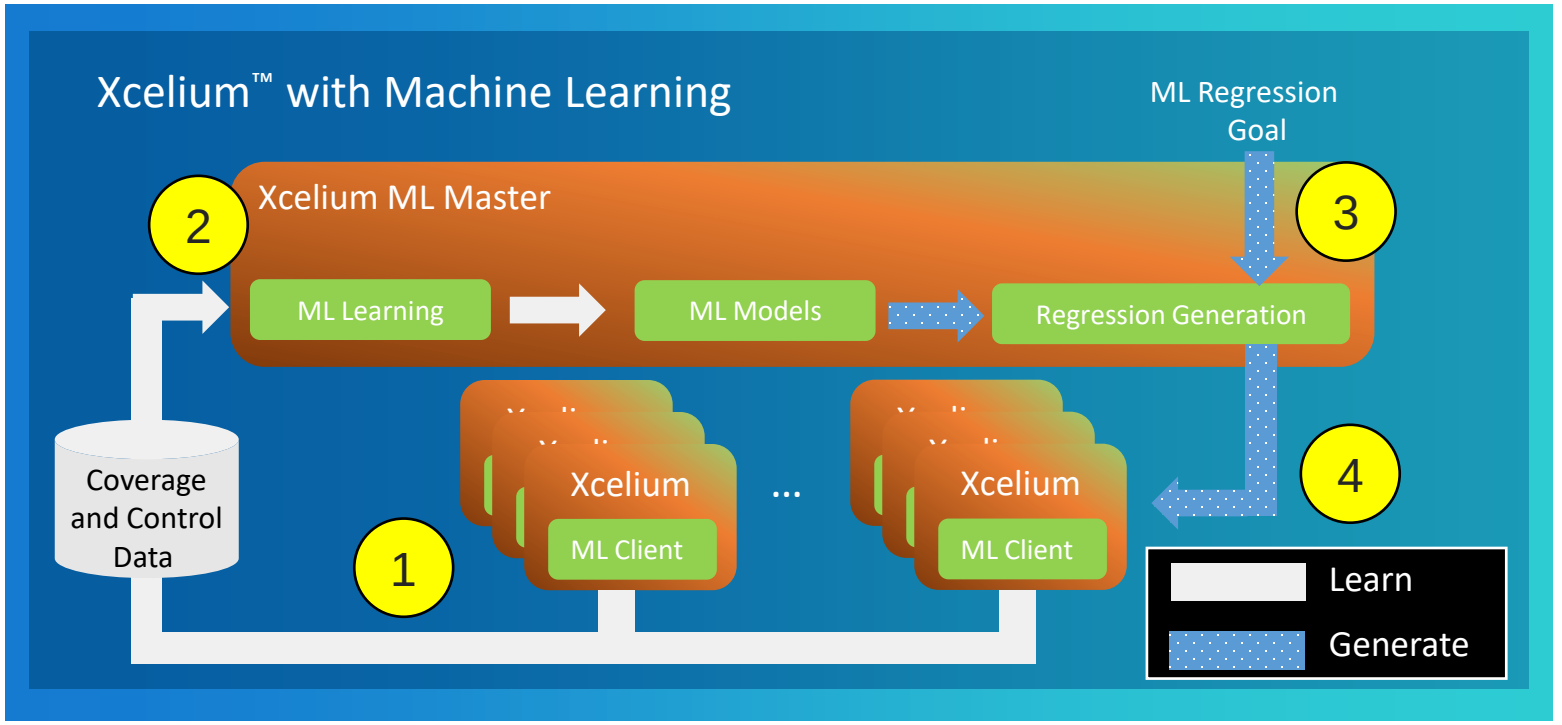
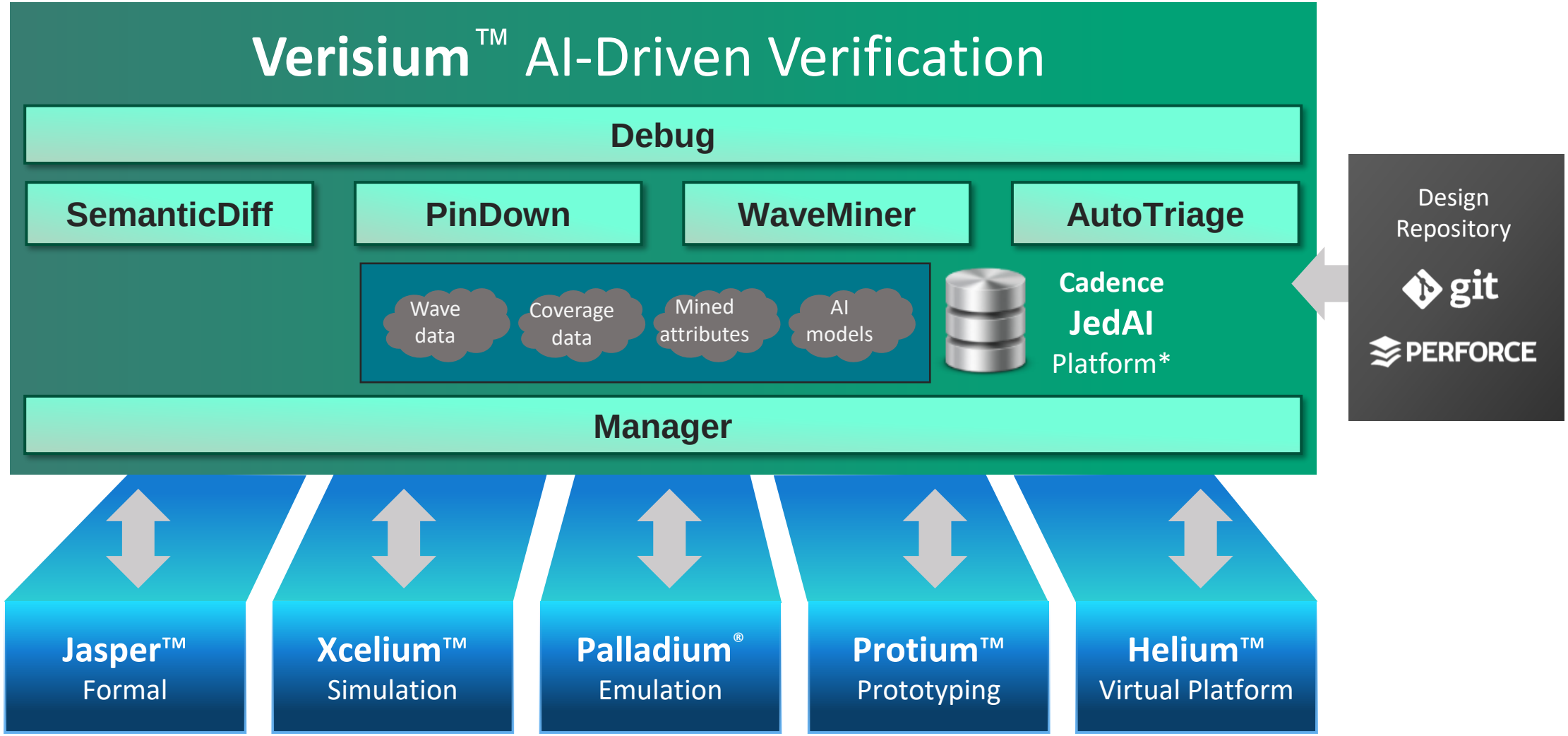
Xcelium-ML

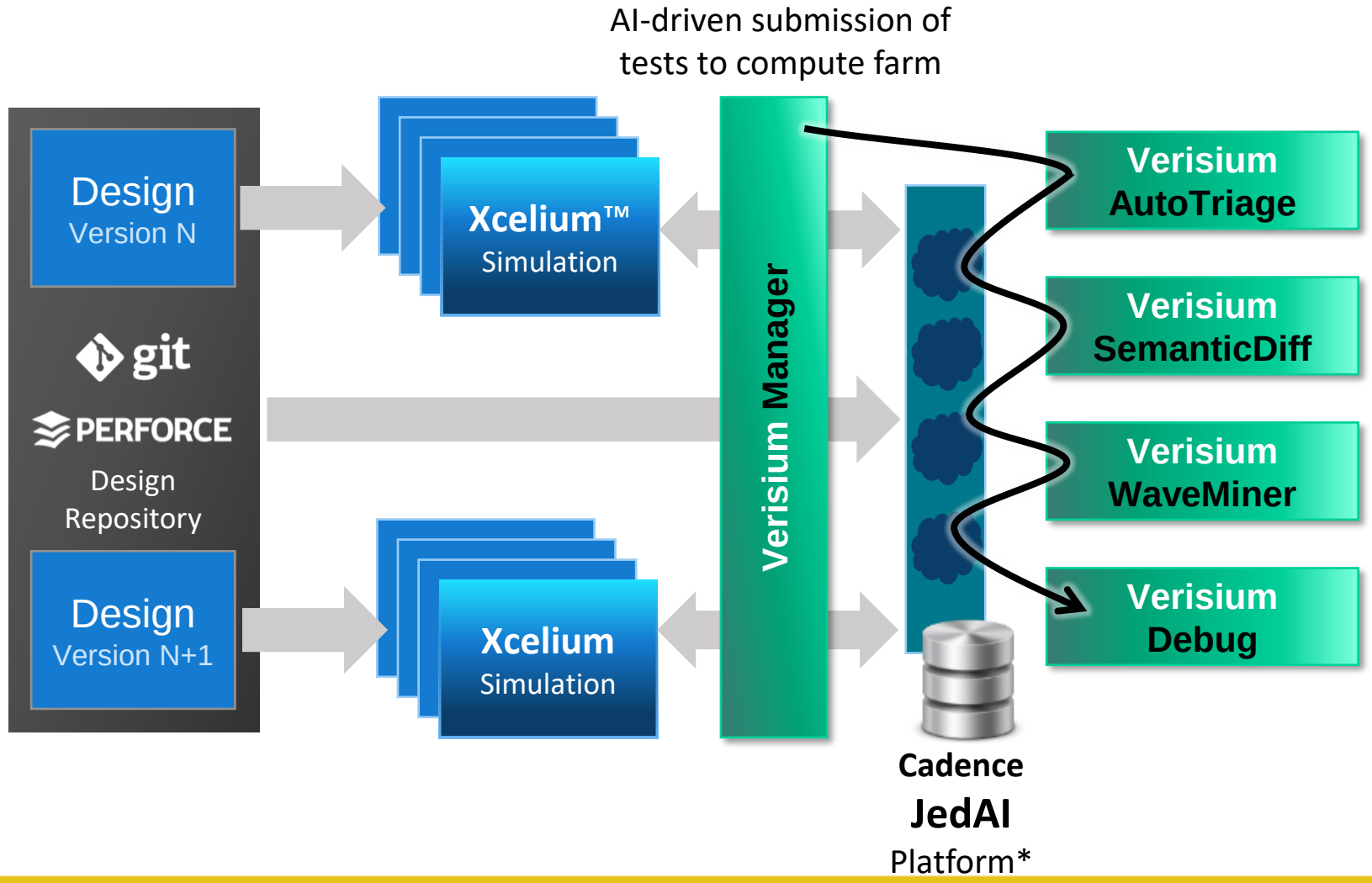

Xcelium ML analyzes patterns hidden in verification regression results


Xcelium™ with Machine Learning
ML Regression Goal
Xcelium ML Master
2
3
ML Learning
ML Models
Regression Generation
Coverage and Control Data
Xcelium
ML Client
...
Xcelium
ML Client
1
4
Learn
Generate

Verisium Platform



Verisium Platform in Action



Verisium AutoTriage — Automatically groups tests failing due to the same underlying bug

Verisium SemanticDiff — Automatically identifies code differences between design versions N and N+1

Verisium WaveMiner — Analyzes waveforms and automatically identifies root cause of bug (signals + time)

Verisium Debug — Interactive side-by-side display of passing vs failing tests with bugroot cause highlighted

* Cadence Joint Enterprise Data and AI (JedAI) Platform

Cadence Joint Enterprise Data and AI (JedAI) Platform

AI-driven Verification | AI-driven Implementation | ... | AI-driven System Analysis

Open APIs

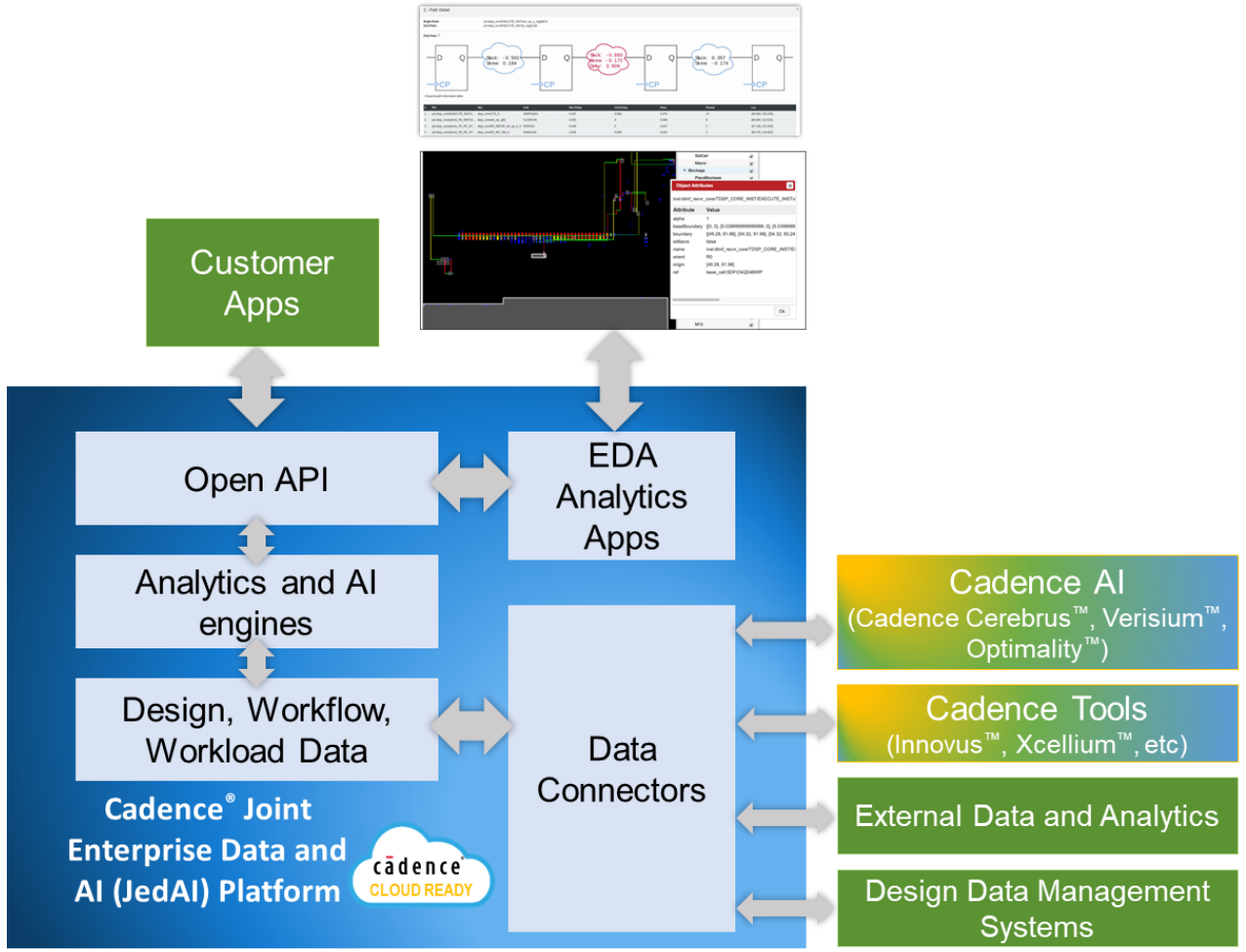
AI and Analytics engines

Design, Workflow, and Workload Data

Wave data | Coverage data | Mined attributes | AI models | ... | Layouts | Reports & logs | Design & constraints

Scalable Cloud-Ready Object Store

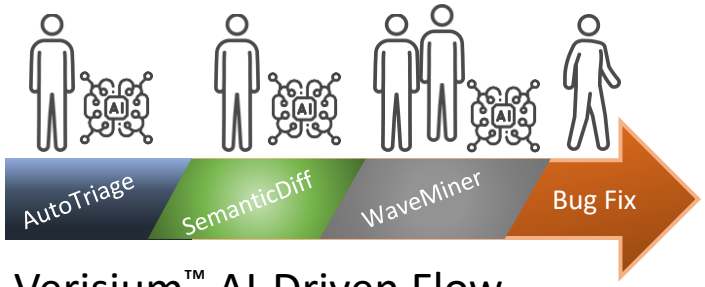
Cadence© JedAI Platform



- Cross-domain big data EDA platform to facilitate AI and analytics deployment delivering productivity multiplier
- Highly scalable, distributed, secure infrastructure
- Open industry-standard user interface and scripting environment optimized for Cadence tools

SoC Debug with Verisium Platform

Manual Flow



Verisium™ AI-Driven Flow

Potential for massive improvement in debug productivity

Questions

- Thanks for joining!
- Feedback and offline questions:
  - magraham@cadence.com