Democratizing Digital-centric Mixed-signal Verification methodologies

Sumit Vishwakarma
Principal Product Manager
Mixed-Signal BU, Siemens EDA

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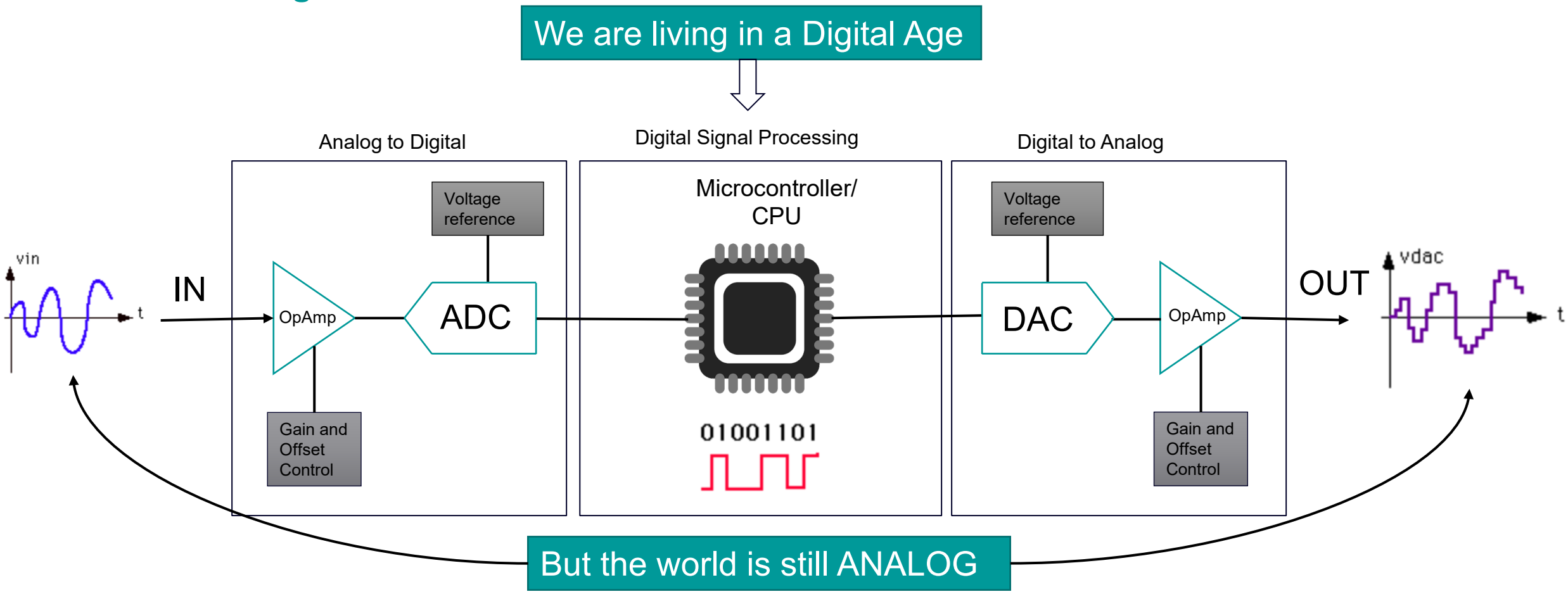
Agenda

- The changing landscape of Mixed-Signal Design
- Siemens EDA Symphony Mixed-Signal Platform
- Mixed-Signal Verification is Evolving
- Introducing Symphony Pro
- Demo

What is Mixed Signal?



Analog is time-varying continuous signals such as: Sound, Light, Pressure, Temperature

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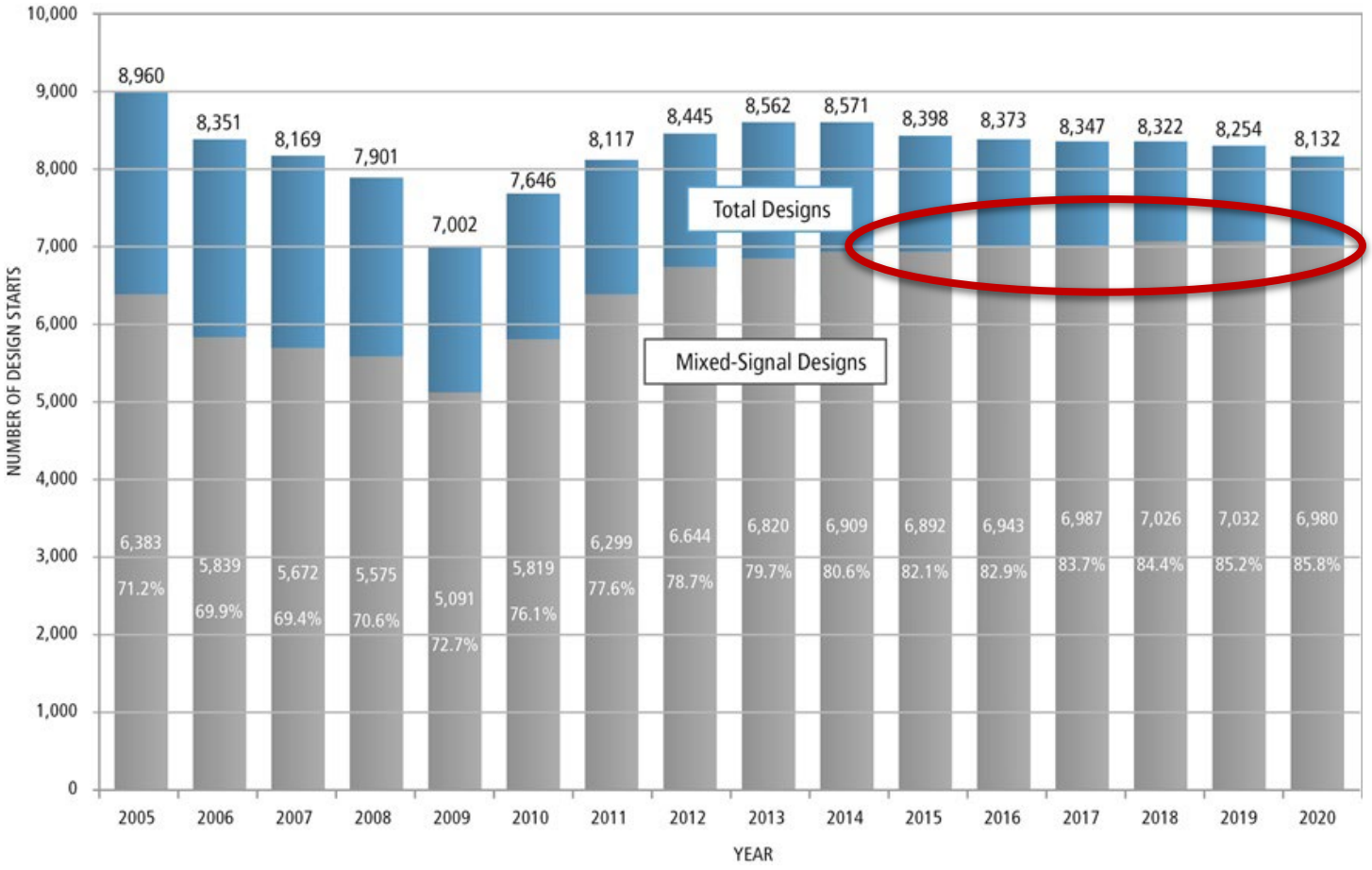
Mixed-Signal is Dominant



85% of design starts are mixed signal

IBS: Mixed-signal design starts as percent of total

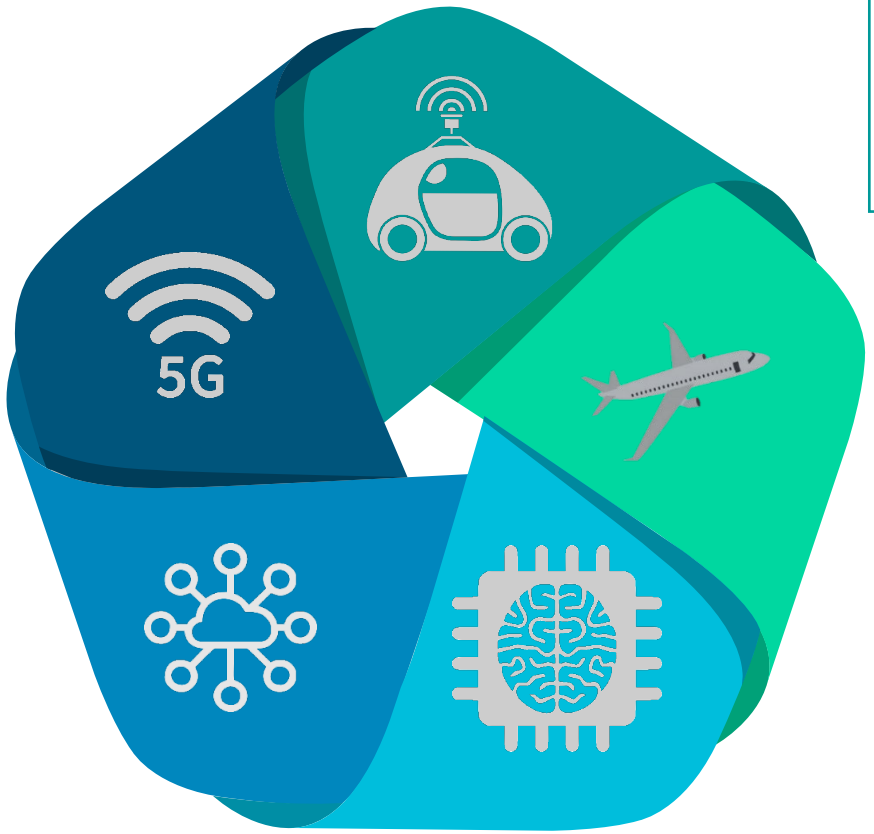
The changing landscape of mixed-signal designs

5G

Massive MIMO needs **Digital** Front End (DFE) and RF-sampling data converters

Automotive + Mil Aero

In-vehicle communication is enabled by multi-modal analog sensor fusion with **digital** MCU for processing and decision making



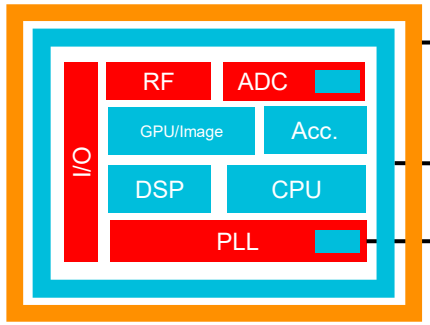
IoT

Complex clocking at ultra-low power for battery powered devices needs **digital** calibration

HPC/AL

Data centers transitioning from 100G NRZ to PAM4 for high-speed serial communication rely on **Digital Signal Processing** (DSP) for equalization and improving signal integrity

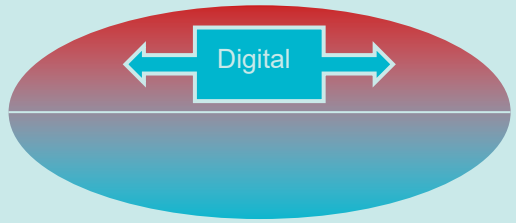
The changing landscape of mixed-signal designs



‘Digital’ Power Intent methodology
- Universal Power Format (UPF)

‘Digital’ Coverage Driven TB methodology
- Automation, Regression, Debug

‘Digitally Assisted’ Analog Design
- Digital calibration & Digital control



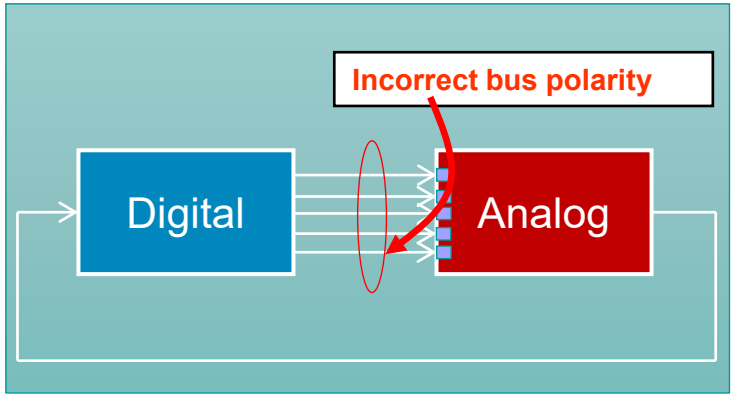
For Semi (source : kbv research)

*The Global Mixed Signal IC Market size is expected to reach **$141.5 billion** by 2026, rising at a market growth of 7.6% CAGR*

Objectives of Mixed-Signal Verification

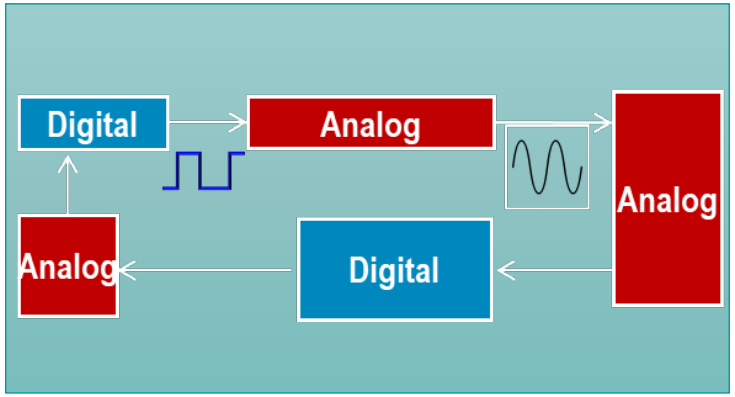
Detect Top Level Connectivity Specification Errors

- Incorrect bus wires, register bits, wrong polarity
- Missing level shifters
- Misunderstood interface specs



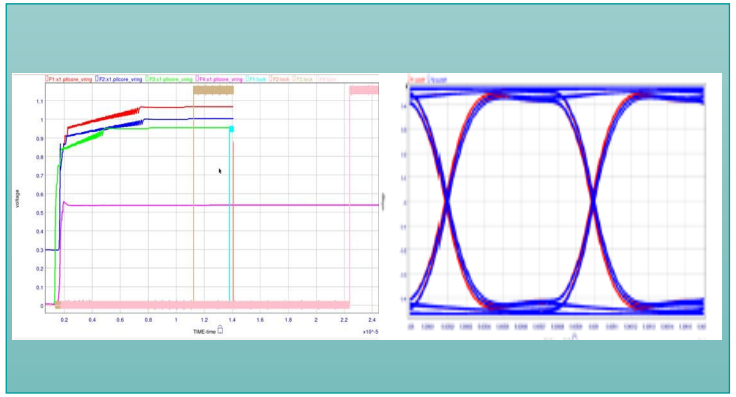
Detect Errors Caused by Electrical Behavior

- Bias mismatch
- IP behavior during startup
- Higher order analog blocks behavior impacting Digital



Performance Verification

- Noise performance
- Floating nodes and Leakage currents
- IP behavior under various process and design corners



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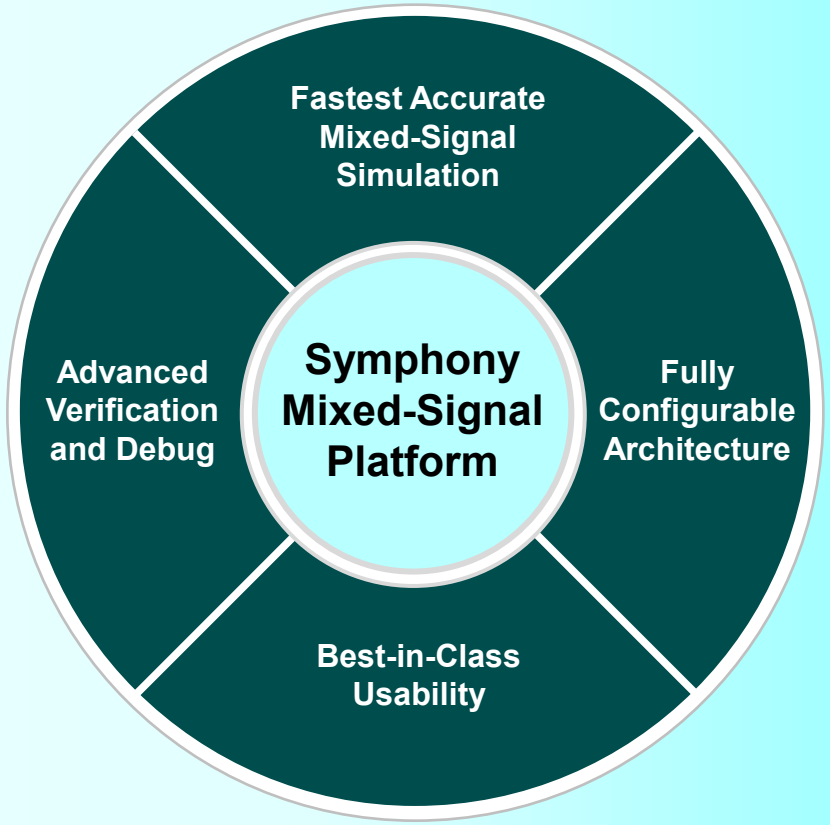
Technology Gaps and Customer Pain Points

Gaps in Legacy Mixed-signal Solution	Customer Pain Points
Lack of performance with golden SPICE accuracy	Silicon re-spins Delayed time-to-market
Not easy to set up and use	Takes longer to bring-up design Cannot scale verification teams quickly
Limited debug and coverage	Takes longer to troubleshoot design issues
Inability to re-use existing verification infrastructure	Cannot take advantage of newer verification methodologies

Industry's Fastest and Most Versatile Mixed-Signal Simulation Platform



~2-5x
Simulation Speedup

Spice
Accuracy

100+
Customers

80+
Production Tapeouts

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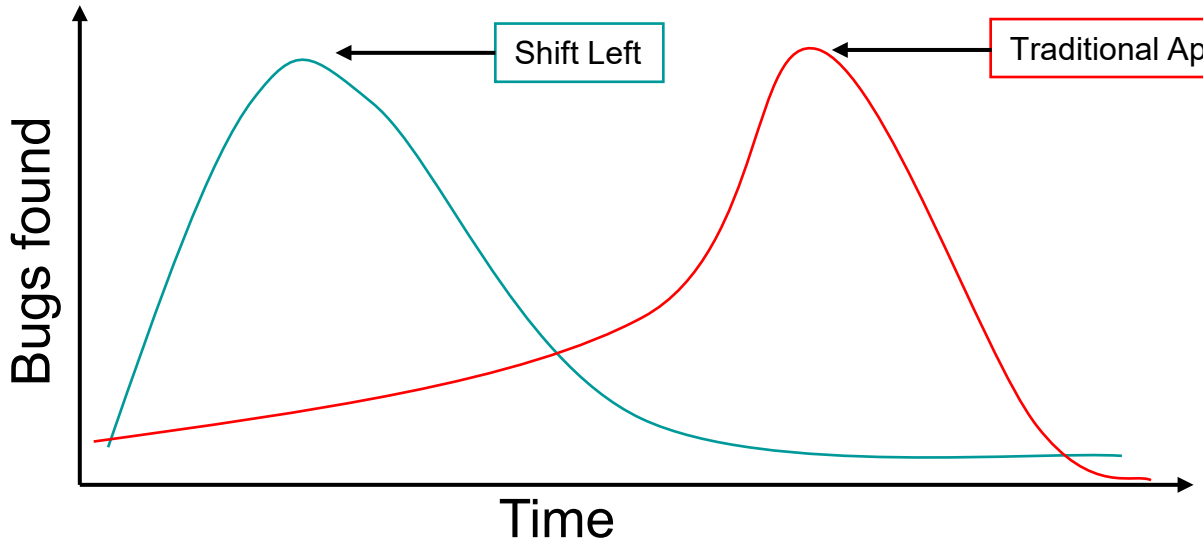
Shift Left: Verifying Early in Design Cycle

Block Design → Block Verification → System Integration → System Verification → Tape-out

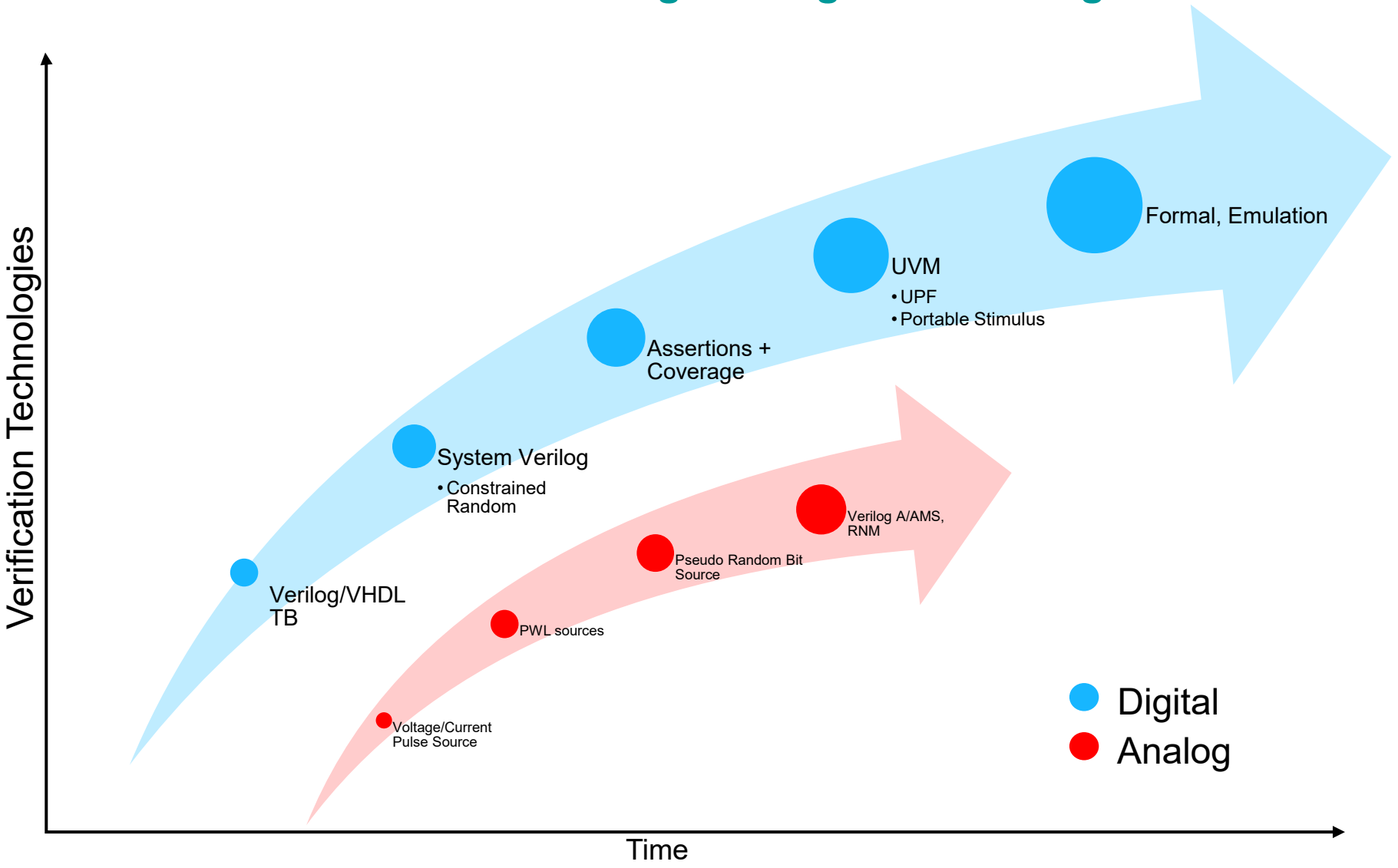
Testing



Shift Left =

- Better Quality
- Better Efficiency
- Lower Cost

Evolution of Verification Technologies : Digital vs Analog



- ✓ Reusability
- ✓ Scalability
- ✓ Interoperability
- ✓ Modularity

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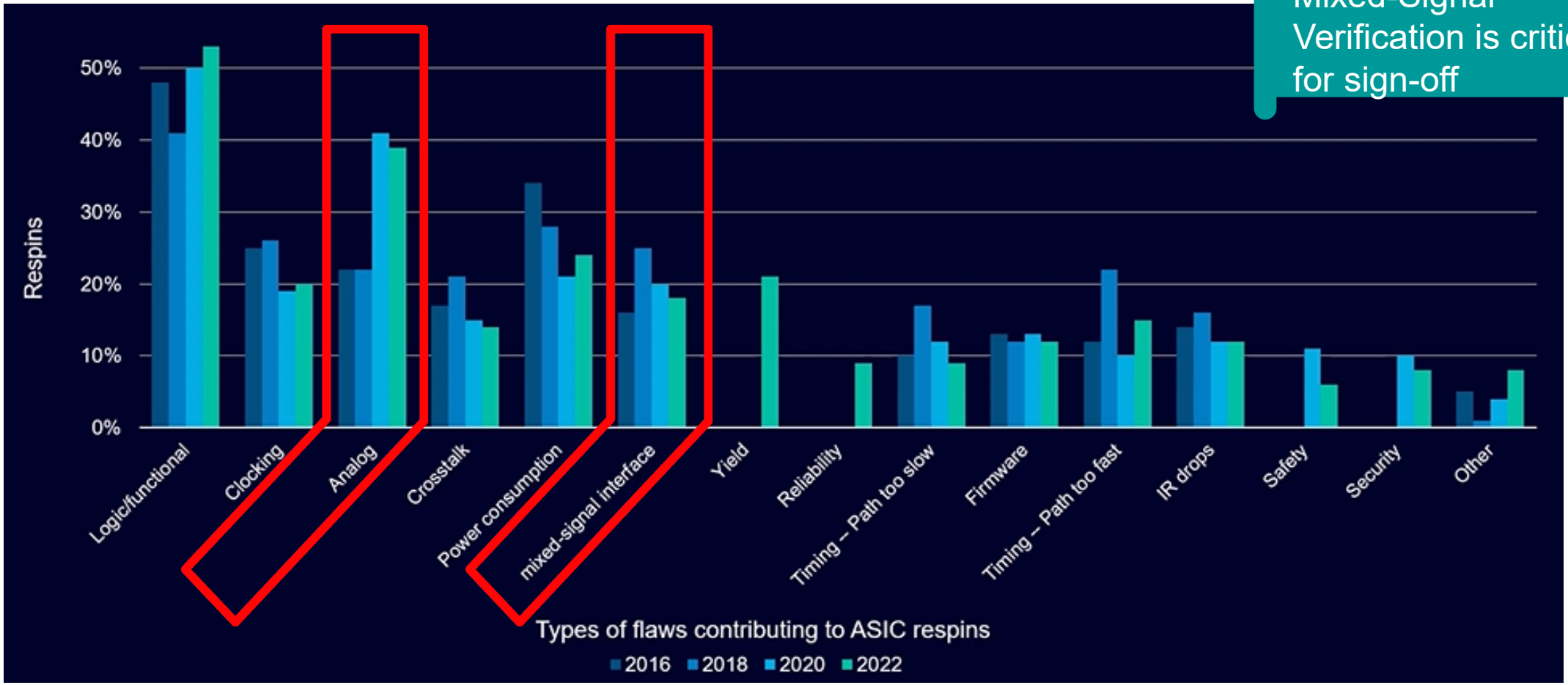
ASIC Type of Flaws Contributing to Respin

Mixed-Signal Verification is critical for sign-off



Source: Wilson Research Group and Siemens EDA, 2022 Functional Verification Study

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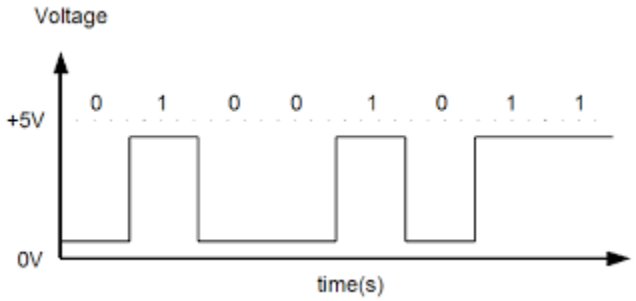
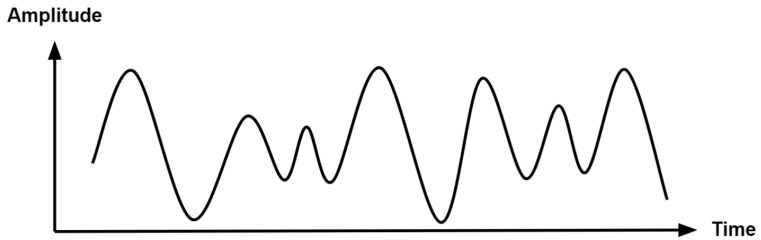
Question:

Can digital verification methodologies be extended for analog and mixed-signal designs?

What is the difference?

Digital Simulation	Analog Simulation
Digital devices and circuits operate in a discrete domain	Analog devices and circuits operate in a continuous domain
Circuit nodes have a binary state of either HIGH (1), LOW (0), X (unknown), or Z	Node voltages and branch currents can take arbitrary (positive or negative) values
The algorithm solves logical expressions sequentially by triggering events	Applying Kirchhoff's laws, the algorithm solves the entire analog system matrix at every time step
There is a defined signal flow from input to output.	Circuit elements can instantaneously influence any other element in the matrix
Very Fast (finishes in mins)	Slow & Compute intensive (hrs to days)





Can we take advantages of Digital Speed with Analog Accuracy?

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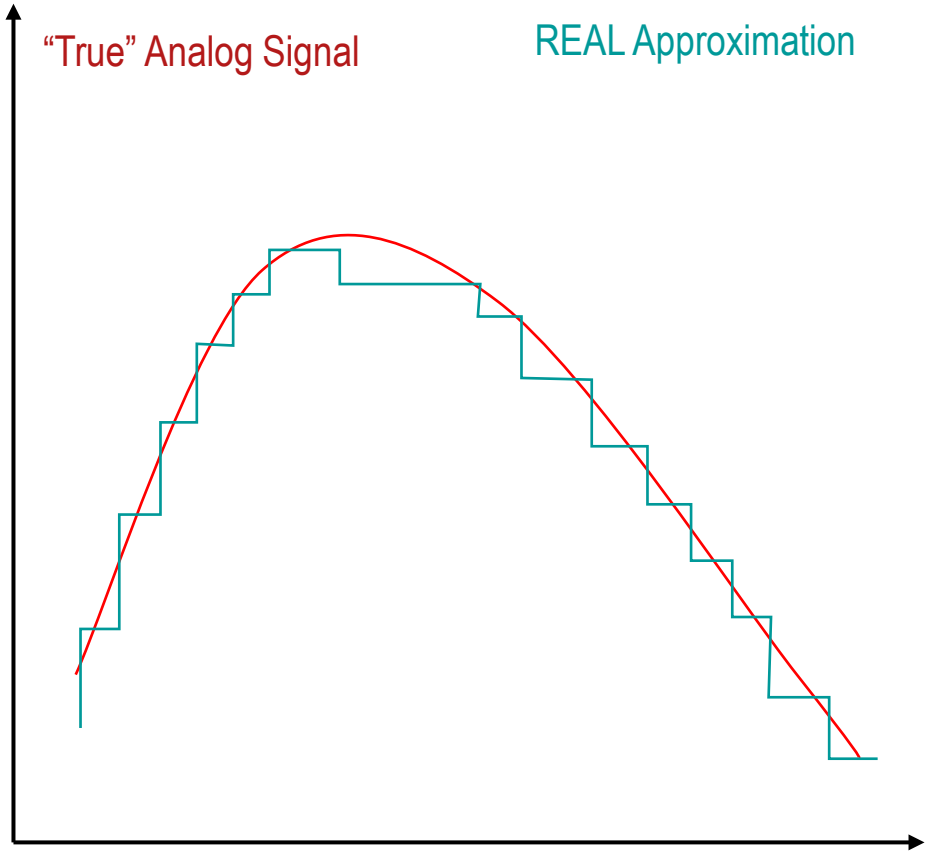
Real Number Modeling Overview

- Modeling analog circuit's behavior as digital circuit
- Allows staying in a 100% Digital flow
- Very fast simulation
  - Event Driven
- Limitations
  - Mostly Transfer Function modeling
  - Frequency-domain modeling is complex
  - Less accurate - assumes A/D/A interactions are perfect

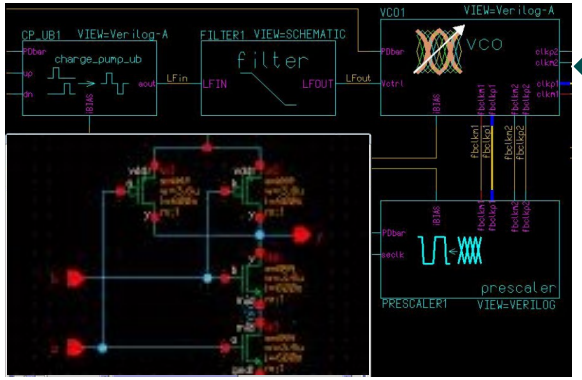


Real Number Modeling (RNM) in Mixed-Signal SoC Verification

Analog Block Design/Verif

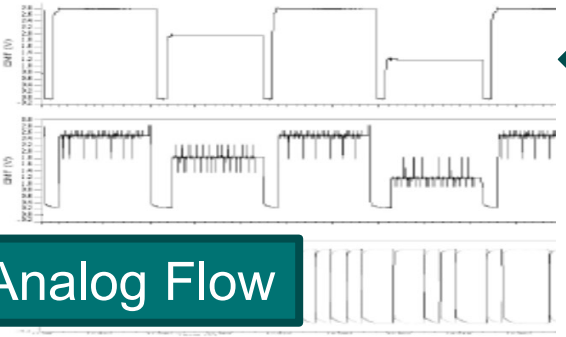
Real Number Models

Digital SoC/Subsystem Verification



Collaborate

Validate



Analog Flow

DDR PHY

LVDS

SER/DES

RADIO/RF

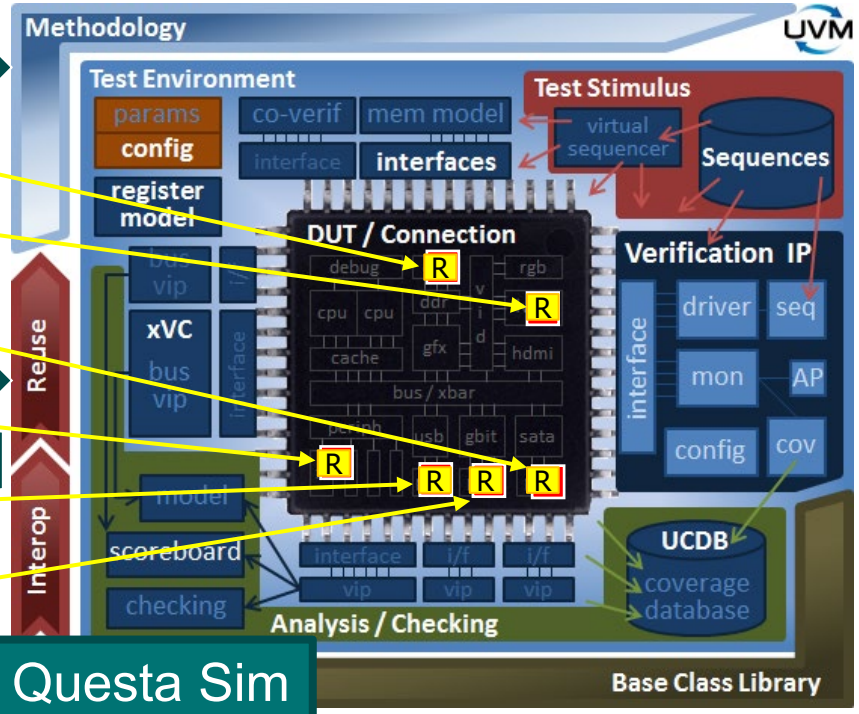
DPLL

RFID/NFC

Collaborate

Integrate

Validate



Questa Sim

A SPICE - VERILOG-AMS/VHDL-AMS WREAL - SV-DC/UDN SV-DESIGN/VHDL - SVA - SV-TB - UVM D

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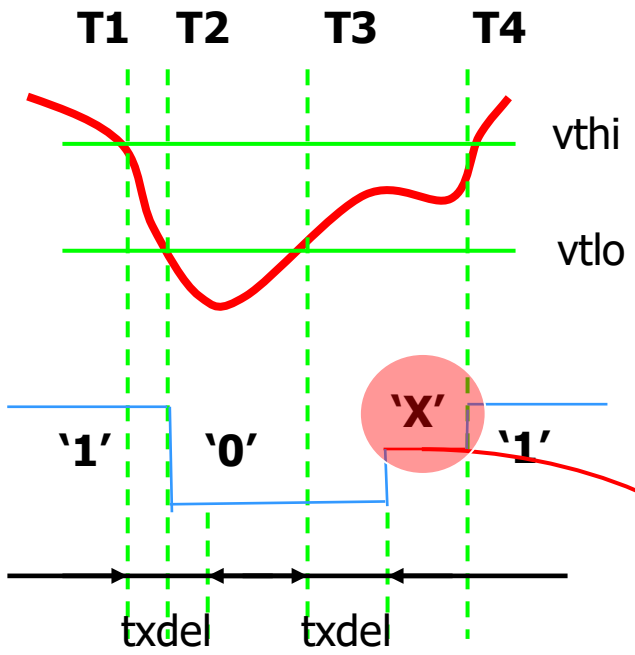
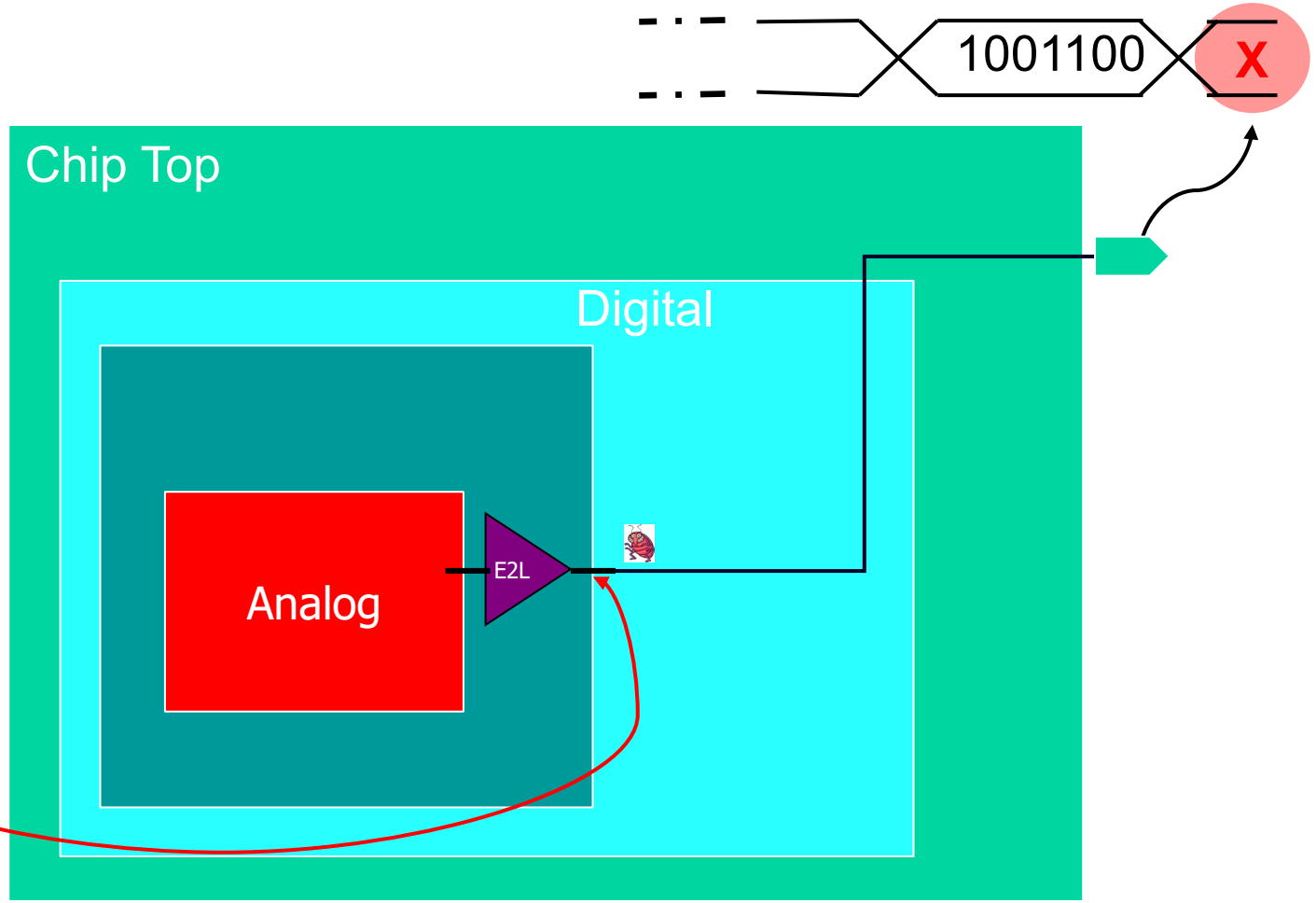
Mixed-Signal Bug





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Need for comprehensive mixed-signal debug?

Digital Debug	Analog Debug
High-capacity comprehensive debug environment	Primarily relies on waveform & schematic/netlist inspection (Manual)
Automation helps difficult and tedious debug (e.g. behavior tracing)	No automation ! Cumbersome debug (driven by designers' knowledge)

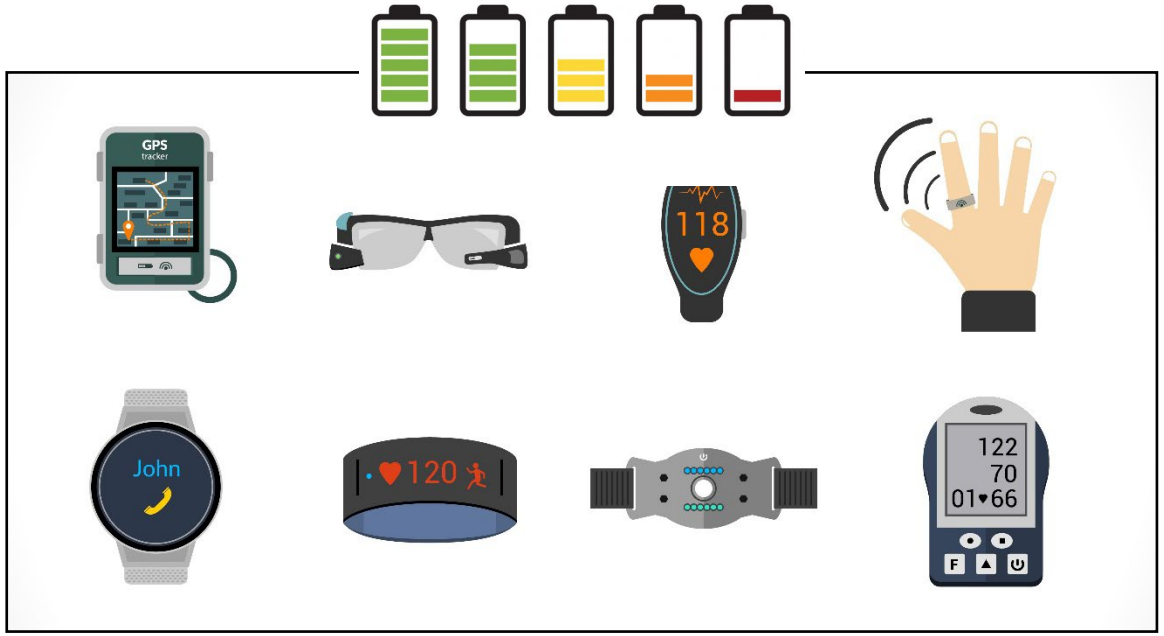
In AMS Design

- We have both analog and digital debug needs
- Complex A/D handshaking => 90% bugs happen at A/D boundary

Need for a Debug solution that caters to both analog and digital engineers

Power Aware Verification

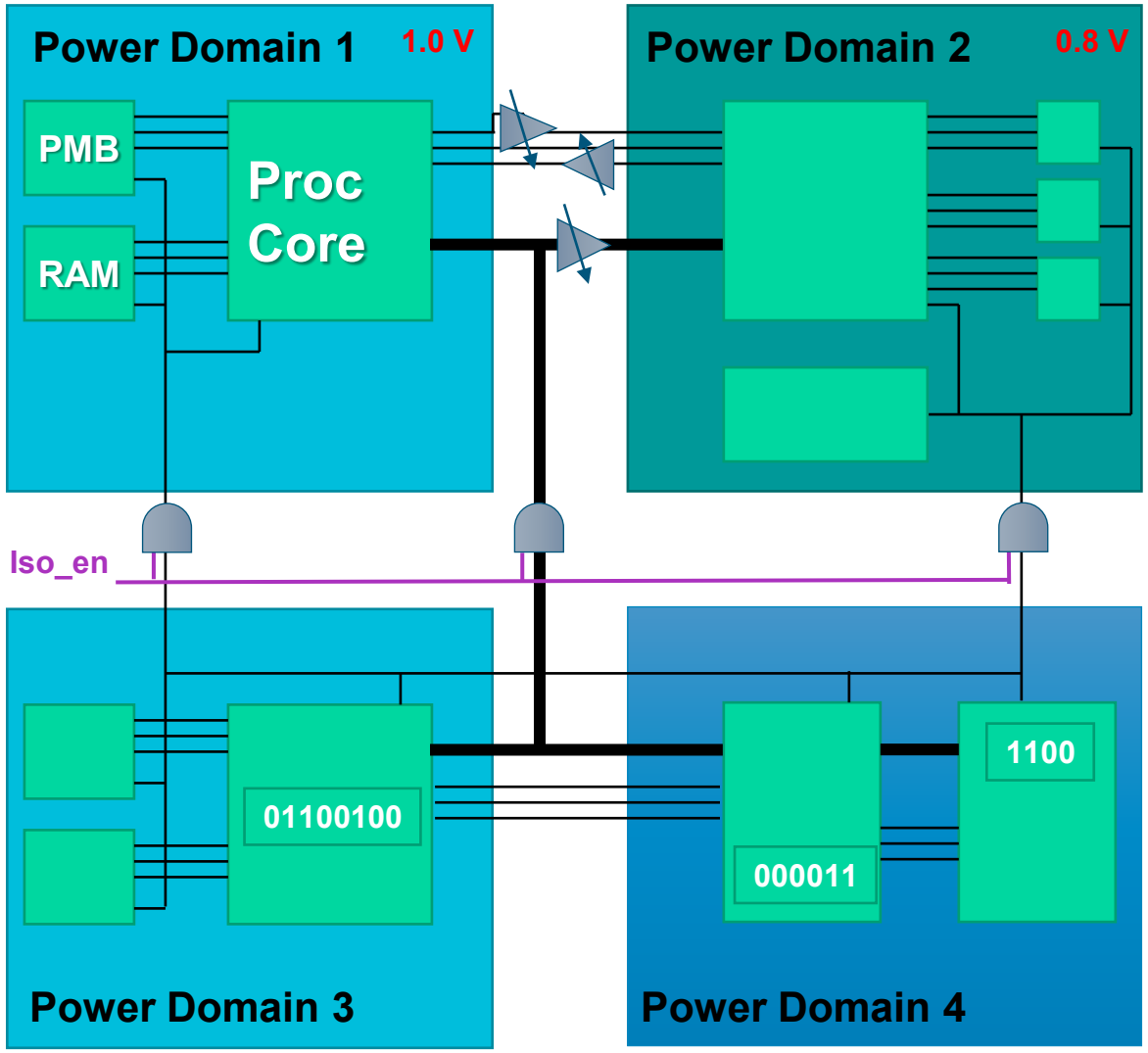
- Today's increasingly complex SoCs are typically used in portable systems
  - Must support increasingly longer battery life
  - Therefore, must minimize power consumption
- Even non-portable systems must avoid wasting energy
  - To minimize both power and cooling costs
- Active power management is required to ensure energy efficiency
- Active power management creates many new verification challenges
- The IEEE Std 1801 Unified Power Format (UPF) is a standard for specifying power intent in power aware verification of SoC



Source: Techcrunch

Power Management Techniques

- Power Domains
- Supply Networks
- Power Gating
- Corruption
- Isolation
- Retention
- Multi-Voltage
- Level Shifting
- Body Bias
- Power States
- Simstates



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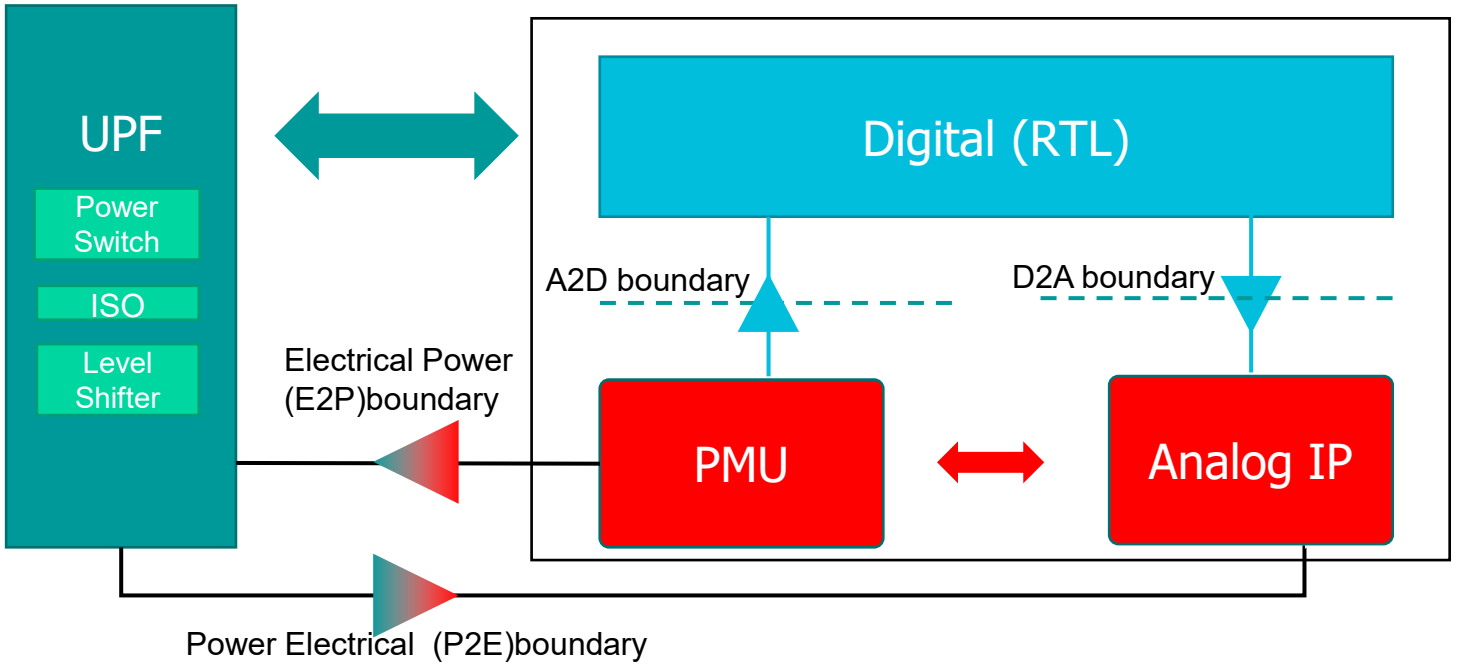
Extend Power Aware Simulation to Mixed-Signal

- Improve Verification Coverage achieved using power-aware methodology with UPF
- Replace the digital DUT with a mixed-signal DUT
- Keep the same TB and UPF infrastructure

Power Boundary Elements are automatically inserted

- P2E : Translates Power supply nets into Voltages to allow the analog block to respond to UPF specification
- E2P : Translates Voltage into Power states that UPF specification and read and respond to



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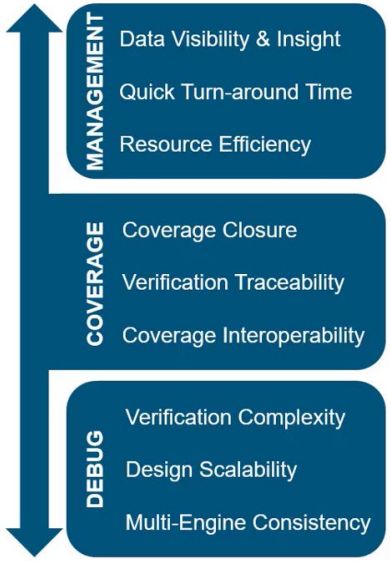
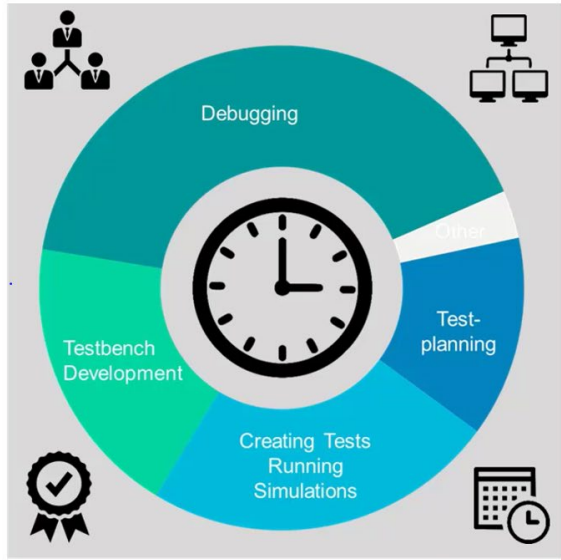
Coverage Closure for a Mixed-Signal Regression

Mixed-Signal Verification is becoming part of sign-off regression flows

There is need to:

- Organize, optimize, and manage mixed-signal regressions
- Automate the mixed-signal regression process
- Manage the simulation regression results efficiently, which enhances debug productivity
- Manage different kinds of compute job for example, Symphony simulation runs, or mixed-signal tcl post-processing





Source: Wilson Research Group and Siemens EDA, 2020 Functional Verification Study

There is a need for a unified solution to accelerate mixed-signal verification closure

Answer: Yes!

- Accellera Systems Initiative: Working on new AMS standards
- Siemens EDA: Working on new Mixed-Signal Simulation Technologies

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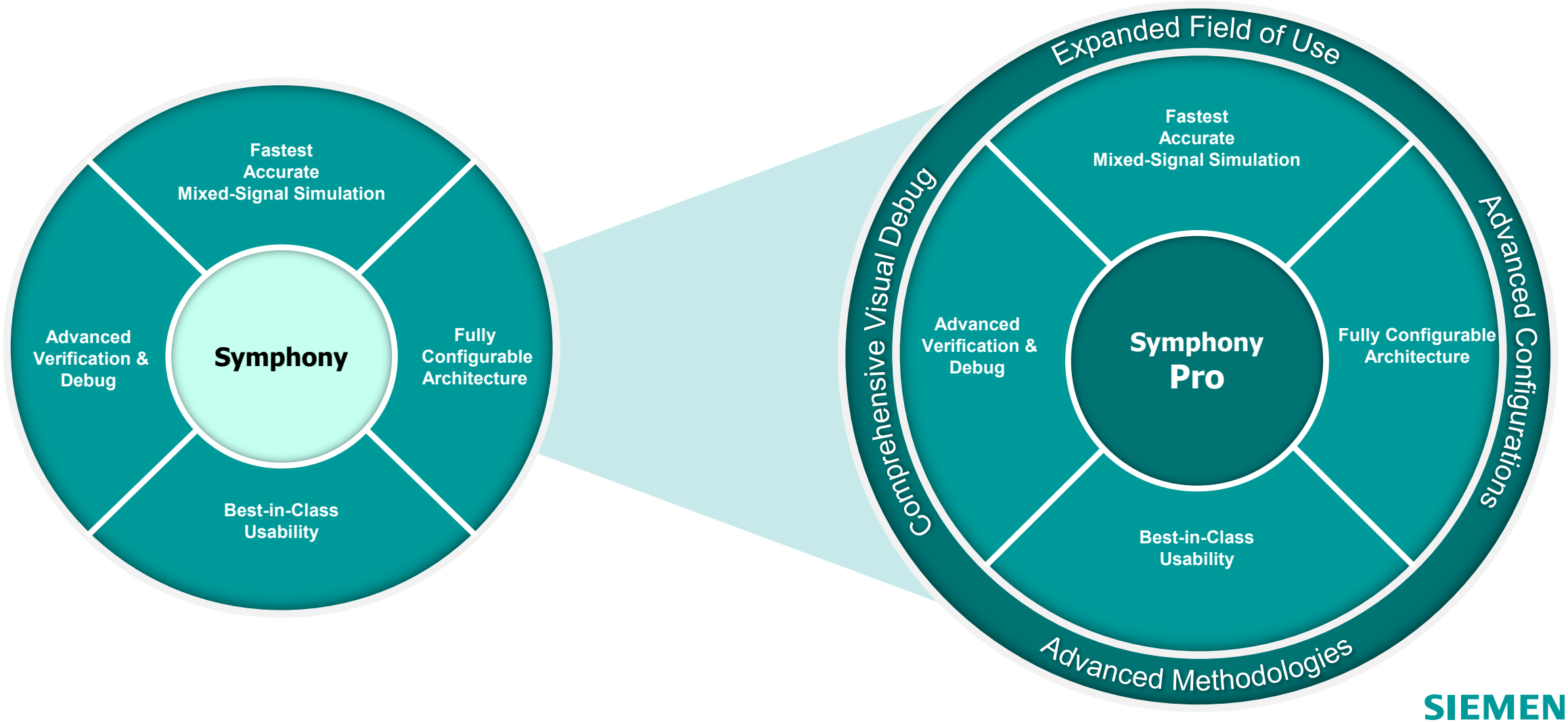
- Demo

Symphony Pro
Accelerate Advanced Mixed-Signal Verification with Comprehensive Visual Debug



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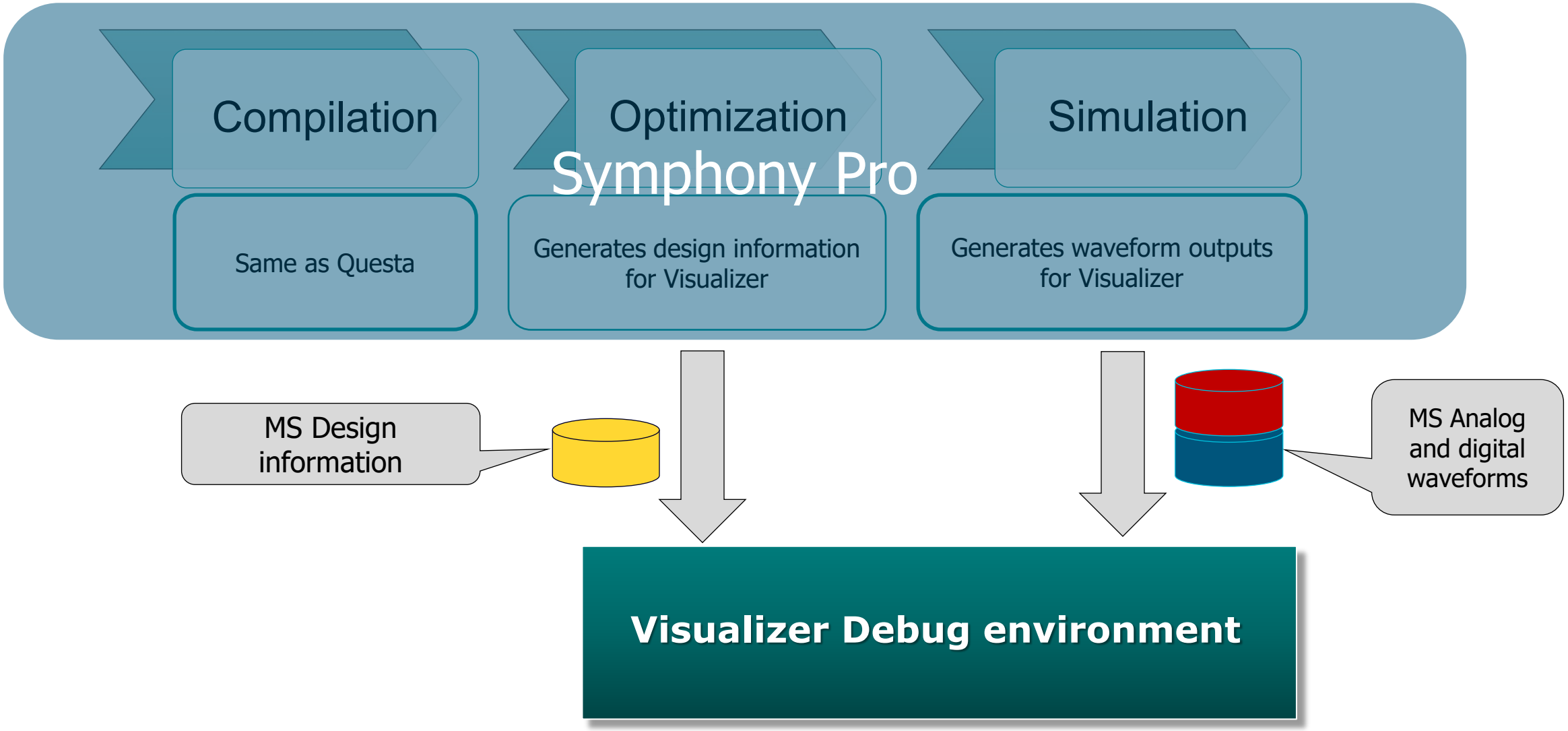
Symphony Current Field of Use (FoU)

Symphony Pro Visualizer Flow & Architecture



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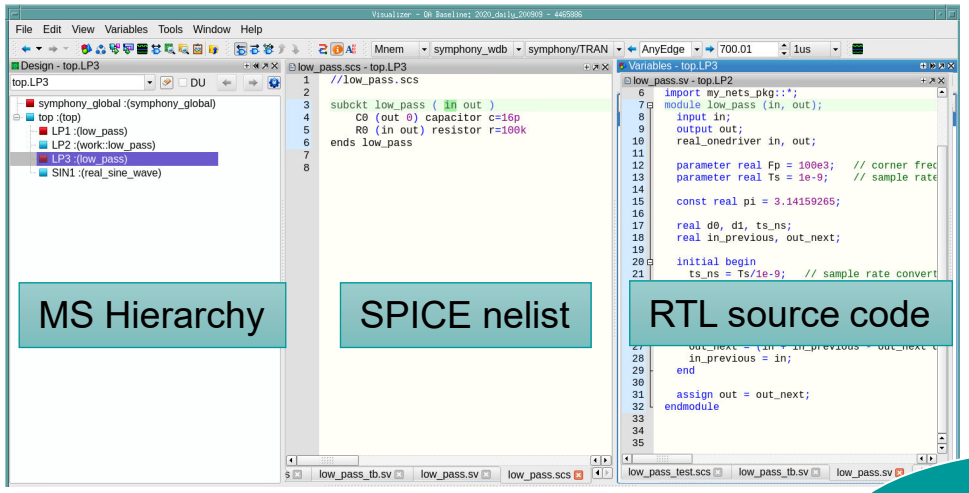
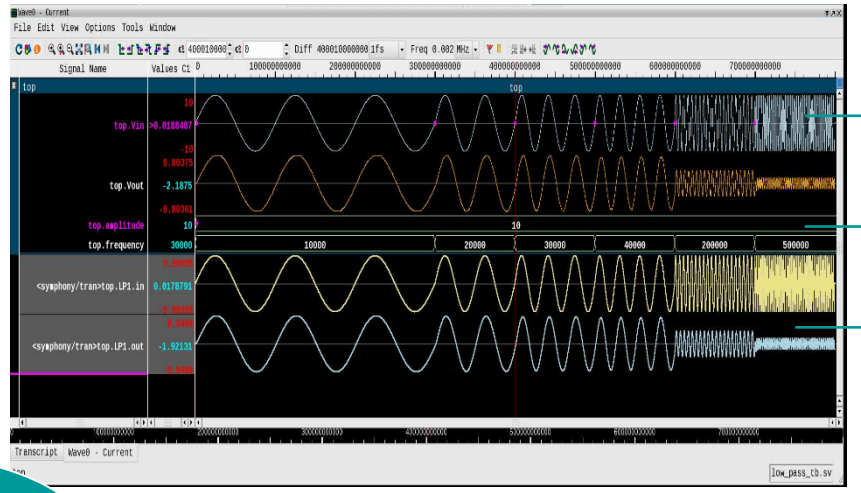
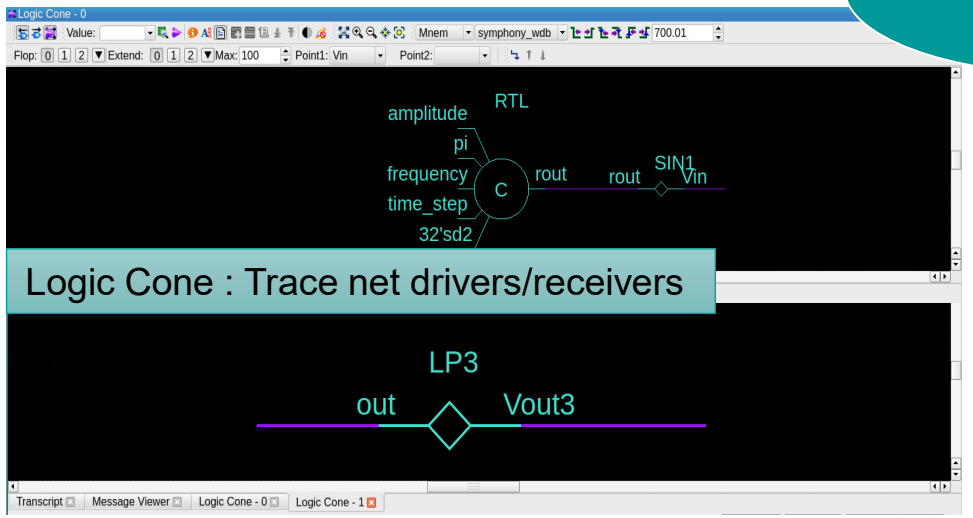
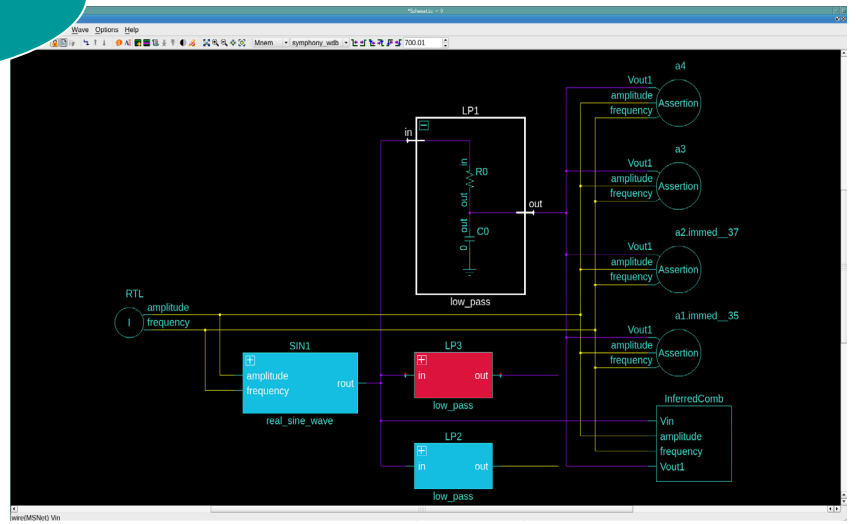
Visualizer MS : Comprehensive Mixed-Signal Debug





Visualizer MS*





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Visualizer MS Key Capabilities

Design Window showing the entire MS hierarchy

- Color coding for different languages

Source Window to view design block source code

- HDL languages and SPICE

Variables Window: Show Nets in the selected block

- MS Nets clearly delineated visually

Schematic Window: Connectivity view of the design

- Instance based connectivity

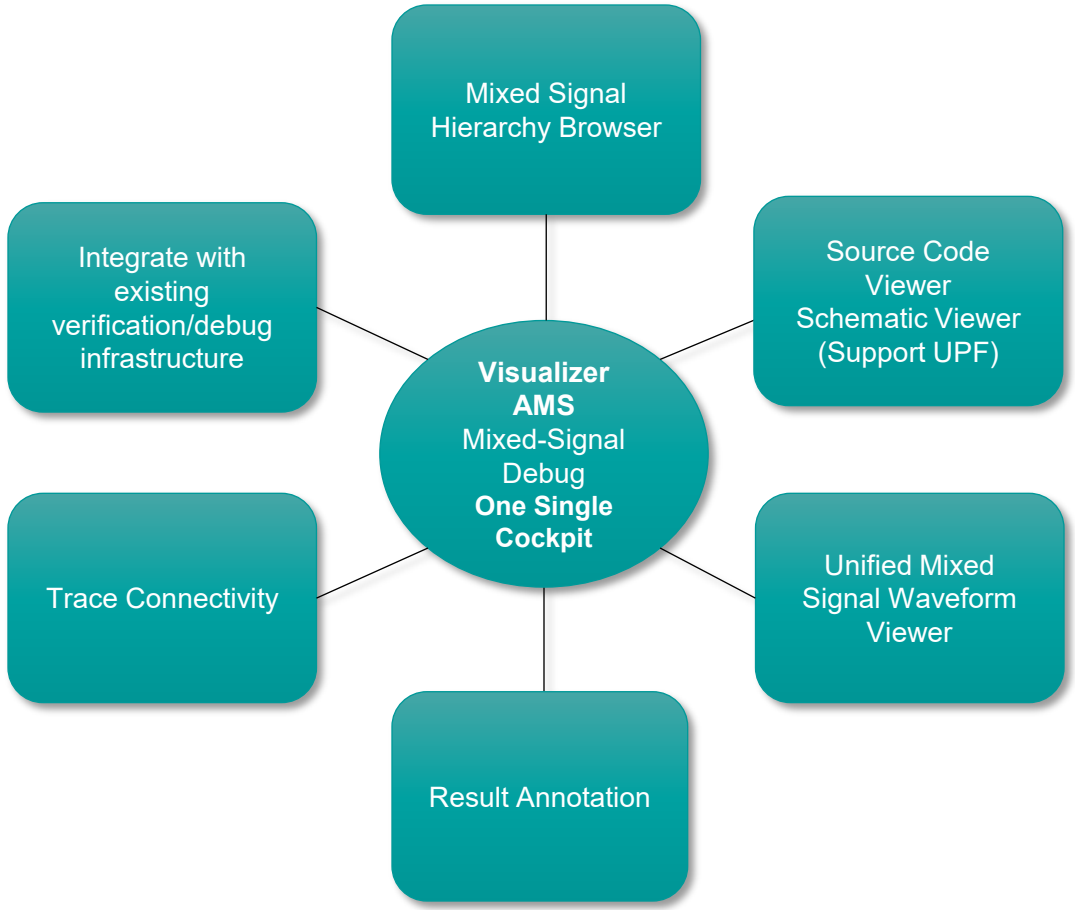
Wave window showing waveforms including BE values

- Back-annotation to schematic window

Logic Cone Window for Driver/Receiver Tracing

MSNet Window

- View of all mixed-signal nets and BEs inserted



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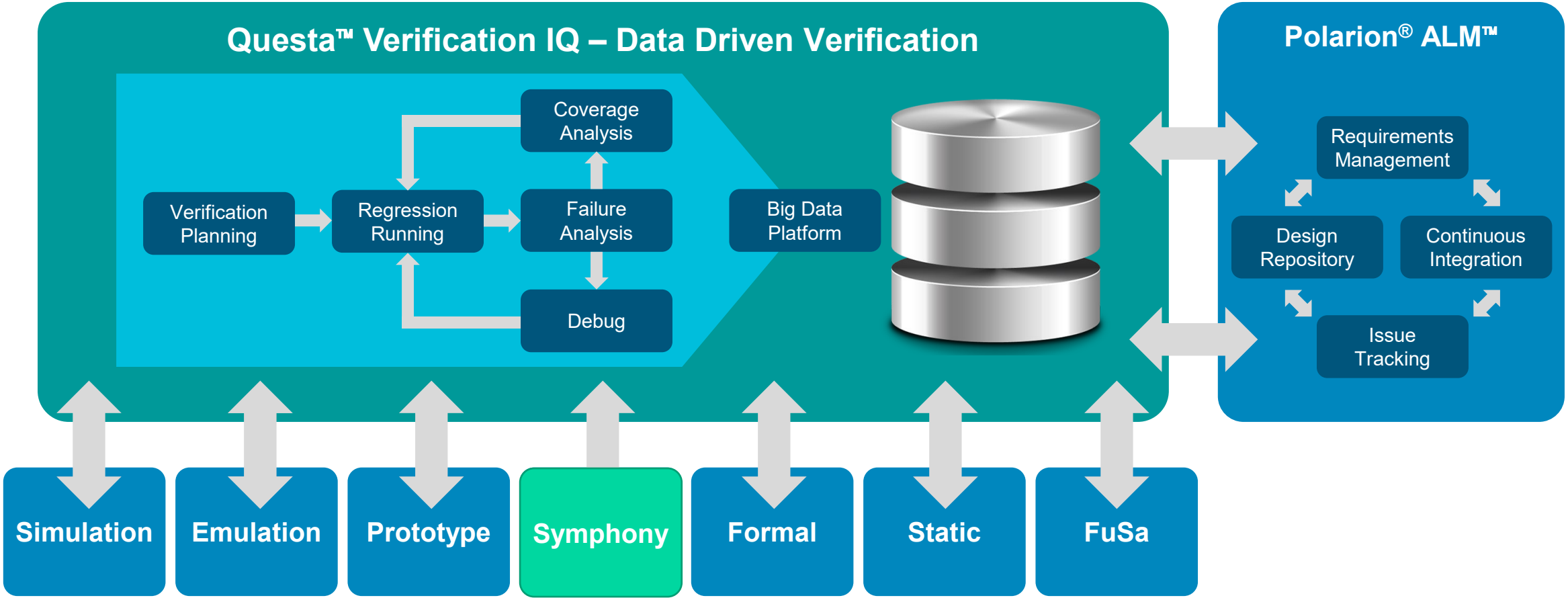
Symphony integrates with VIQ - Collaborative Data Driven Verification Powered by Analytics



Symphony Pro Customer Testimonials

"Mixed-Signal functional verification is increasingly vital for our sophisticated designs targeted for the imaging and automotive industries. We've participated in the early access program for Symphony Pro and have seen significant productivity gains thanks to advanced debugging capabilities and seamless support for multi-layer sandwich configurations in Symphony Pro. We look forward to using Symphony Pro as our sign-off solution for present and future mixed-signal verification projects." - STMicroElectronics

"Our high-performance, energy-efficient chips designed for the IoT are analog intensive and mixed-signal in nature. To ensure high quality, we expanded our digital verification methodology to enable effective regression of our mixed-signal designs. Symphony Pro Visualizer mixed-signal technology accelerated debug turn-around time for our digital on top UVM test suites, enhancing our verification productivity from days to hours and dramatically improving our coverage closure." – Silicon Labs

Summary

- Symphony is digital simulator agnostic

- Symphony Pro is an advanced tier of Symphony
  - Support advanced capabilities, configurations and debug
  - Symphony Pro is not replacing Symphony
  - Symphony Pro works only with Siemens-EDA simulators

- If you are Siemens EDA customer, you can take advantage of Symphony Pro capabilities right away
  - Please contact your Siemens EDA sales team

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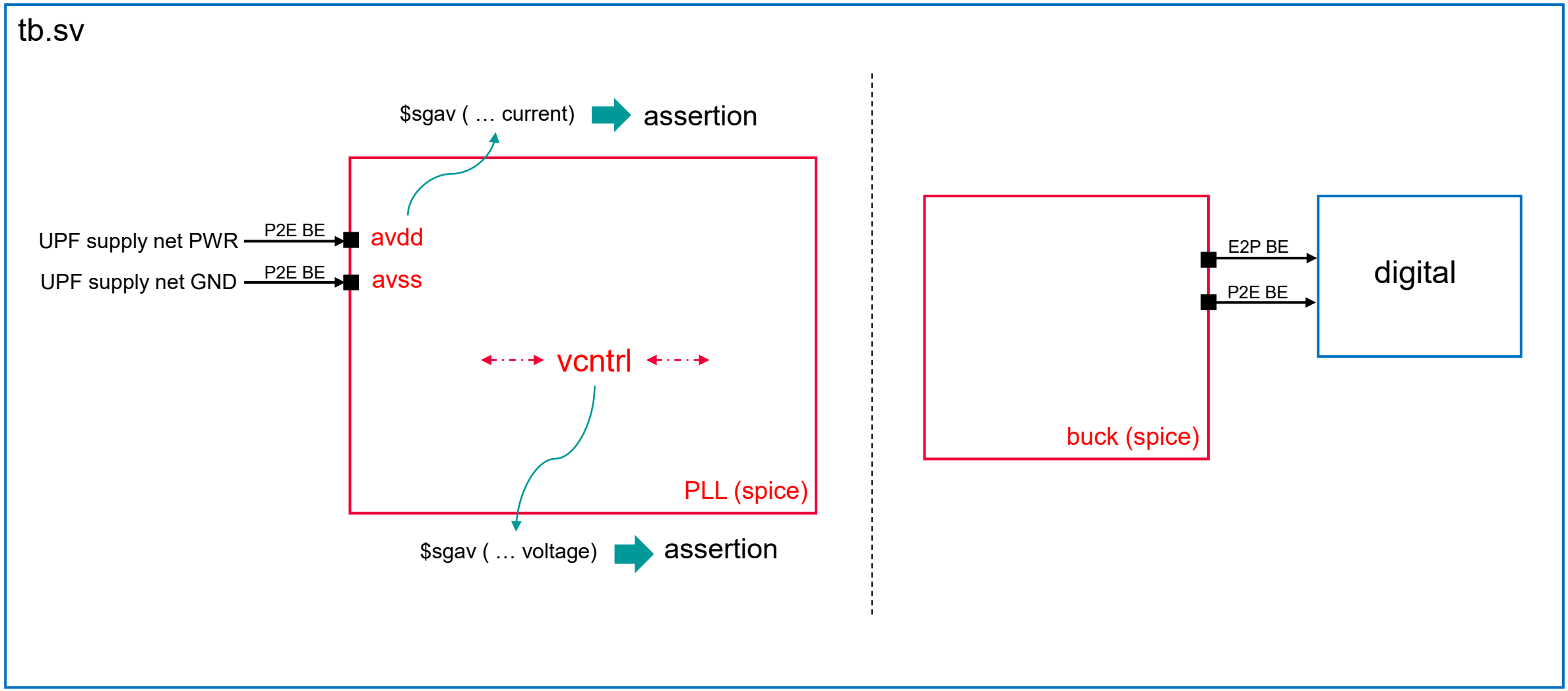
Demo description

- In this demo we are going to see how to connect UPF supply nets to analog (electrical) ports through Symphony's power-aware E2P and P2E boundary elements, in one part of the demo we will focus on having UPF drive the analog circuit's supplies (P2E), and in another part, we will see how an analog circuit can drive the UPF supplies (P2E), we will also see how to use Symphony's access functions to monitor the analog circuit's currents and internal node voltages to create mixed-signal assertions, all within the Visualizer mixed-signal debugging platform.
- We will also demonstrate how to integrate a Symphony mixed-signal simulation example inside VIQ (Questa's Verification IQ).
- And finally, we will show some of the upcoming Real Number Modeling features related to user-defined nettypes connectivity.

Demo Diagram



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Contact

Sumit Vishwakarma
Product Manager
Mixed Signal Verification

E-mail Sumit.vishwakarma@siemens.com

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