2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

SAN JOSE, CA, USA
FEBRUARY 27-MARCH 2, 2023

A Methodology for Power and Energy Efficient Systems Design

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SIEMENS

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Agenda

- Power and Energy as Key Metrics
- RTL Power Analysis – Need, the Challenges and a comprehensive methodology
- The proposed methodology
- Brief discussion about the key elements of the proposed methodology
- Power and Energy Reporting in PowerPro
- Summary

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Power and Energy – Getting the centerstage

Power and Energy As Key Design Metrics

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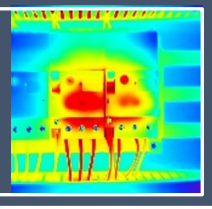
Power is everywhere…

- Battery Life 
- Eco Friendly 
- OpEx 

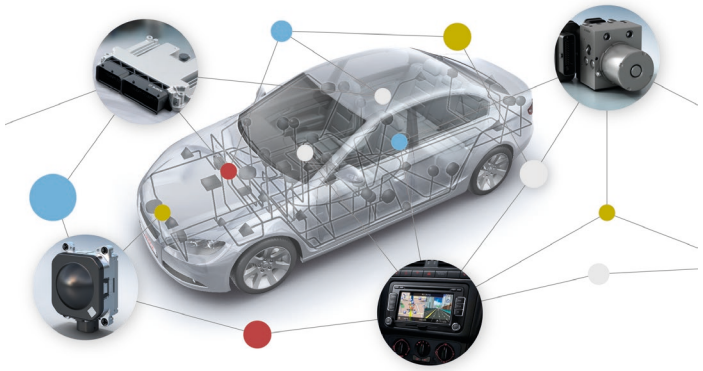
- Heat 

Mobile

Data Center

Processing

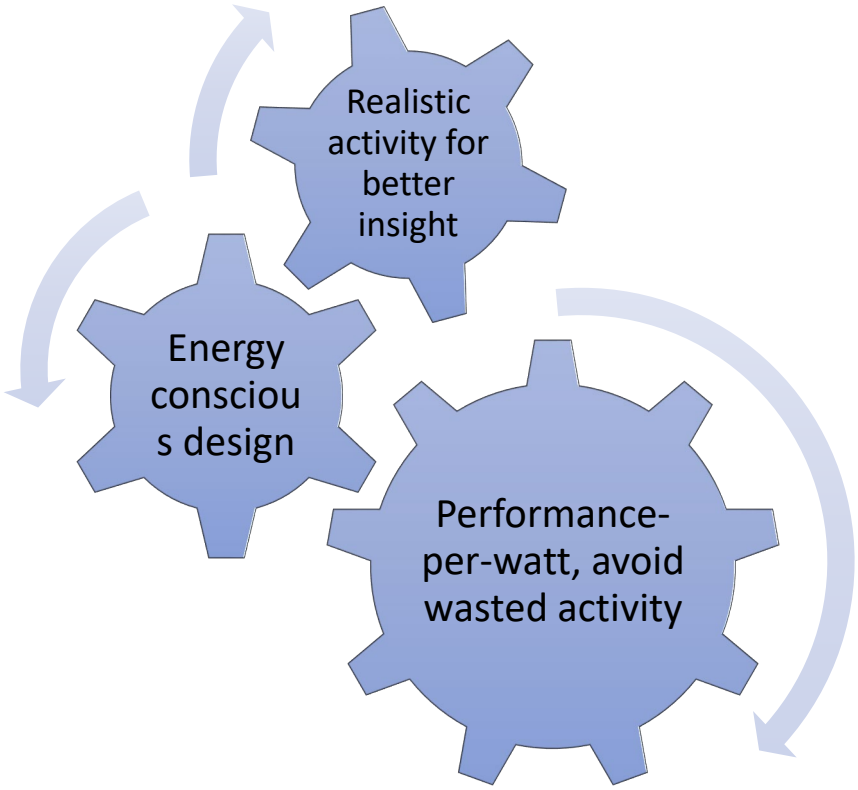
Networking



Automotive

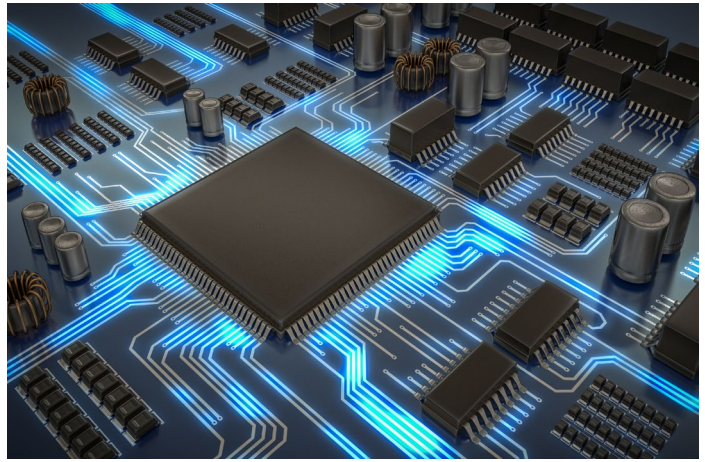
The Need for an Energy Conscious Design Strategy

Energy efficiency unfortunately doesn't mean pulling the supply down! We need a comprehensive design strategy to achieve that.



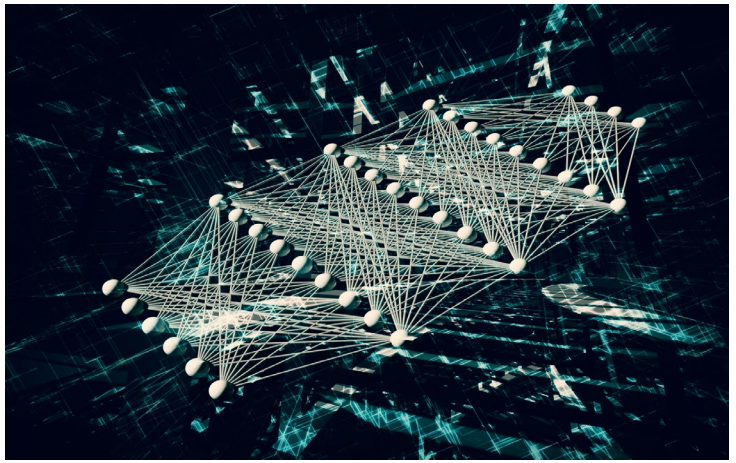
De-carbonization of compute Infrastructure

Power and Energy becoming a key design consideration



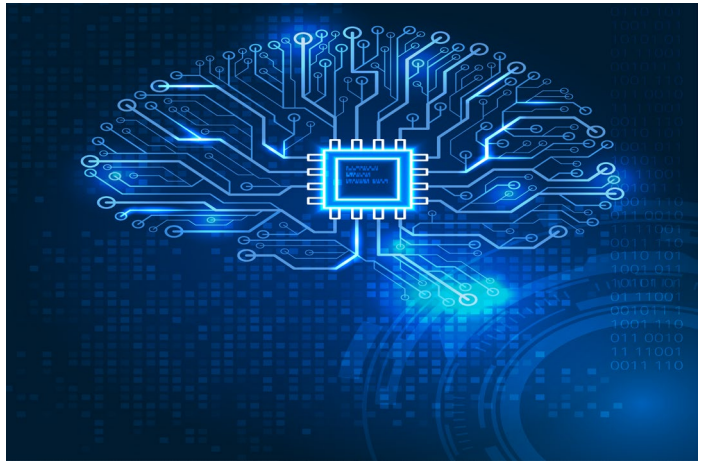
Speed/Timing Critical

Desktop Personal Computing-
Mainly MH/GH race



Power & Timing Critical

Design Complexities Making
Power and Timing Critical



Power & Energy Critical

Complex AI/Big Data
Application Processors

Compute Technology Trend

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RTL Power/Energy

The benefits of a fast and accurate RTL Power Analysis Flow

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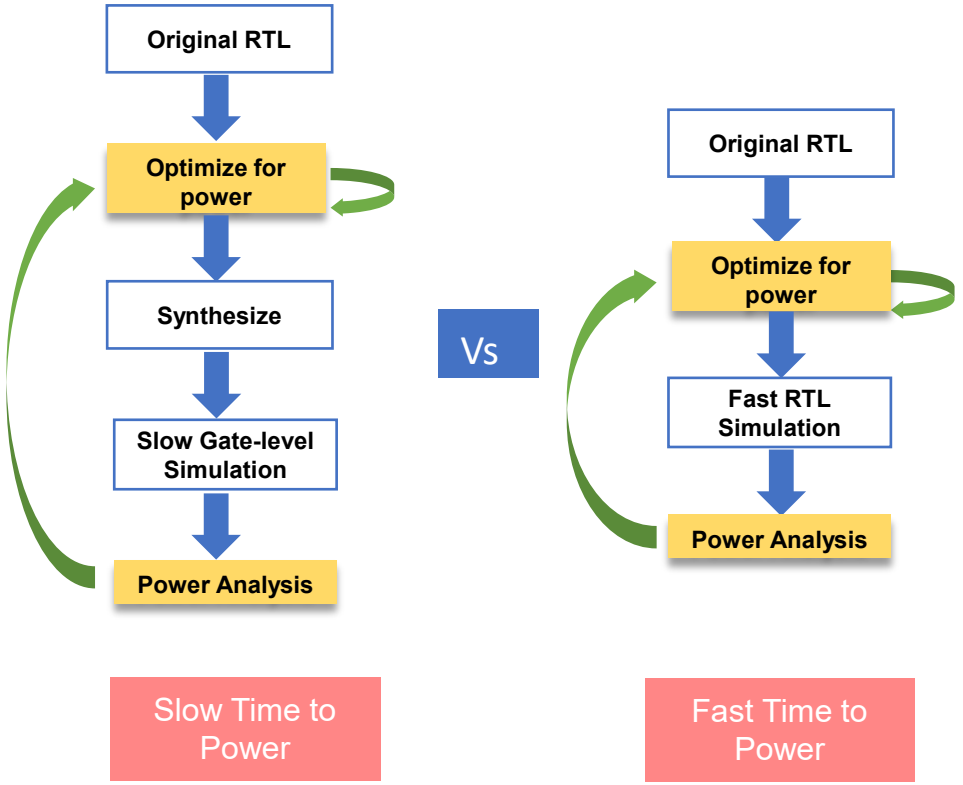
RTL Power Analysis, Why and Where?

RTL Power Analysis		GL Power Analysis	
Fast TTP (Time to Power)	↑	Long TTP (Time to Power)	↓
Flow owned by single team	↑	Inter-team dependency	↓
Best speed-accuracy trade-off	↑	More suitable for accuracy.	↓
Faster iterations (allows What-if analysis)	↑	Time consuming iterations	↓
Near accurate Power numbers. Good for relative comparison	↑	Comparatively accurate Power numbers	↑



RTL Power -*The Challenges*

Difficult Tool Setup

- Provide inputs like waveform, physical information etc
- Calibration for Power Estimation

Power Analysis and Large TAT

- May require deeper analysis of reports to understand the problems and fix them, often late in the design cycle

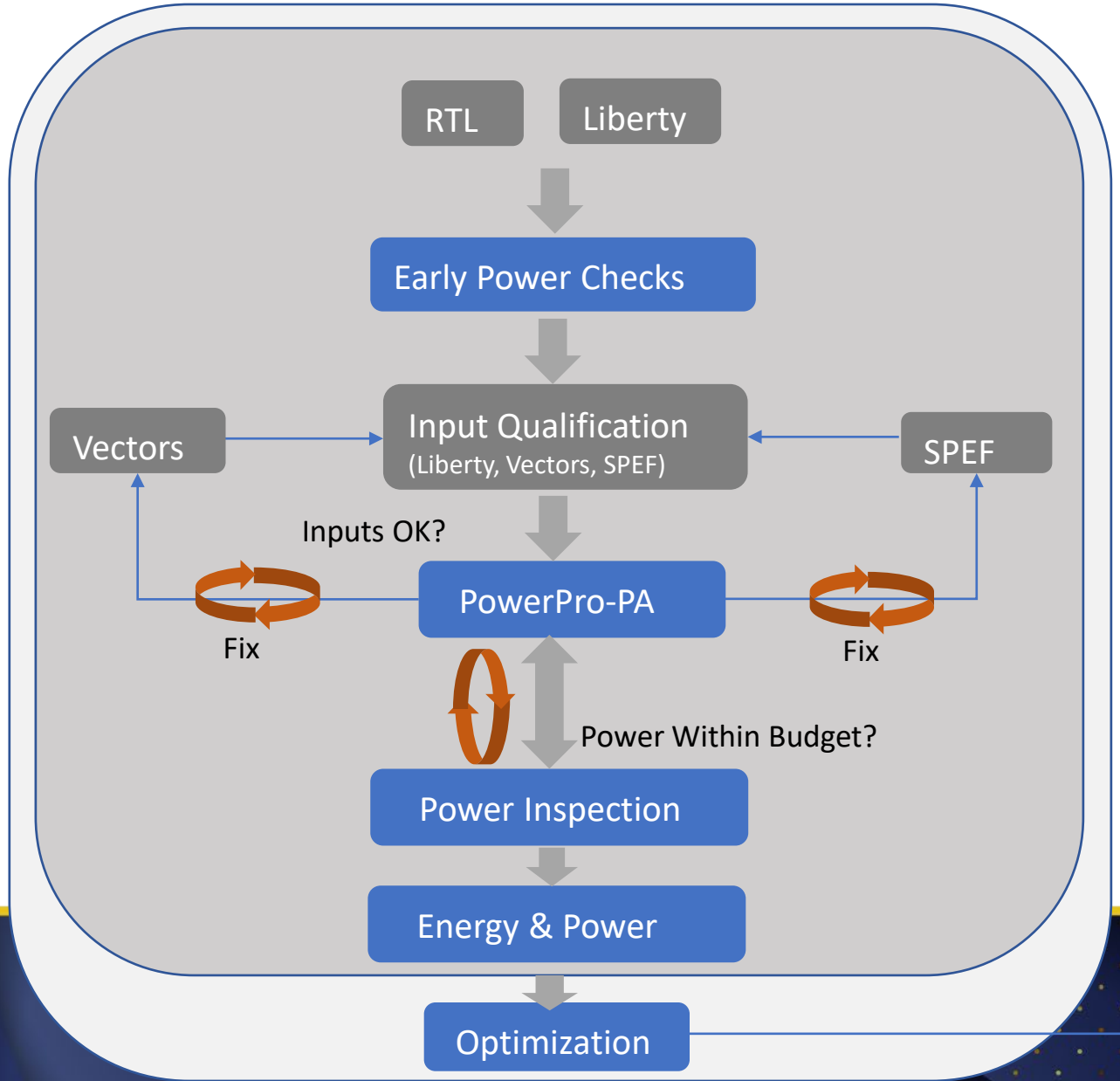
Late Consideration of Power

- Lack of time to find and fix power issues
- Discovering problems late will delay schedules

RTL Power -*The Essential ingredients of the Required Methodology*

- Support Structural Checking when Vectors are not ready yet
- Helps clean inputs and provide power coverage insight
- Helps quick Power/Energy trending and tracking in regression
- Helps inspect the Power and Energy profile for optimization opportunities

Methodology for Power/Energy Exploration and Optimization



Regression Ready Framework
Power/Energy Analysis and Optimization

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Early Power Checking using EDCs

Structural Power Linting for Catching Low Hanging Power Issues Early-on

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Early Design Checks

Structural Analysis of RTL to reveal power issues upfront

- Can be run without vectors
- Runs extremely fast
- Performs structural analysis of the RTL to find potential issues that can impact power downstream
- EDC metrics can be used to qualify IPs for lowpower

Coverage Checks

Design Checks

Early Design Checks		
Ungated Memories	9	81.82 %
Ungated Macros	1	50 %
Ungated Memory Inputs	49 Input(s)	100 %
Ungated Operator Inputs	8 Input(s)	
Ungated Flops	613	59.8 %
Ungated MUX Inputs	9 MUX Inputs	
Not Combinationally Enabled Flops	728	71.02 %
Floating Memory Data Outputs	1 Output(s)	0.09 %
Memory Redundant Toggle Inputs	11 Input(s)	73.33 %
Constant CGICs	3	17.65 %
Functionally Redundant CGICs	4	23.53 %
Structurally Redundant CGICs	2	11.76 %

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Input Qualification

Cleanup the inputs, otherwise it is Garbage-in-Garbage-out

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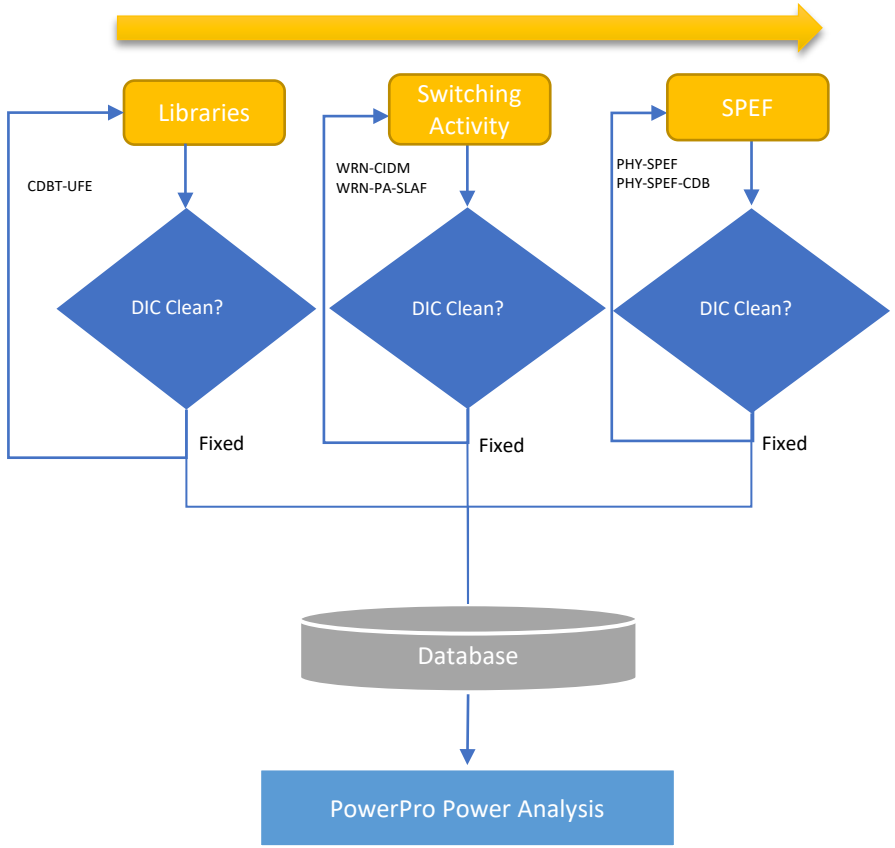
Power Setup and Input Quality Check

Ensure first-time right power estimates with data integrity checking

- Correct setup leads to correct power estimates !
  - Incorrect setup and deficient inputs can lead wrong power estimates, longer TAT
- Did I provide the correct setup?
  - Setup can be wrong unintentionally, leading to incorrect power numbers
- Quality of input determines the quality of output
  - Data integrity checks (DICs) ensure that the input provided is not deficient
  - Quality checks at each step (Libraries, SPEF, Waveform)



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Power Analysis

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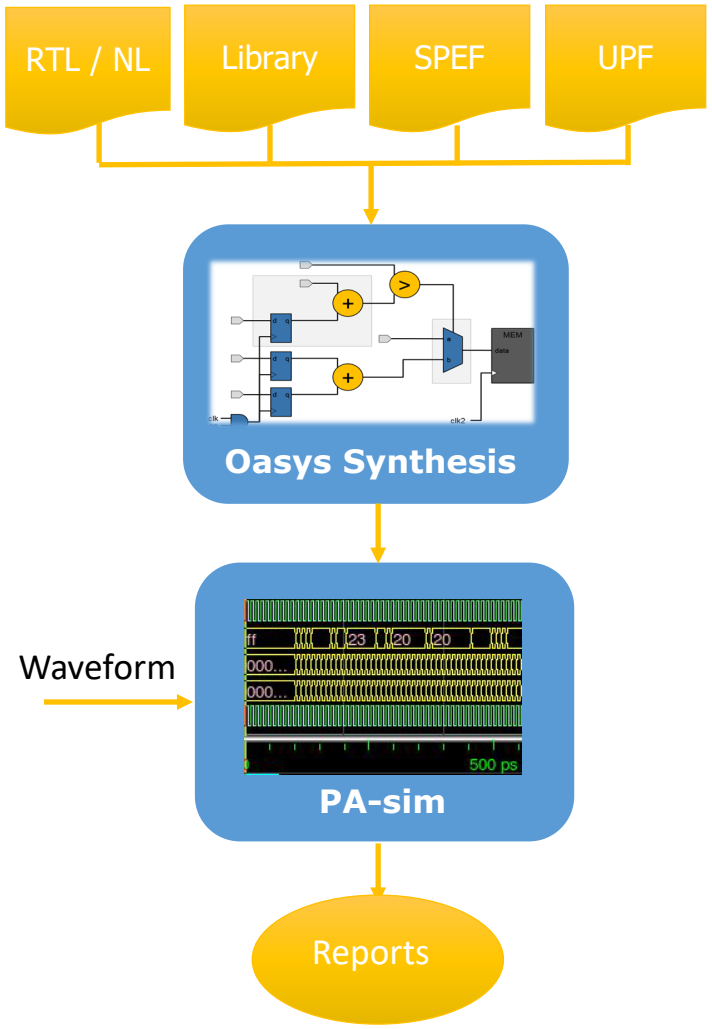
Comprehensive Power Analysis

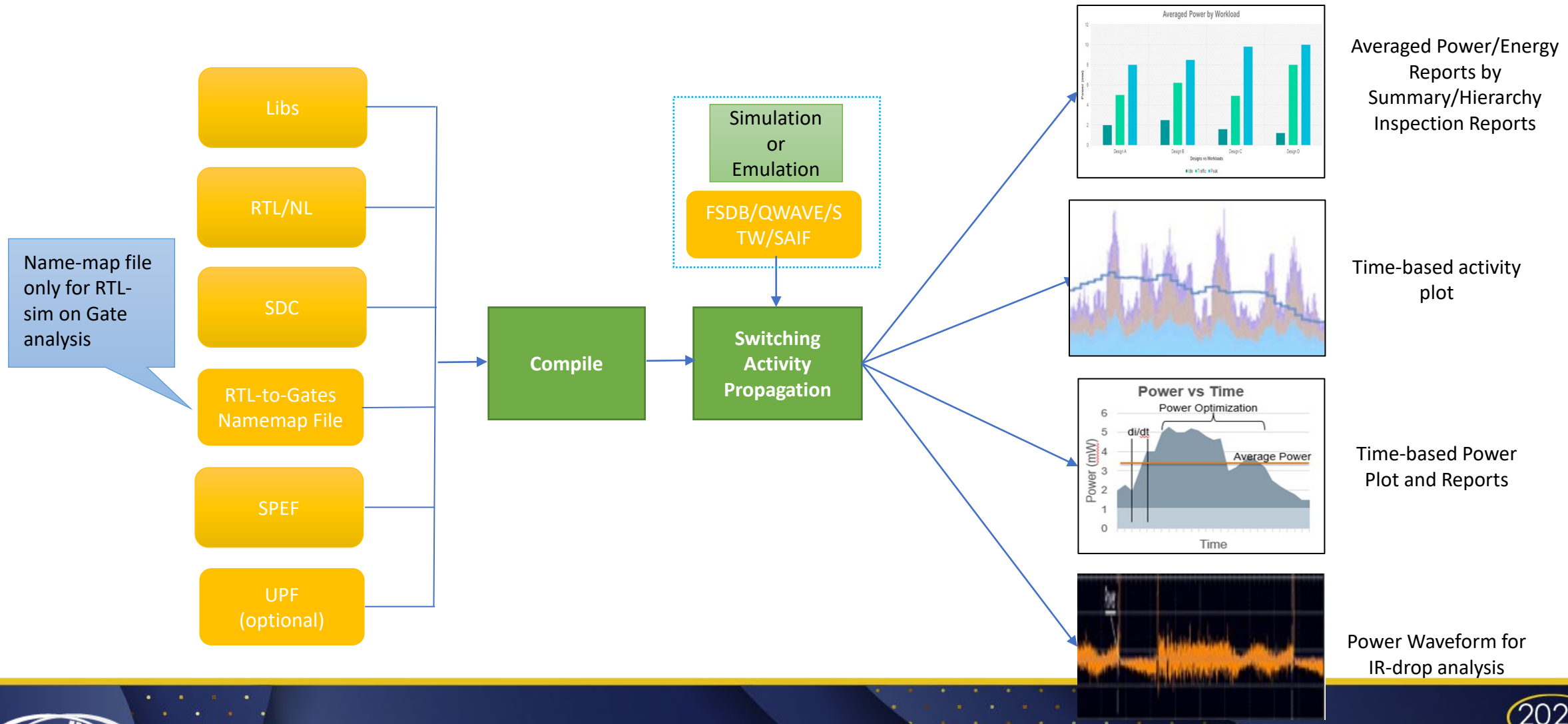
Complete portfolio for Power Analysis, from early RTL to Gate, IP to SoC

- **Accurate RTL and Gate-level Power Estimation**
  - RTL Power Accuracy within 15% of layout
  - Gate Power Accuracy within 3% of layout
  - Ability to use RTL stimuli to perform Gate-level Power Analysis
- **Averaged Power and Time-based Power**
  - Averaged Power
  - Time-based Power (Cycle-Accurate)
  - Supported switching activity formats: QWAVE, FSDB, SAIF, STW
- **Detailed Reports and Intuitive Debug**
  - Summary Power, Hierarchical Power
  - Power by Component/Category
  - Power by Clock Domain
  - Intuitive GUI with cross-probing, querying, filtering etc



Averaged and Time-based Power Analysis

RTL, Gate and RTL-stimulus-on-Gate



Averaged Power/Energy Reports by Summary/Hierarchy Inspection Reports

Time-based activity plot

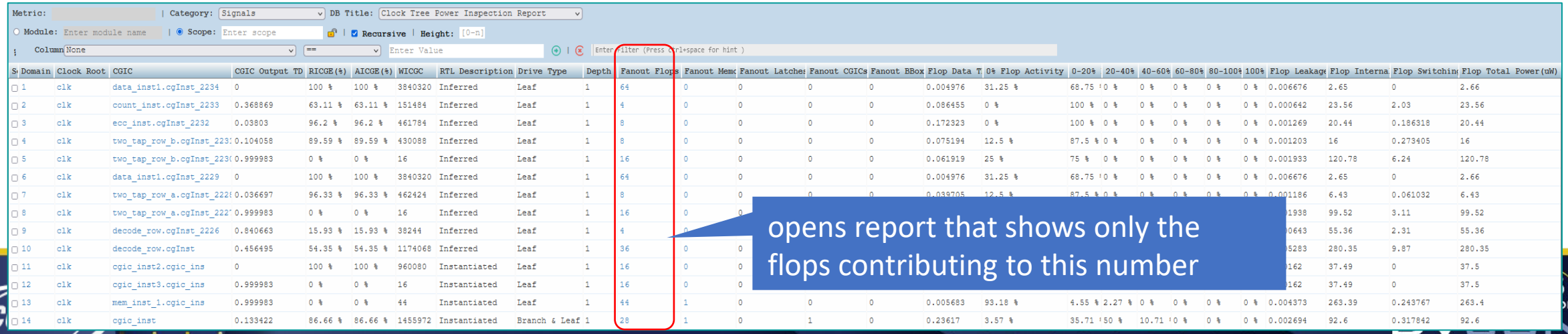
Time-based Power Plot and Reports

Power Waveform for IR-drop analysis

Power Inspection Reports

- Power Inspection
  - New set of reports to visualize, inspect and determine gating opportunities for Flops/Memories
  - Clock-Tree visualization for holistic view of gaters in the design and their effectiveness
  - Fan-out profile per clock root/ICG along with toggle profile for detailed analysis
  - Detailed Flop and Memory reports to analyze and find potential solutions for gating

Power Inspection		
Clock Tree Power Inspection	21.65%	63.35 uW
Flop Power Inspection	51.22%	111.29 uW
Memory Power Inspection	12.34%	24.46 uW
Glitch Power Inspection	18.85%	41.37 uW



Average Power Report

Command

Library Used

Design Hierarchy and Characteristic

PVT Corner

Average Power Summary

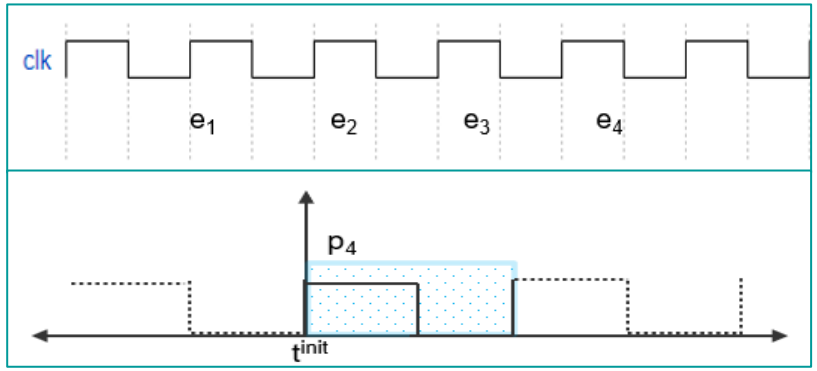
```
powerpro> report_power
Library(s) Used:
  sc9_base_lvt_tt_typical_max_0p90v_25c
  sc9_base_lvt_ff_typical_max_0p72v_0c
  sadrlskkb2p256x64m2b2w0c1p0d0t0_lib
…..

Operating Conditions    : tt_typical_max_0p90v_25c
  ------------------------------------------------------------------------------
  Design                    | Target Libraries        | Voltage | VTH Distribution
  ------------------------------------------------------------------------------
  dut                         All                         0.9
  uut.rxReceiveEngine         All                         0.9
  ……
  ------------------------------------------------------------------------------
Global Operating Voltage = 0.9
Power-specific unit information:
  Voltage Units       = 1V
  Capacitance Units   = 1pf
  Time Units          = 1ns
  Dynamic Power Units = 1uW
  Leakage Power Units = 1uW
…..Power Summary Report
-------------------------------------------------------------------------------------------------------------------------------
Power Group     Count          Leakage Power(uW)      Internal Power(uW)     Switching Power(uW)    Total Power(uW)        Percentage(%)
-------------------------------------------------------------------------------------------------------------------------------
io_pad          0              0                      0                      0                      0                      0%
memory          5              263.897                278.173                0                      542.07                 20.93%
black_box       2              0                      0                      1.467e-03              1.467e-03              0%
register        2136           169.694                770.985                0.30607                940.985                36.33%
combinational   12414          693.335                24.0329                13.8433                731.211                28.23%
sequential      0              0                      0                      0                      0                      0%
clock_network   2              20.2277                350.193                5.22296                375.644                14.5%
total           14559          1147.15                1423.38                19.3738                2589.91                100%
```

Cycle Accurate Peak Power (CAPP) Report

- Energy value is computed for each event (toggle) in the design
- CAPP analysis provides cycle level accurate power behavior for the design

```
report_power -time_based
```



Power Summary Report

Power Group	Count	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)
io_pad	0	0	0	0	0
memory	11	2941.41	7750.67	2.38406	10694.5
black_box	0	0	0	0	0
register	975	0.118966	8665.94	235.431	8901.49
combinational	978	60.0481	486.968	846.197	1393.21
sequential	0	0	0	0	0
clock_network	345	0.0121443	987.864	1325.48	2313.35
total	2309	3001.59	17891.4	2409.49	23302.5

Energy Reports

- Power & Energy both are critical parameters in low power/energy circuit design.
- Power defines rate of energy consumption per unit time.
- Like power, it is also necessary to know total amount of consumed energy in given simulation timeline.
- Along with power reports, users also want energy consumption reports.

```
Energy Summary Report
-------------------------------------------------------------------------------------------------------------------------------------------------------
-------------------------------------------------------------------------
Power Group     Count          Leakage Power(uW)    Leakage Energy(uJ)    Internal Power(uW)    Internal Energy(uJ)    Switching Power(uW)    Switch
ing Energy(uJ)    Total Power(uW)    Total Energy(uJ)    Percentage(%)
-------------------------------------------------------------------------------------------------------------------------------------------------------
-------------------------------------------------------------------------
io_pad          0              0                    0                     0                     0                      0                      0
                  0                  0                    0%
memory          11             2941.41              0.176499              7750.67               0.465079               2.38                   1.4305
58e-04            10694.46           0.641721             45.89%
black_box       0              0                    0                     0                     0                      0                      0
                  0                  0                    0%
register        975            0.118966             7.138571e-06          8665.94               0.52                   235.43                 0.0141
271               8901.49            0.534134             38.2%
combinational   978            60.05                3.603187e-03          486.97                0.0292205              846.2                  0.0507
76                1393.21            0.0835998            5.98%
sequential      0              0                    0                     0                     0                      0                      0
                  0                  0                    0%
clock_network   345            0.012144             7.287208e-07          987.86                0.0592768              1325.48                0.0795
352               2313.35            0.138813             9.93%
total           2309           3001.59              0.18011               17891.44              1.07358                2409.49                0.1445
81                23302.51           1.39827              100%
```

Toggle Activity Reports/Plot

```
report_toggle_profile -start_instance {TOP_HIER large_mem_inst
large_mem_inst_1 mem_inst mem_inst1 mem_inst3 mem_inst_1} -
toggle_waveform mems.vcd
```

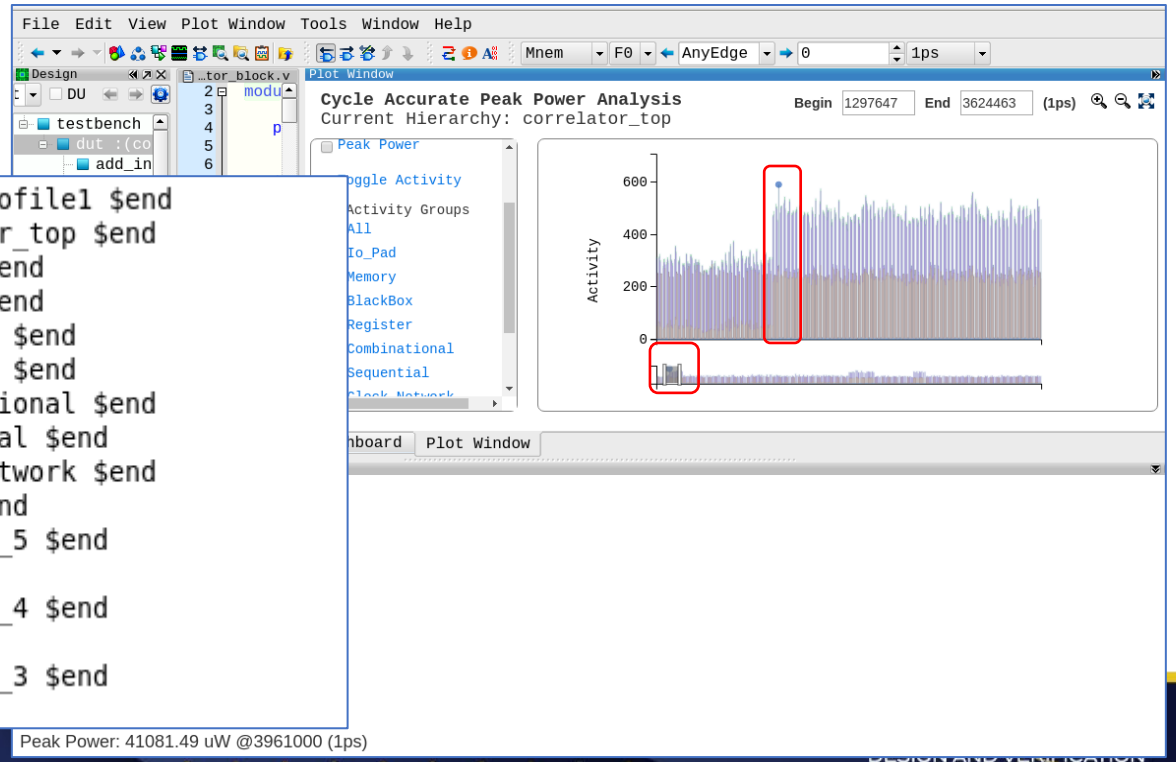
```
----------------------------------------------------------------------------------------------------
Toggle Profile Analysis (Power Group: 'Register')
----------------------------------------------------------------------------------------------------
Summary:
        Instance                                        = correlator_top
        Start Time for Toggle Profile analysis          = 0
        End Time for Toggle Profile analysis            = 60005000
        Average Toggle Count of analysis window         = 0.12133
        Peak Toggle Count of analysis window            = 306
        Peak Toggle Count timestamp                     = 58735500
        Timescale for all above timestamps              = 1ps
        Detailed Report                                 = Toggle_Profile_Register_


----------------------------------------------------------------------------------------------------
Toggle Profile Analysis (Power Group: 'Register')
----------------------------------------------------------------------------------------------------
Summary:
        Instance                                        = mem_inst_1
        Start Time for Toggle Profile analysis          = 0
        End Time for Toggle Profile analysis            = 60005000
        Average Toggle Count of analysis window         = 0.000716874
        Peak Toggle Count of analysis window            = 7
        Peak Toggle Count timestamp                     = 4500
        Timescale for all above timestamps              = 1ps
        Detailed Report                                 = Toggle_Profile_Register_


----------------------------------------------------------------------------------------------------
Toggle Profile Analysis (Power Group: 'Register')
----------------------------------------------------------------------------------------------------
Summary:
        Instance                                        = mem_inst1
        Start Time for Toggle Profile analysis          = 0
        End Time for Toggle Profile analysis            = 60005000
        Average Toggle Count of analysis window         = 0.000500292
```

Toggle waveform VCD

```
$scope module toggle_profile1 $end
$scope module correlator_top $end
$var real 64 ! IO_PAD $end
$var real 64 " Memory $end
$var real 64 # BlackBox $end
$var real 64 $ Register $end
$var real 64 % Combinational $end
$var real 64 & Sequential $end
$var real 64 ' Clock_Network $end
$var real 64 ( Total $end
$scope module cgic_inst_5 $end
$upscope $end
$scope module cgic_inst_4 $end
$upscope $end
$scope module cgic_inst_3 $end
$upscope $end
```



Conclusion and Summary

- Develop low-power, energy efficient RTL right from the beginning
- Early Design Checking (with EDCs) helps weed out low-hanging power issues without the need of vectors
- Input qualification helps remove structural or functional abnormalities in the provided inputs for right-at-first-time power/energy results
- Iteratively improve the power and energy efficiency of your RTL
- Regress RTL to track Power and Energy KPIs for qualifying the design for low power and energy

Questions

- What is CAPP?
- How PowerPro is able to provide accurate power numbers at the RTL level?
- How to run PowerPro in a regression framework to develop a robus power and energy efficient methodology at RTL level?