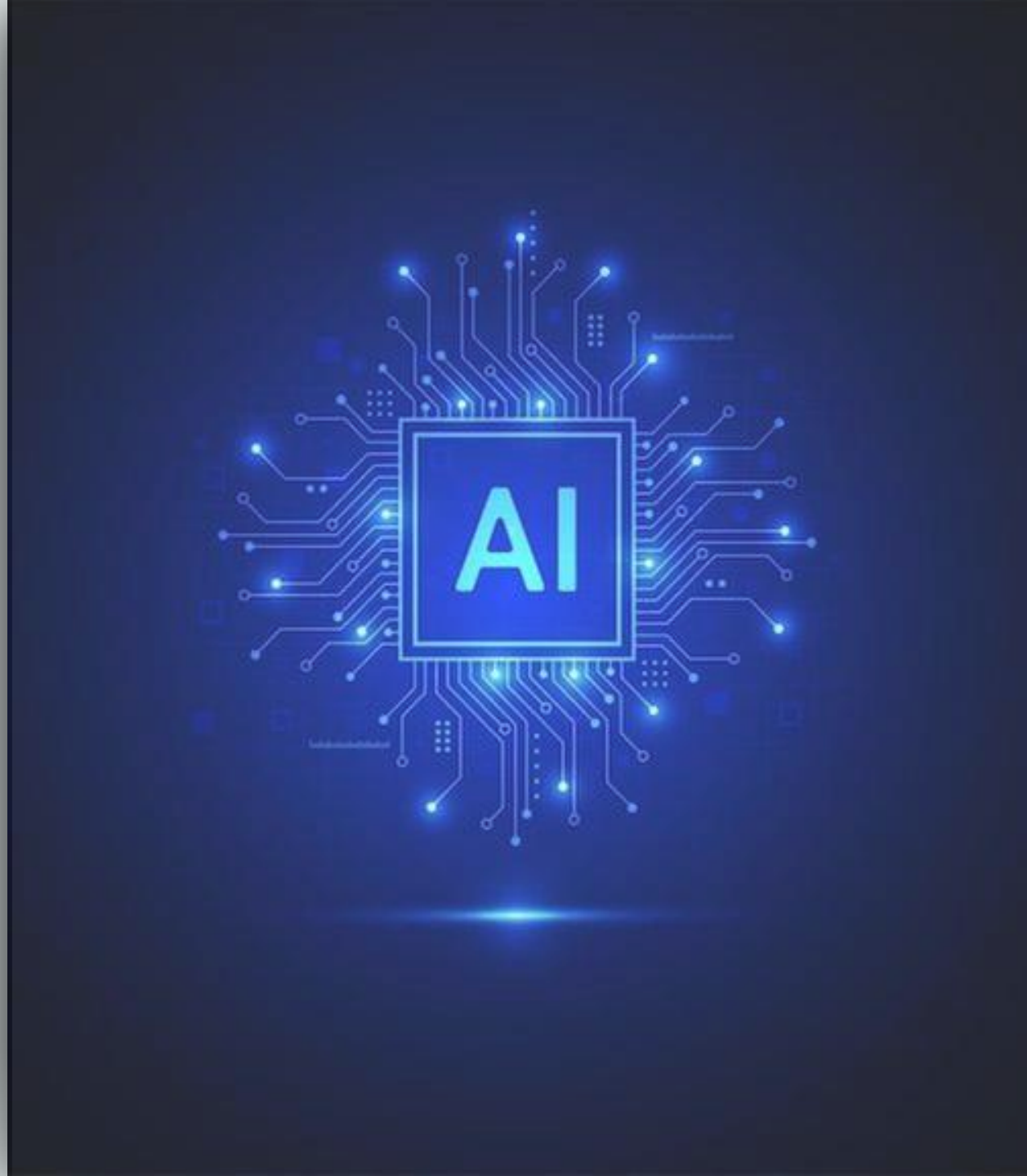
MAVEN SILICON

Centre of Excellence in Semicon

AI-powered Chip Design: *Spec to Silicon*

SIVAKUMAR P R
Founder and CEO
Maven Silicon



Maven Silicon

16+ Years Semicon COE

Wireless US Chipmaker Multiyear LS

(500+ Engineers per Year)

World's Largest OEM Mobility Solutions

(100+ Engineers per year)

World's Leading IP, EDA, Service Providers

(500+ Engineers per year)

5000+
VLSI Engineers Deployed

250+
Hiring Industry Partners

120+
Employees

BLOGS:

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VLSI Training Solutions

- ARM Cortex A V7/V8/V9
- ARM Cortex M V7/V8
- NEON
- Coherent Hub Interface (CHI)
- AMBA
- ARM SoC Design and Verification
- ARM Toolchain

- RISC-V ISA
- RISC-V Privileged Architecture
- RISC-V Debug System
- RISC-V Tool Chain
- RISC-V Processor IP Design & Verification
- RISC-V SoC Design and Verification

NEW COLLEGE GRADS VLSI PROGRAMS

- Digital Design - DD
- Design Verification - DV
- Design for Testability - DFT
- Physical Design & Verification – PD
- Embedded System Design - ESD
- Analog Design & AMS Verification

ADVANCED VLSI PROGRAMS

- Designing Verification IPs using UVM
- Low Power Design and Verification
- SoC Design and Verification
- Advanced ASIC & FPGA Verification Methodologies
- Formal Verification
- Physical Design and Verification - ICC2/Fusion Compiler & Calibre
- Design For Testing - Tessent/TestMax
- SystemVerilog for RTL Design
- RTL Linting and Synthesis
- Equivalence Checking, STA & GLS
- FPGA Architecture and SoC Design using FPGA
- RTL Design using Verilog/VHDL
- RTL Verification using SystemVerilog and UVM

PROTOCOLS

SoC Interface Protocols

USB, PCIe, DDR/LPDDR, Ethernet, Wireless, IoT, BLE

BUSINESS MODELS

- Multi-year online Learning Subscriptions
- Refresher and Bootcamp Courses
- Specialized Project Specific Courses
- NCG - Pre-onboarding Programs

INDUSTRY PARTNERS

CLIENTELE

DELIVERY MODES

VILT(Blended)

ILT(Offline)

Self-paced(Online)

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Executive M.Tech VLSI

For professionals with ***2+ years of Experience***

Powered by RISC-V®

PES UNIVERSITY | MAVEN SILICON Centre of Excellence in Semicon

Course with Multi-Exit Options

- Advanced Computer Architecture – RISC-V ISA
- System-on-a-Chip Design – RISC-V SoC
- Analog Mixed Signal Design
- AI Chip Design – RISC-V Accelerator
- ASIC Verification with SystemVerilog – RISC-V CPU
- Design For Testing (DFT) – RISC-V SoC
- Next Generation IC Manufacturing, Packaging & Testing
- UVM for Digital and AMS Verification – RISC-V SoC
- Physical Design & Verification – RISC-V SoC
- Formal Verification – RISC-V CPU
- Power Aware Design and Verification
- Embedded Systems - Chip Programming
- Machine Learning for EDA
- Design Automation using Python
- Gen AI for VLSI
- IC Project Management

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Executive Certification Courses

In Collaboration with **iHUB DivyaSampark**
IIT Roorkee

For graduates and professionals aiming to
advance their careers in VLSI.

Courses

- **Executive Certification in ASIC Verification**
- **Executive PG Certification in VLSI SoC Design and Verification**
- **Executive Certification in RISC-V IP Verification**
- **Executive Certification in RISC-V IP Design**
- **Executive Certification in VLSI Physical Design and Signoff**
- **Executive Certification in VLSI Design for Testing**

Key Highlights

- **750+ Hrs of total Learning**
- **5 Days Campus Immersion at IIT Roorkee**
- **Master Classes from IIT Faculty and Industry Experts**
- **Hands-On with on Real-World Projects**
- **Upto Rs 50L startup incubation support***
- **iHub DivyaSampark - IIT Roorkee Certification**

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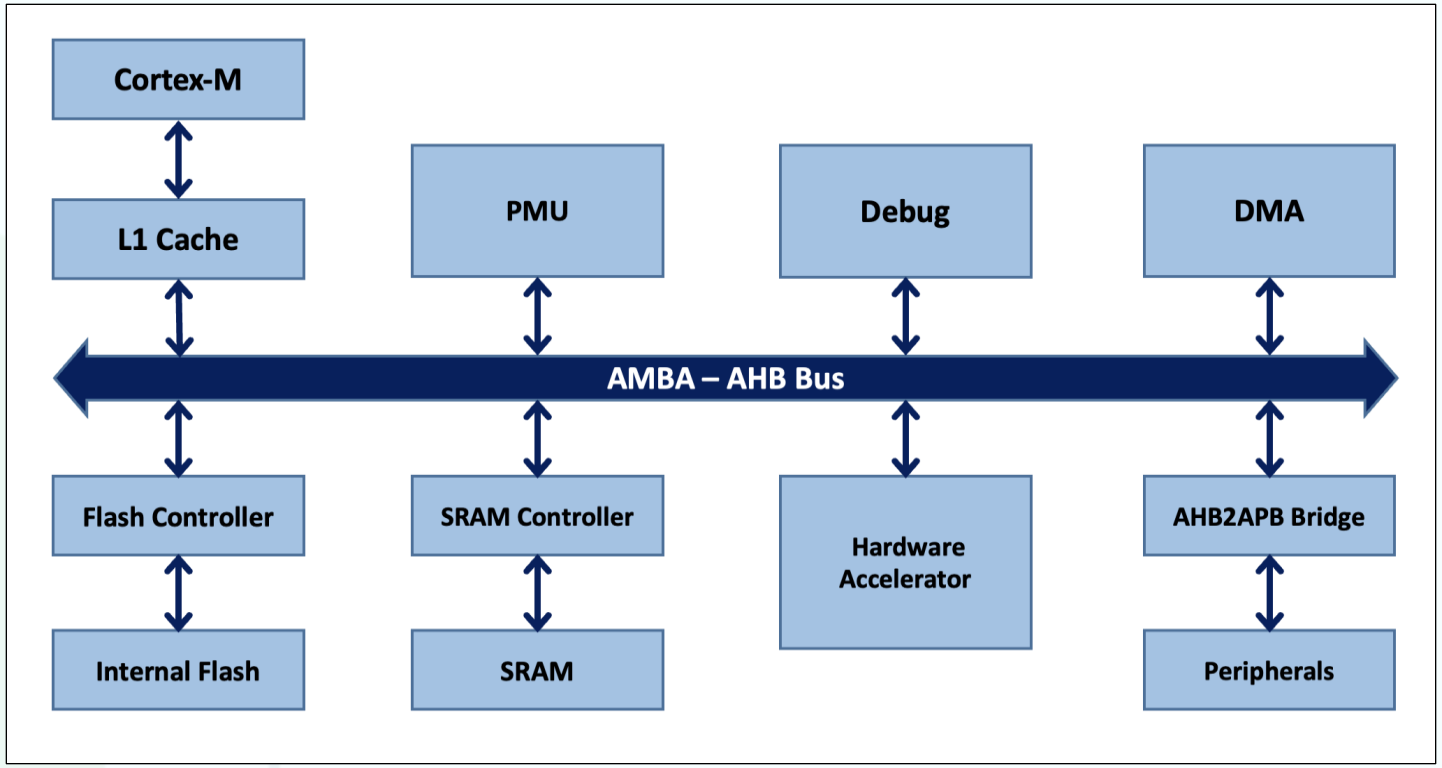
Agenda

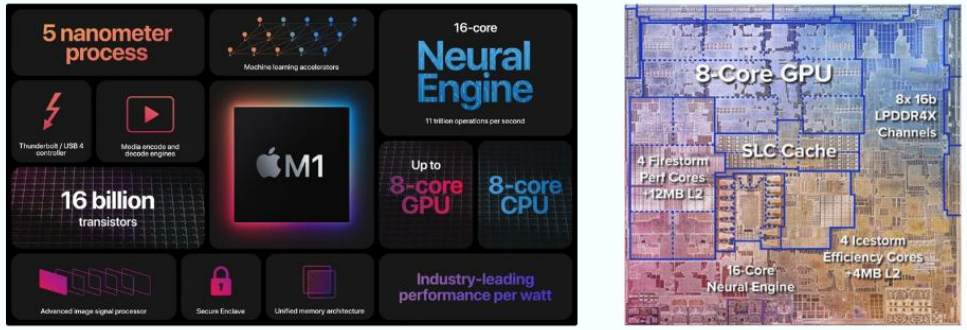
- Microcontrollers Vs SoCs
- AI-driven Semiconductor Industry
- AI-powered Chip Design
- AI Accelerators

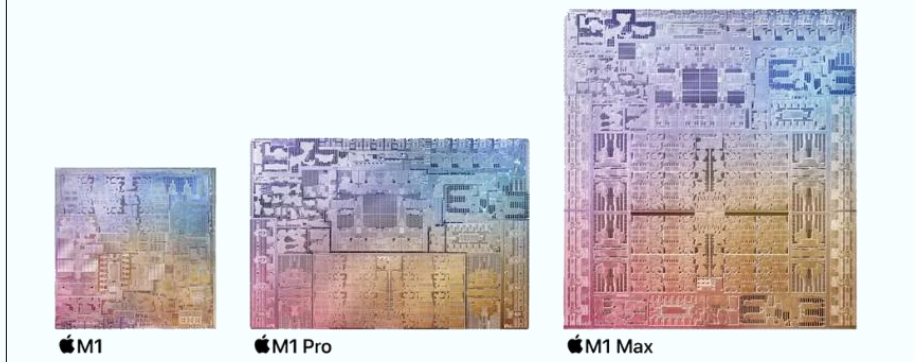
Embedded MCUs

- Specialized computer designed for a specific application
- Designed for a larger market — Low-cost high-volume chips
- Bare metal software application - With/without OS/real-time kernel
- **Examples:** ABS on cars, Coffee machines, Sports watches, etc

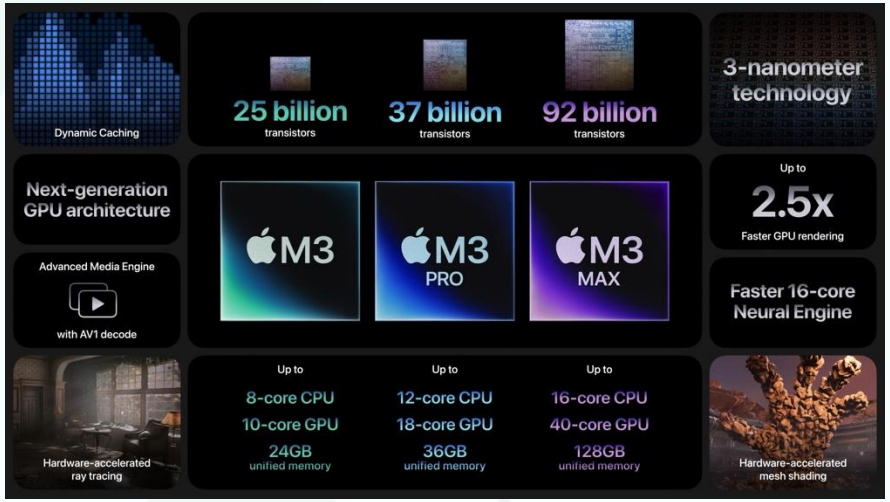


Apple's MacBook SoCs





Source: Anand Tech

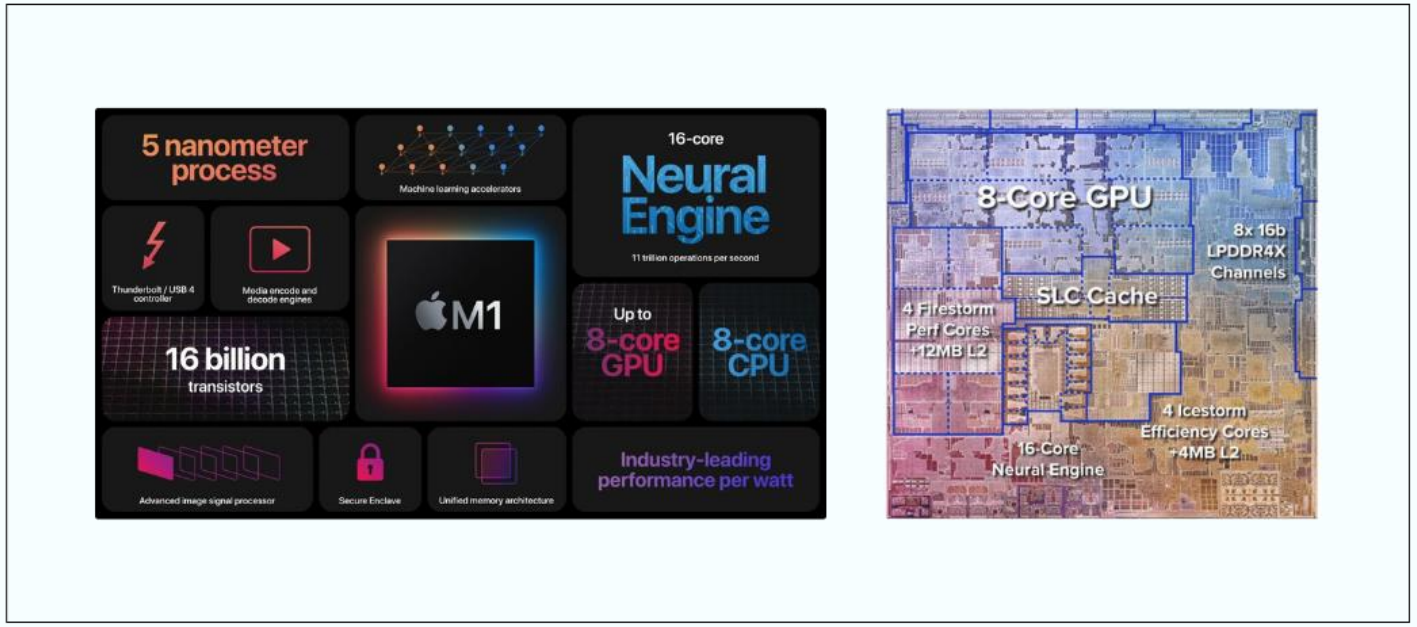


Apple Silicon M3 SoCs			
SoC	**M3 Max**	**M3 Pro**	**M3**
CPU: Performance	12-Core	6-Core	4-Core
CPU: Efficiency	4-Core	6-Core	4-Core
GPU	40-Core	18-Core	10-Core
Display Controller	5 Displays (1 Internal + 4 External)	3 Displays (1 Internal + 2 External)	2 Displays (1 Internal + 1 External)
Neural Engine	16-Core 18 TOPS (FP16)		
Memory Controller	LPDDR5-6400 32x 16-bit CH (512-bit) 400GB/sec Total Bandwidth (Unified)	LPDDR5-6400 12x 16-bit CH (192-bit) 150GB/sec Total Bandwidth (Unified)	LPDDR5-6400 8x 16-bit CH (128-bit) 100GB/sec Total Bandwidth (Unified)
Memory Capacity	128GB	36GB	24GB
Encode/ Decode	8K H.264, H.265, ProRes, ProRes RAW, AV1 (Decode)		
USB	USB4/Thunderbolt 4 6x Ports?	USB4/Thunderbolt 4 4x Ports?	USB4/Thunderbolt 4 2x Ports
Transistors	92 Billion	37 Billion	25 Billion
Mfc. Process	TSMC N3B		

SoC with many different ISAs

- RISC CPUs
- GPUs
- ML accelerators
- Application processors
- Image processors
- Radio DSPs
- Audio DSPs
- Security and Neural engines
- Power Management processor

- Based on various general purpose and specialized ISAs
- Each ISA with unique software stack



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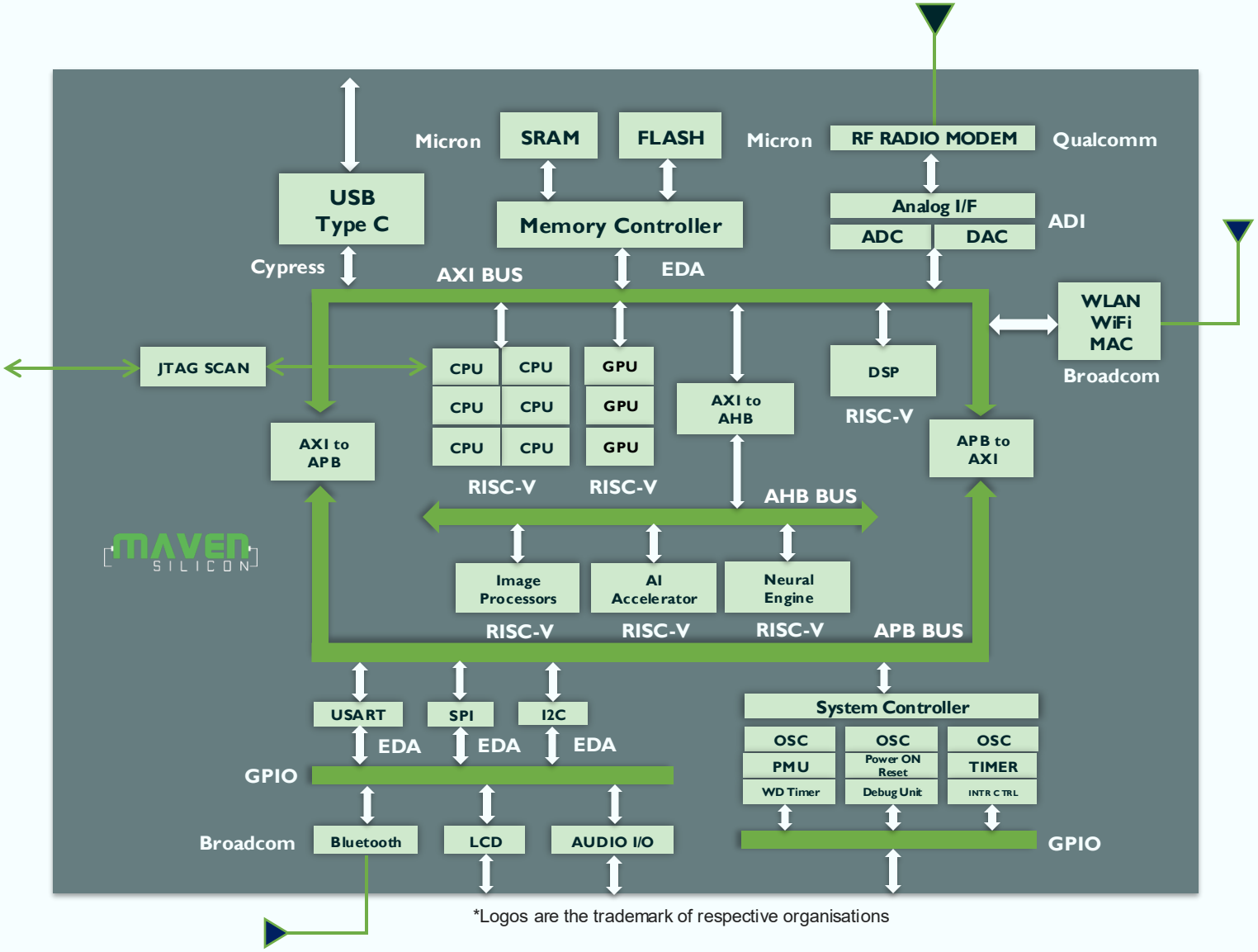
Source: Anand Tech

Why RISC-V?

- **Risk without RISC**
- **General Purpose ISAs last for decades:**
  - IBM 360 – 56+ years
  - Intel X86 – 42+ years
  - ARM – 35 years
  - RISC V – 10 Years
- **Special-Purpose ISAs rarely last for Decades:**
  - Network Processors
  - Image Processors
  - DSPs
  - GPUs
  - AI accelerators

RISC-V will emerge as an Industry Standard ISA for all computing Devices



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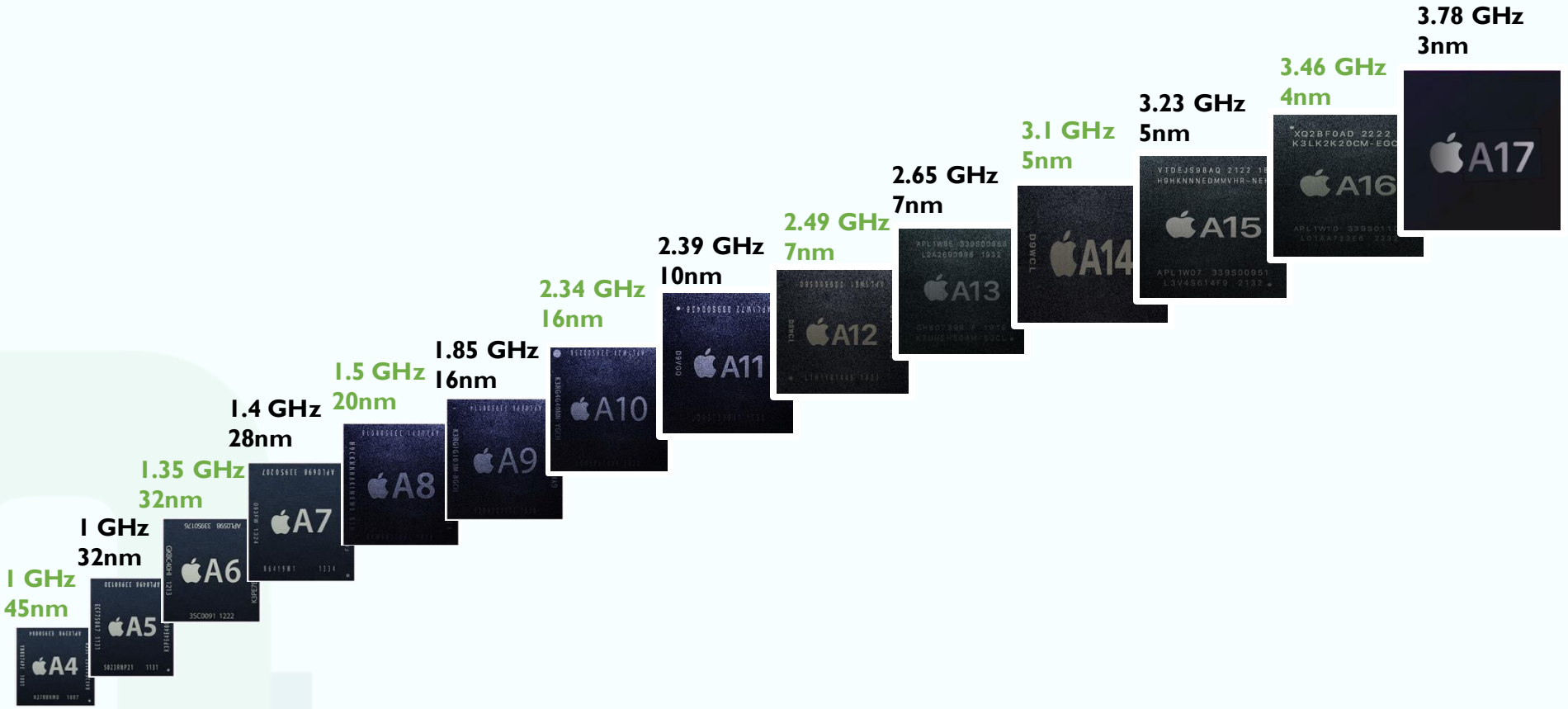
iPhone Chip



iPhone16 Motherboard

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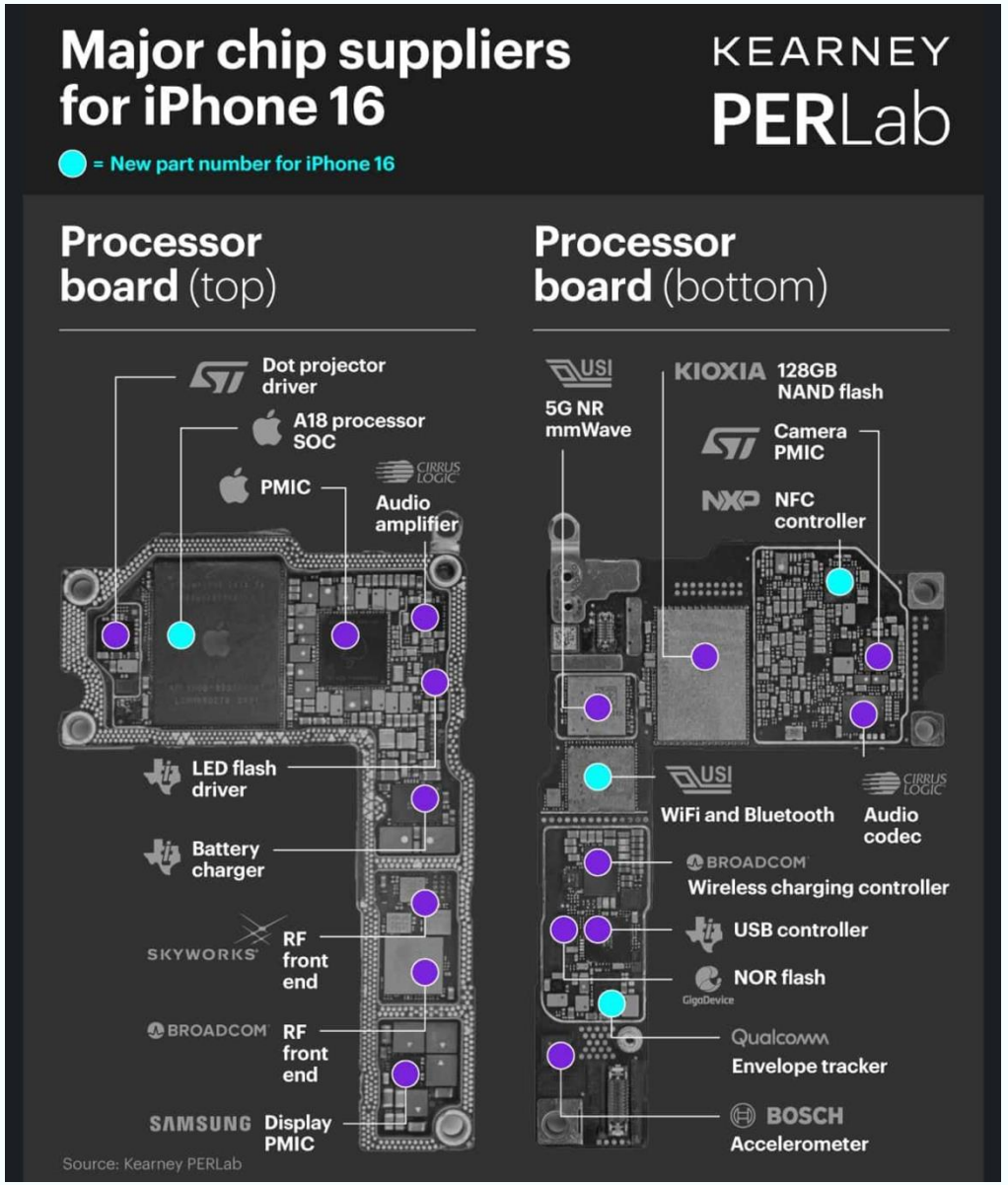
Technology	Usage
3nm to 7nm (leading edge nodes)	Smartphones, AI, data centres, graphic processing units (GPUs), high performance computing (HPC); automotive advance driver assistance systems ADAS, defense and mission critical hardware, supersonics
16nm to 28nm (advanced nodes)	Mid-range smartphones, laptops and tablets, HPC, IoT devices, sensors, EVs, automotive, consumer electron-
40nm, 65nm & 90 nm	Automotive, computing, data storage, wireless communication, power management, set top box, smart home, smart grid, medtronics, industrial CPUs
180nm, 250nm & beyond (older nodes)	Industrial controls, older telecom equipment
Analog chips	Communications inside phones, consumer electronics, industrial, analog to digital convertor, telecom towers

Source: Fab Economics, Fortune India Research



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Apple A18 Series

General information	
Launched	September 9, 2024
Designed by	Apple Inc.
Common manufacturer	TSMC
Max. CPU clock rate	to 4.04[1] GHz
Cache	
L2 cache	A18: 8 MB (performance cores) A18 Pro: 16 MB (performance cores) 4 MB (efficiency cores)
Last level cache	A18: 12 MB (system level cache) A18 Pro: 24 MB (system level cache)
Architecture and classification	
Application	Mobile **A18** [show] **A18 Pro** [show]
Technology node	3 nm (TSMC N3E)
Instruction set	ARMv9.2-A[2]
Physical specifications	
Cores	6 cores (2 performance + 4 efficiency)
Memory (RAM)	8 GB[3][4]
GPUs	A18: 5-core A18 Pro: 6-core
Co-processor	NPU: 35 TOPS

Semicon Supply Chain

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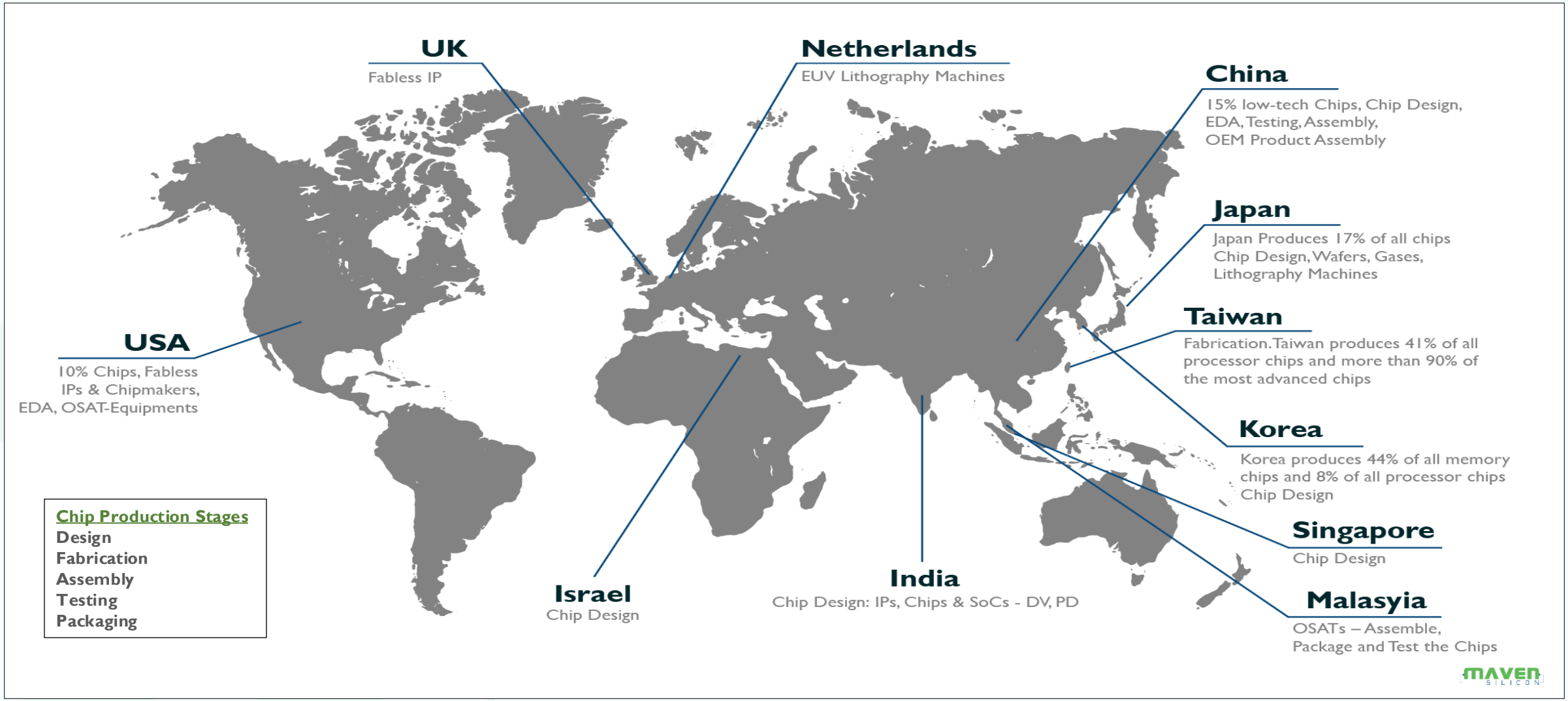
Global network of companies that annually produces trillions of chips at nm scale



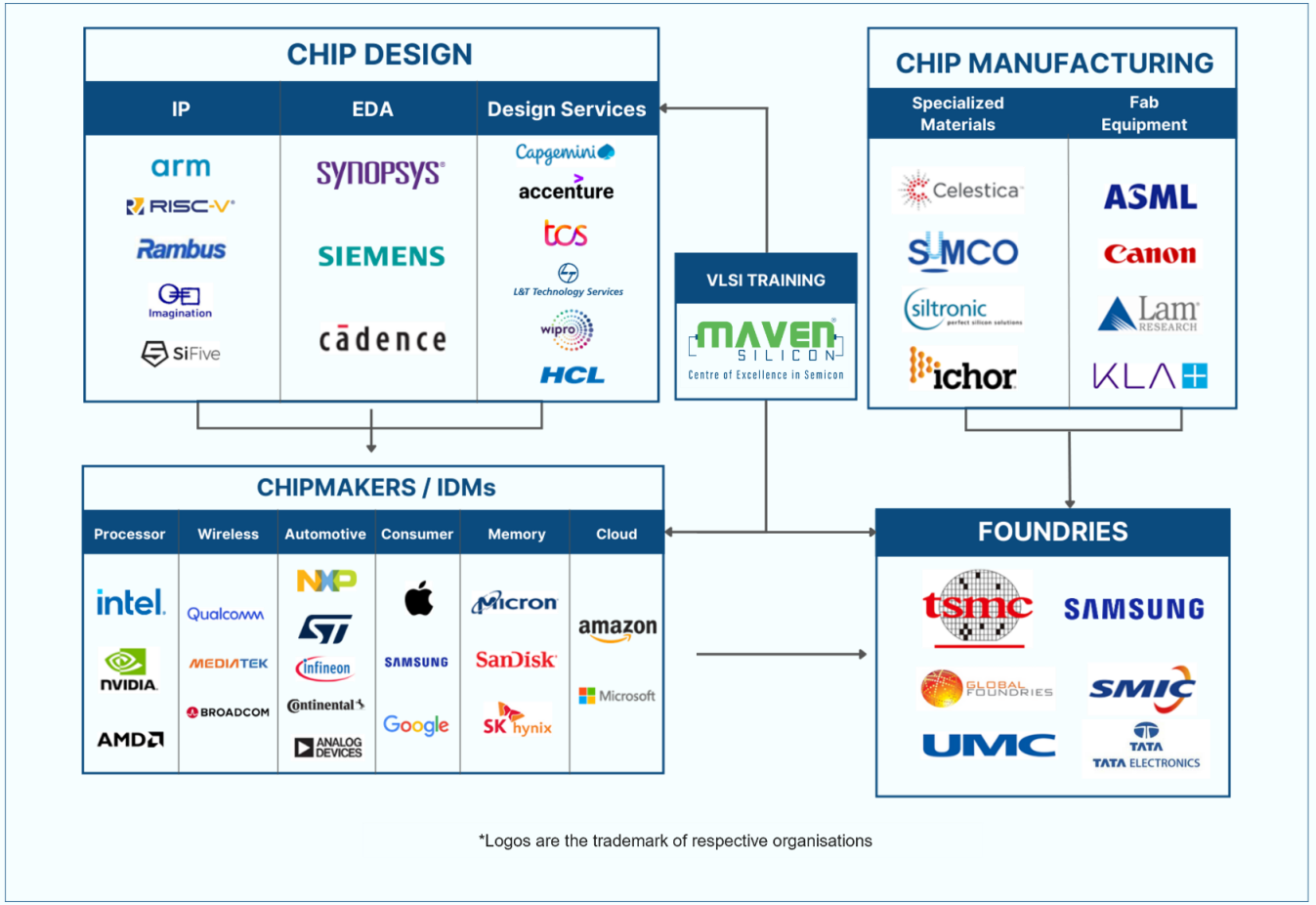
Ref: Chip War, Chris Miller

Taiwan: TSMC builds almost all the world's most advanced processor chips

Indian Semiconductor Ecosystem

- **Design Services:** Pre-silicon Design, Verification, Implementation, Silicon Testing,Validation, Chip Programming.
- **Chip Design:** L&T Semiconductor Technologies – A fabless chip design company. **Investment: INR 830 Crore**
- **Fabrication:** Tata Electronics and Taiwan's Powerchip Semiconductor Manufacturing Corp – Setting up a Foundry.
  Investment: INR 91000 Crore
- **Assembly & Testing:** US chipmaker Micron – Setting up an ATMP facility in Gujarat. **Investment: $2.75 Billion**
- **Testing & Packaging:** Tata is setting up a testing and packaging unit in Assam. **Investment: INR 27000 Crore**
- **OSATS:** CG Power – Renesas JV. **Investment: 7600 Crore**
  Many others: HCL, Hiranandani Group
- **Need more Players/Investments: for:** Wafer Level Micro Bumping, Surface Mount Technology, Component Level Assembly

Ref: Fortune India



Indian Semiconductor Manufacturing Projects

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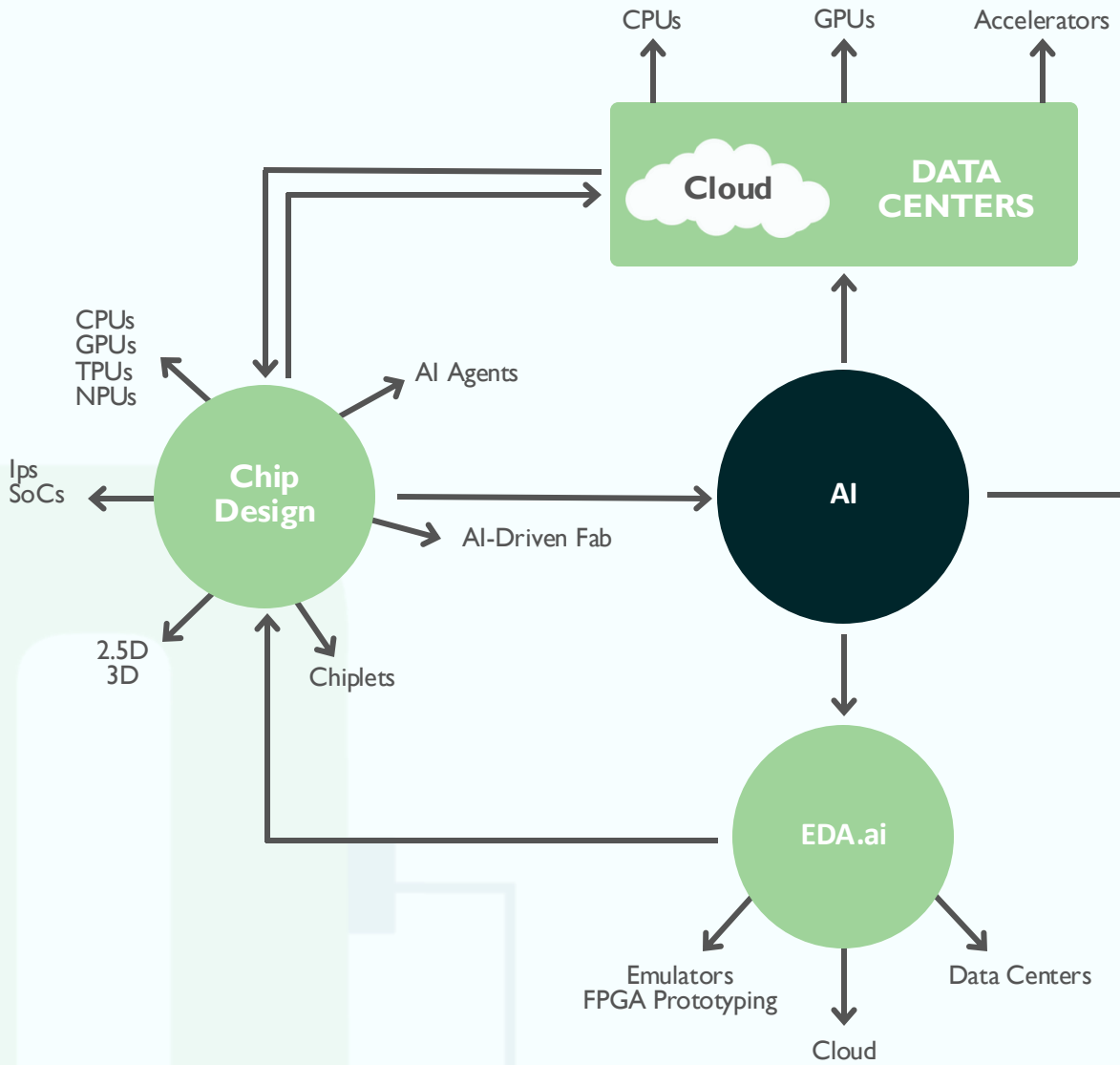
In India, the semiconductor market is expected to hit $110 billion by 2030, from $22 billion in 2019, as per a report by IESA and Counterpoint Research.

What	Under	Where	Who	Start	How Much (in ₹)
Fab	India Semiconductor Mission	Dholera, Gujarat	Tata Electronics, PSMC	29 February 2024	910B
OSAT Unit	India Semiconductor Mission	Morigaon, Assam	Tata Semiconductor Assembly & Test	29 February 2024	270B
OSAT Unit	India Semiconductor Mission	Sanand, Gujarat	CG Power, Renesas Electronics (Japan) Stars Microelectronics (Thailand)	29 February 2024	76B
ATMP Unit	India Semiconductor Mission	Sanand, Gujarat	Micron Technology	June 2023	225.16B
ATMP Unit	India Semiconductor Mission	Sanand, Gujarat	Kaynes Semicon	2 September 2024	33B
Fab	MH gov, ISM (Pending)	Taloja, Panvel, Maharashtra	Tower Semiconductor (Israel), Adani Group	5 September 2024	839.47B
OSAT Facility	MH gov, Sachin Tendulkur	Navi Mumbai, Maharashtra	RRP Electronics, HMT Microelectronic AG	September 2024	365.73B
OSAT Facility	GJ gov, ISM (Pending)	Surat, Gujarat	Suchi Semicon	Opened in Dec 2024	$100M

Source: Electronics For You

AI-Driven Semicon Industry



SMART WORLD
- Smart Retail
- Intelligent Factory
- Smart City
- Digital Home

TRANSPORTATION
- ADAS
- Autonomous Vehicles

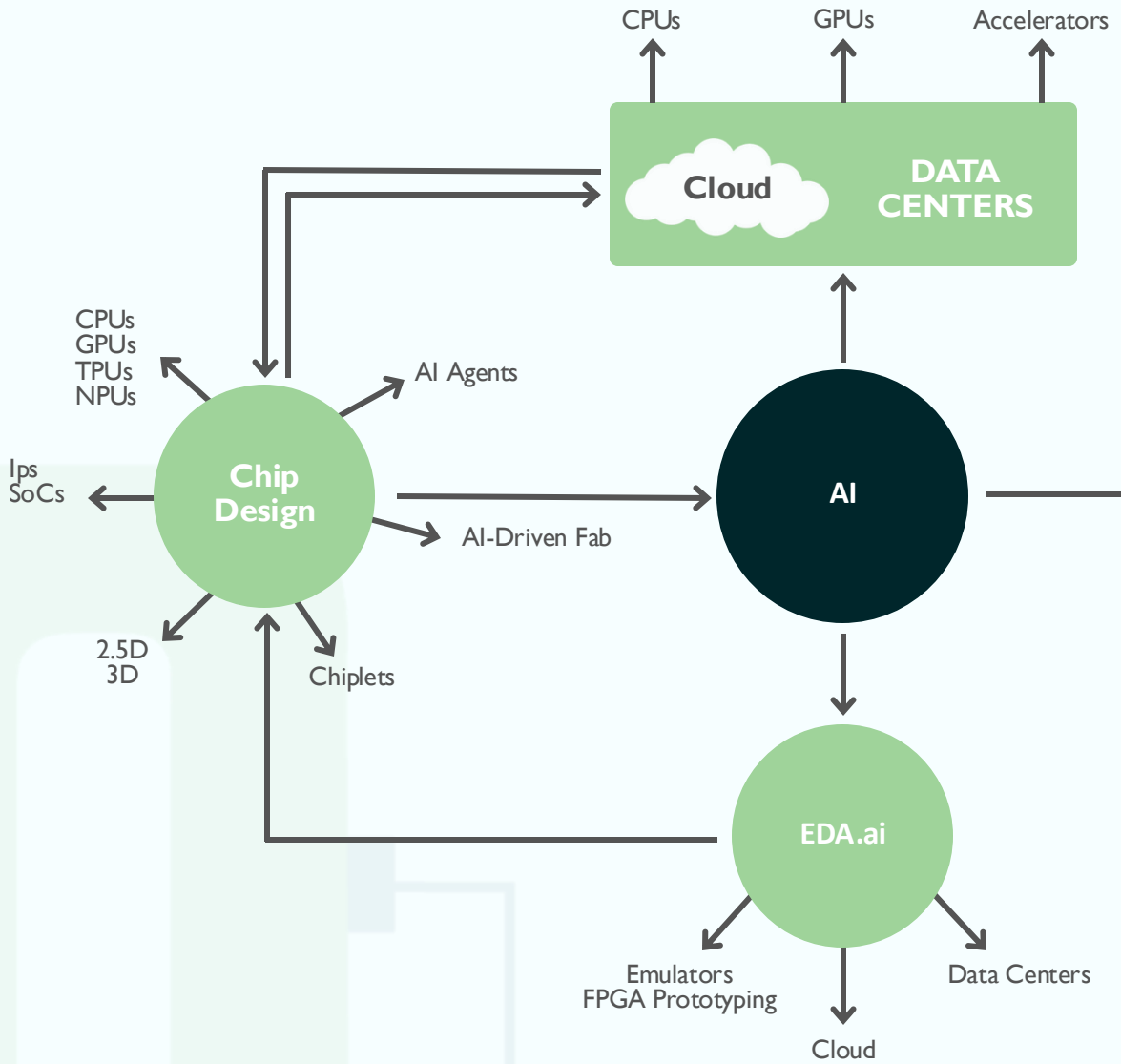
EDUCATION

CLOUD DATA CENTER
- AI-powered Cloud - RM

COMMERCIAL & ENTERPRISE
- Server, PC, Smartphone Edge AI

HEALTHCARE
- Diagnosis
- Surgical Robotics

AI-Powered Chip Design



Chip Design
- Code Review
- RTL Linting
- AI Agents
- Co-pilots

Chip Verification
- Testcase generators
- Coverage Closure
- SV/UVM TB code reviews

EDA
- EDA Vs Design Services
- ML in EDA
- Improved Performance
- Co-pilots for EDA/IP UGs

Chip Implementation

Chip Fabrication

Silicon Testing

PCB Testing

AI For Chip Design

- **AI helps junior engineers do their projects as experienced engineers:**
  - LLMs trained by experts can assist juniors who can do their job as their seniors.
  - RTL linting: Trained LLMs can accept/reject warnings and update the source code.
  - Juniors can use co-pilots for their code review.
  - TB Code Optimization: LLMs trained with SV/UVM coding/performance guidelines can update/optimize the TB source code

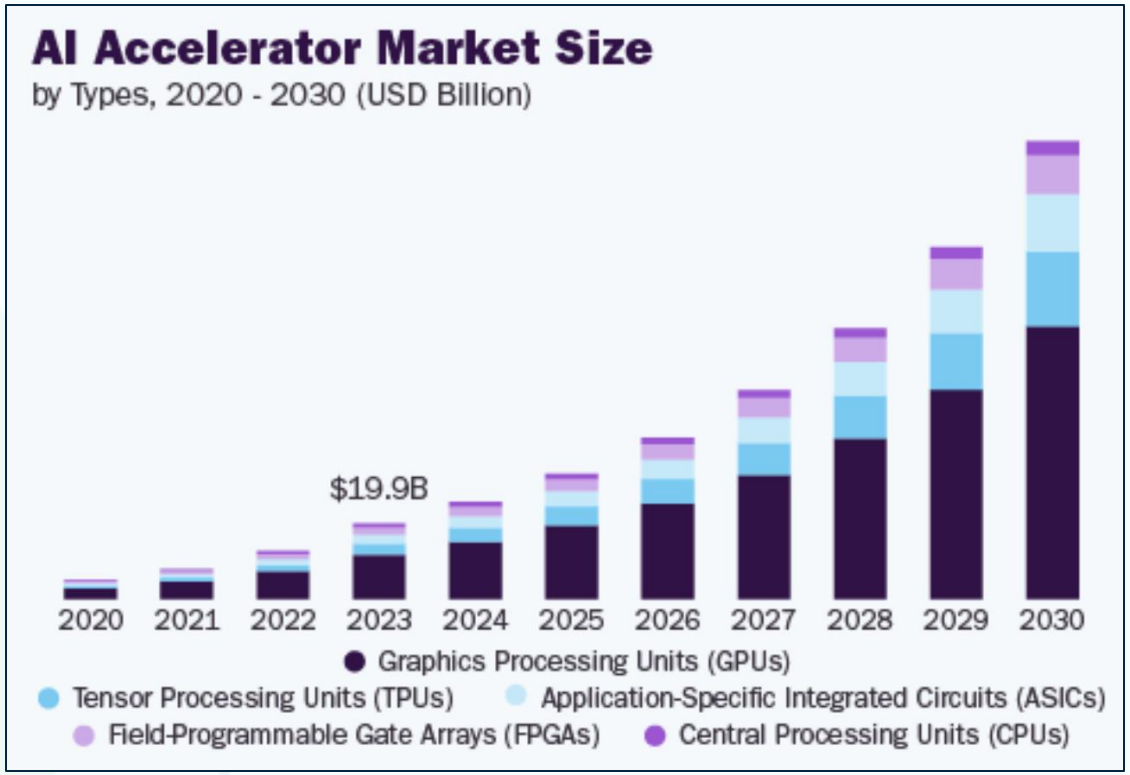
- **AI improves the productivity:**
  - Doing more[2X] with the same team - **EDA Vs Design Services**
  - ML in EDA automates more and improves the quality:
    Verification Sign-Off: Automated coverage closure, Implementation: PPA Optimization.
  - **Agentic AI** - Agent approach for chip design by chipmakers:
    Chipmakers' IPs/Chips to train their agents: Specs, Coding Guidelines, Test Generation, Layouts, PCBs.

AI For Chip Design

- **AI helps engineers own and do multiple things as Generalist:**
  - RTL to Synthesis
  - DV Engineers with domain expertise will do RTL and DV as well.
  - AI will offer: Co-pilots, Code Generators for IPs and TBs, Automated coverage closure, Verification and Synthesis sign-off
- **AI Co-pilots for EDA/IPs:**
  - Easier than referring to UGs/TRMs.
- **Full Chip Implementation:**
  - Automating the PD flow requires training LLMs extensively on customer projects.
  - Ambitious but unrealistic. Training LLMs : Challenges – IP Rights, Design Data, and Security

AI Accelerators - Market

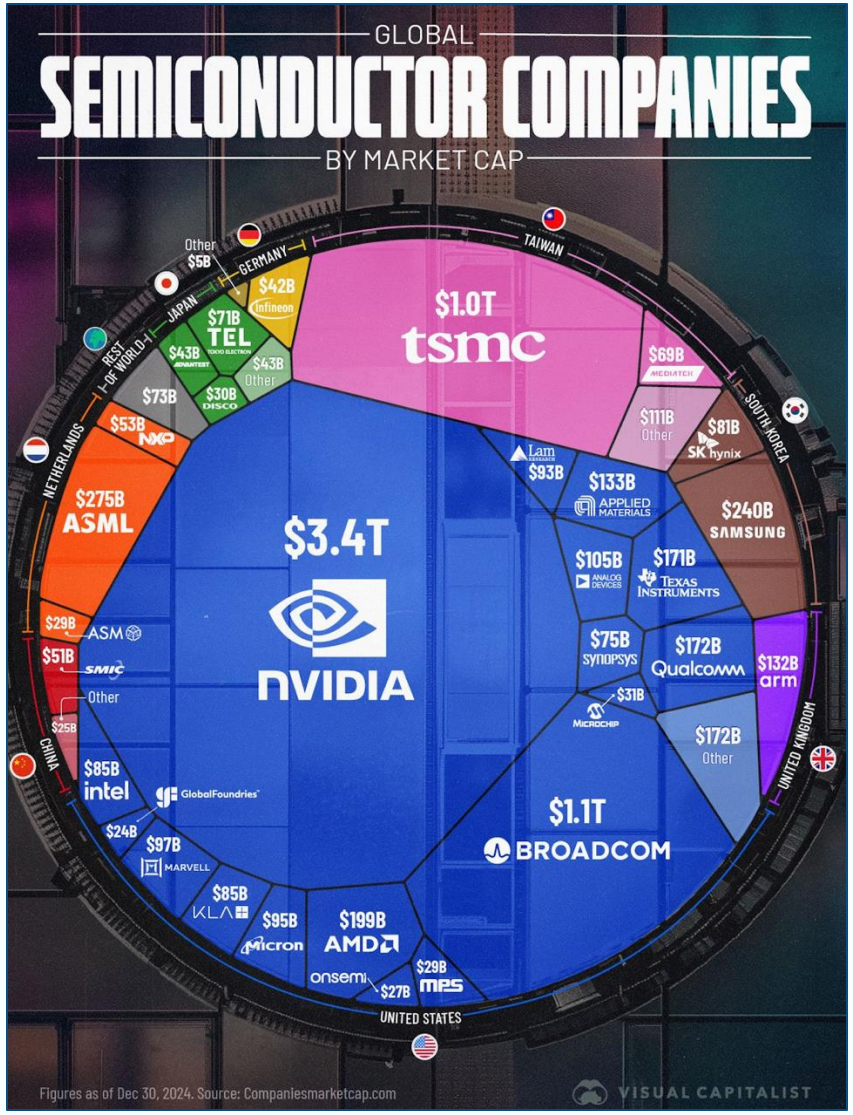
- The global AI accelerator market size was estimated at USD 19.89 billion in 2023 and is projected to grow at a CAGR of 29.4% from 2024 to 2030.
- NVIDIA Corporation, Google, and Intel are leading the AI accelerators market with their next-gen accelerators.



Source: Grand View Research

Global Semiconductor Industry

- **A Trillion-Dollar Industry by 2030**
- **2023 Revenue : $526.8 Billion**
  - ✓ Logic Chips: $178.5 Billion
  - ✓ Memory Chips: $92.3 Billion
  - ✓ MCUs: $27.9 Billion
  - ✓ Automotive Chips: $42.2 Billion
- **2024 Revenue: $621 Billion**
  - ✓ 19% YoY in 2024 ↑
  - ✓ Logic chips 11% ↑
  - ✓ Memory Chips 64% ↑
- **70% Growth from three industries:**
  - ✓ Automotive,
  - ✓ Enterprise Compute, Networking & Data Storage
  - ✓ AI, IoT/Wireless



AI Accelerators - Future

- **Future of AI Accelerators: Major players NVIDIA, AMD, Intel, Google, Amazon, and more unveiling their upcoming AI accelerators.**

  - With the growing demand for AI and LLMs, companies are racing to deliver high-performance AI accelerators with advanced HBM (High Bandwidth Memory) configurations.

  - **NVIDIA Dominance:** NVIDIA continues to lead with a robust roadmap, extending from H100 to future Rubin and Rubin Ultra chips with HBM4 memory by 2026-2027.
  - **AMD's Competitive Push:** AMD's MI300 series is already competing, with MI350 and future MI400 models on the horizon.
  - **Intel's AI Ambitions:** Gaudi accelerators are growing, with Falcon Shores on track for a major memory upgrade.
  - **Google & Amazon's Custom Chips:** Google's TPU lineup expands rapidly, while Amazon's Trainium & Inferentia gain traction.
  - **Microsoft & Meta's AI Expansion:** Both companies are pushing their AI chip strategies with Maia and MTIA projects, respectively.
  - **Broadcom & ByteDance Join the Race:** New challengers are emerging, signaling increased competition in AI hardware.

Ref: :LinkedIn, X

Next-Gen Chip Designers

- **AI will not replace Subject Matter Experts**
- AI will handle repetitive tasks, freeing up human time for creative work and strategic thinking
- Understand Electronic Systems – Embedded Systems, Smartphones, Desktops, Cloud Servers
- System Level Design expertise – AI Accelerators, SoCs, Chiplets, 3D IC Packaging

Entrepreneurs:

- Think beyond design/software services : EDA → Fabless-IP → Chipmaker → Product/OEMs
- **IPs/Chips : EVs, Healthcare, AI**
- Innovation: Products for domestic needs – Defence, Space, and Consumer Applications

VLSI.ai

'Let's design AI chips and let AI implement its AI Chips' - Siva

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THANK YOU!