2016 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

CONFERENCE PROGRAM

HOLIDAY INN MUNICH CITY CENTRE

OCTOBER 19-20, 2016 | DVCON-EUROPE.ORG

WELCOME TO DVCON EUROPE 2016

OLIVER BELL

General Chair - *Intel*

Yes, DVCon Europe has indeed been established now. I'm pleased to welcome you to the 2016 edition of the **Design and Verification Conference & Exhibition Europe!**

Since its launch in 2014, we have seen in the past two years nice growth in attendance, packed tutorial rooms, a variety of technical presentations, exciting keynotes and panels and a good mixture of companies at the exhibition floor: DVCon Europe is a practical, industry application-oriented conference, focusing on design and verification of electronic systems and integrated circuits. This conference is made by Engineers for Engineers. We work year round at DVCon Europe to bring you the best program and conference experience. I'm grateful for the countless hours spent by the Board, the Technical Review teams and all the great team members "behind the scenes" to make DVCon Europe happen.

DVCon Europe brings the engineering community together to share experiences and to present the practical use of Electronic Design Automation standards, languages and methodologies for design and verification. The European emphasis on mixed-signal, functional-safety and system-level design and variation are well reflected in the 2016 DVCon Europe program. The program offers valuable technical content on a broad range of current Design and Verification topics, including SystemC methodology evolution, UVM, Portable stimulus, Formal, Analog mixed signal, low power, Functional safety and high reliability development, and many more.

Automotive design and verification continues to be a strong topic for Europe, therefore a plenary panel session has been added to the program to discuss the requirements and needs for functional security in the automotive value chain. For the first time this year we even enjoy two keynotes: The opening keynote on Wednesday from Mr. Hobson Bullman will focus on practical design and verification methodologies, and the keynote on Thursday from Mr. Juergen Weyer will give you further ideas and insights into the Securely Connected, Self-Driving Car. Both keynotes well reflect the growing importance of embedded software.

DVCon Europe starts traditionally with a rich tutorial program on Wednesday with 16 tutorials, given by user-companies, standardization teams, training institutes, consultancy companies, or EDA tool providers. I'm personally also looking forward to the Wednesday evening gala dinner, with a presentation from Lucio Lanza. The diner is one of many nice networking opportunities during DVCon Europe.

The technical program on Thursday hosts 30 informative, high-quality papers, reflecting today's industry practices in design and verification. We also introduce this year the so-called "lightning talks": The idea behind them is to give a fast overview for selected topics with an emphasis on direct interaction and follow-up with the speakers. Also new this year are Thursday's Special Interest Tracks with a focus on SystemC Evolution, following up from the initial "Accellera SystemC Evolution Day" in May this year. Alongside dedicated in-depth sessions on SystemC and UVM, the technical program contains papers on subjects from system level down to the gate level verification. DVCon Europe also offers this year a great mix of application and verification experience, with good technical discussions among the DVcommunity. You are invited to vote on the best paper and poster, which will be announced at the closure of the conference.

The exhibition at DVCon Europe is an integral part of the conference and we welcome all the new exhibitors this year presenting their EDA tools, services and solutions. Please have a look and interact both days with the exhibitors – maybe you will find the solution for your current design or verification problem!

With all these tutorials, technical program and exhibition, DVCon Europe is a fantastic opportunity for you to network, learn and grow. The DVCon Europe Steering Committee and the Accellera Systems Initiative welcome you to the conference. Enjoy DVCon Europe!

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CONFERENCE SPONSOR

Accellera Systems Initiative, the proud sponsor of DVCon Europe 2016, is an independent organization with the mission to provide design and verification standards required by systems, semiconductor, IP and design tool companies to enhance a front-end design automation process. We collaborate with our community of companies, individuals and organizations in delivering the standards that lower the cost to design commercial EDA, IC and embedded system solutions. As a result of its partnership with the IEEE, Accellera standards are transferred to the IEEE Standards Association for formalization and ongoing change control.

Accellera Systems Initiative: A New Synergy for Standards

System, software, and semiconductor design are converging to meet the increasing challenges to create complex integrated circuits and system on chips. This convergence has brought to the forefront the need for a single organization to facilitate the creation of system-level, semiconductor design, and verification standards. Leading industry standards associations Accellera Organization Inc. and the Open SystemC Initiative (OSCI) merged in 2011 to form a single organization, Accellera Systems Initiative, to address the needs of the system and semiconductor designers who must find new and smarter ways to create and produce increasingly complex chips. The new organization will evolve to create more comprehensive standards that benefit the global electronic design community.

Membership

Accellera members directly influence development of the most important and widely used standards in electronic design. Member companies protect and leverage their investment in design languages through their funding of a proven, effective and responsible organization. In addition, our members have a higher level of visibility in the EDA industry as active participants in Accellera-sponsored activities and as contributors to its decisions, which impact the EDA industry. For a full list of technical activities that are supported by Accellera, and for information on how to join us, please visit our website at www.accellera.org.

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CONFERENCE DETAILS

REGISTRATION HOURS

Location: Foyer GroBer Saal

Wednesday, October 19 ------ 7:30am - 7:30pm
Thursday, October 20 --------- 7:30am - 6:00pm

Thank You to Our Sponsor:

DVCON EUROPE 2016 EXPO

Location: GroBer Saal

Wednesday, October 19 ------ 5:30 - 7:30pm
Thursday, October 20 --------- 12:00 - 6:00pm

TUTORIALS & PROCEEDINGS DISTRIBUTION

DVCon Conference Papers and Tutorial presenter slides will be delivered electronically online via a username and password.

To access: http://proceedings.dvcon-europe.org
Username and password will be provided to registered conference attendees

ATTENDEE COFFEE BREAKS

Wednesday, October 19

7:30 - 8:30am
9:30 - 10:00am
3:30 - 4:00pm

Thank You to Our Sponsor:

Thursday, October 20

7:30 - 8:30am
10:30 - 10:45am
2:45 - 3:15pm

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Follow @DVConEurope on Twitter and tweet #DVConEurope about your experience and highlights at the conference!
Don't miss DVCon on Facebook at https://www.facebook.com/DVCon-Europe-898352006944641/.

BEST PAPER VOTING

The 2016 DVCon Europe Best Paper award will be determined based on conference attendee feedback. To vote for your favorite paper, be sure to collect a voting form from the registration desk. Forms must be returned to the registration desk immediately following the last session of the day on Thursday, so that responses can be tallied. Be sure to submit yours and record your vote!

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AWARDS PRESENTATION

Join us on Thursday, October 20 at 5:30pm in the Exhibit Hall for the Closing Ceremony and announcement of the Best Paper Awards.

CONFERENCE FLOORPLAN

WEDNESDAY'S AGENDA

7:30 - 8:30am	Attendee Coffee Break *Room: Foyer* *Thank You to Our Sponsor:* SYNOPSYS®			
8:30 - 9:30am	Keynote: Design and Verification Focus in ARM TSG *Room: Forum 6 & 7*			
9:30 - 10:00am	Attendee Coffee Break *Room: Foyer* *Thank You to Our Sponsor:* SYNOPSYS®			
10:00 - 11:30am	Tutorial 1 - Advanced UVM Coding Techniques *Room: Forum 4* *Thank You to Our Sponsor:* ***Doulos***	Tutorial 2 - ISO26262 - This Changes Everything *Room: Forum 5* *Thank You to Our Sponsor:* ***Cadence Design Systems, Inc.***	Tutorial 3 - How Portable Stimulus Addresses Key Verification, Test Reuse, and Portability Challenges *Room: Forum 6*	Tutorial 4 - Formal Verification - Too Good To Miss *Room: Forum 7*
11:00am - 1:00pm	Tutorial 5 - Advanced UVM tips & tricks *Room: Forum 4*	Tutorial 6 - UVVM - A game changer for FPGA VHDL Verification *Room: Forum 5*	Tutorial 7 - Platform Level Design : IP-XACT and SoC Verification *Room: Forum 6* *Thank You to Our Sponsor:* ***Magillem Design Services***	Tutorial 8 - Simplified Assertion Abstraction to Code High-reliability Requirements for the Formal Verification of Safety Critical and Other Designs *Room: Forum 7* *Thank You to Our Sponsor:* ***OneSpin Solutions***
1:00 - 2:00pm	Luncheon *Room: Foyer*			
2:00 - 3:30pm	Tutorial 9 - An Industry Proven UVM Reuse Methodology for Coverage Driven Block Level Verification to Software Driven Chip Level Verification Across Simulation and Emulation *Room: Forum 4*	Tutorial 10 - Model Driven Approach to Software Driven Verification *Room: Forum 5*	Tutorial 11 - Shadow Simulation: A New Verification Methodology for Configurable Logic *Room: Forum 6* *Thank You to Our Sponsor:* ***Xilinx***	Tutorial 12 - Back to Basics: Doing Formal the Right Way *Room: Forum 7* *Thank You to Our Sponsor:* ***Mentor Graphics Corp.***
3:30 - 4:00pm	Attendee Coffee Break *Room: Foyer* *Thank You to Our Sponsor:* SYNOPSYS®			
4:00 - 5:30pm	Tutorial 13 - UVM-SystemC goes random - Introducing CRAVE in UVM-SystemC *Room: Forum 4*	Tutorial 14 - Applying UPF 3.0 for Early, System-level Power Analysis of SoCs with DDR Memories *Room: Forum 5* *Thank You to Our Sponsor:* ***Synopsys, Inc***	Tutorial 15 - Advancing the SystemC Ecosystem *Room: Forum 6*	Tutorial 16 - Designing Safe Cars - How to Ensure Your Semiconductor Design Meets ISO-26262 Fault-Safety Requirements *Room: Forum 7*
5:30 - 7:30pm	DVCon Europe Expo *Room: Exhibit Hall*			
7:30 - 9:30pm	Gala Dinner Presentation - Supporting the Exponential Growth in New Application Areas *Room: Ballsaal*			

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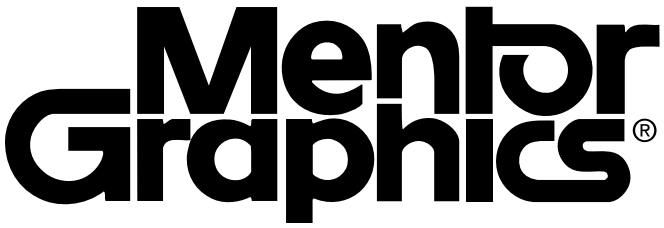

Keynote: Design and Verification Focus in ARM TSG

Time: 8:30am - 9:30am | Room: Forum 6 & 7

As the world leader in semiconductor IP, ARM supplies technology that's at the heart of billions of new devices manufactured every year. In order to make that possible, ARM has enabled an engineering infrastructure and workflow group to support the compute and tooling needs of ARM, called TSG (Technology Services Group), which enables and develops best practice and promotes effectiveness, understanding and continuous improvement. TSG tools and services are used by ARM engineers across all regions and functions, across software, process and system design, and physical implementation.

In this Keynote, Hobson will address some of the methodology and infrastructure challenges faced, and solutions delivered by TSG, for delivering IP into a demanding partner base, across a wide variety of markets.

Speaker:

Hobson Bullman - *ARM Ltd.*

Tutorial 1 - Advanced UVM Coding Techniques

Time: 10:00am - 11:30am | Room: Forum 4

Organizer:

John Aynsley - *Doulos*

This tutorial focuses on three aspects of UVM coding that can pose particular challenges to practitioners as they move beyond the beginner level because the techniques in question are not explicitly spelled out or explained in the standard UVM documentation. The three topics are run-time phasing, the sequencer, and random stability.

This tutorial is aimed at practitioners who already have a basic understanding of UVM and are looking to extend their knowledge.

Speaker:

John Aynsley - *Doulos*

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Tutorial 2 - ISO26262 - This Changes Everything

Time: 10:00am - 11:30am | Room: Forum 5

Organizer:

John Brennan - *Cadence Design Systems, Inc.*

ISO 26262 is an international standard for functional safety of electrical and/or electronic systems for production of automobiles, and is the first standard of its kind which will drive significant change in both EDA and silicon suppliers. Similar to it parent superset, IEC 61508, ISO 26262 is a risk-based safety standard – something EDA has not dealt with in the past. In simple terms, risk metrics are qualitatively assessed and safety measures are defined to avoid or control systematic failures, and to detect or control random hardware failures, or to mitigate their effects. This is metric driven verification (MDV) on steroids.

With ISO 26262 moving into the spotlight for automotive functional safety, Cadence has seen more questions and confusion than answers, and discussions are emerging around the application of the standard to actual silicon designs for automotive systems. We know based on actual adoption in production environments - this standard will have a significant impact on us in terms of tools, methodology, metrics, documentation, traceability, process and ecosystem communication. The good news is for most MDV environments, ISO 26262 is fairly manageable on the verification aspect. The bad news is that no matter how you cut it, this is more work and changes everything.

ISO 26262 Part 5 is focused on product development at the hardware level, and specifies the safety activities during the phase of the automotive hardware development. In this phase, hardware safety design is planned, implemented, integrated, and tested. To prove the safety integrity compliance in the hardware development process, quantitative evaluations on the hardware are required. These quantitative evaluations are new functional and safety metrics which need to be both statistical and measured, and both correlated to assessment results. The assessment results qualify a design with an Automotive Safety Integrity Level (ASIL) which ranges from ASIL-A (lowest) to ASIL-D (highest).

In this tutorial, we will explain the scope of ISO 26262 and provide guidance on the most important attributes of the standard specific to the verification flow. Both the flow and the tool become certifiable assets and part of the safety integrity analysis. And emphasis will be placed on what needs to be done and why, versus how. The tutorial will highlight functional safety measurements and its closely related functional verification counterpart, because as we have seen in production, when you augment the functional verification aspects with functional safety aspects, you minimize duplication of effort. Further, if you are able to utilize specialized built for purpose tools such as statistical calculators for planning purposes, formal for fault collapsing, and accelerators for measuring transient faults, flow productivity is substantially improved. Lastly, as users will attest, having the right tool support for ISO26262 can become an essential asset for verification of devices that are intended to be used in a safety critical application.

While not intended to be a cookbook, that would take several days, the tutorial will reflect on the interdependencies of the verification tools to the ISO 26262 standard, providing clear visibility on to what the new verification environments need to look like and why.

Speakers:

Riccardo Oddone - *Cadence Design Systems, Inc.*
Matt Graham - *Cadence Design Systems, Inc.*
Viktor Preis - *Cadence Design Systems, Inc.*

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Tutorial 3 - How Portable Stimulus Addresses Key Verification, Test Reuse, and Portability Challenges

Time: 10:00am - 11:30am | Room: Forum 6

Organizer:

Larry Melling - *Cadence Design Systems, Inc.*

Portability of reusable test cases has long been a goal for semiconductor verification and validation teams. No one wants to "reinvent the wheel" by having to rewrite similar tests again and again. The widely accepted Accellera Universal Verification Methodology (UVM) standard enabled reuse of testbench components and constrained-random tests at the IP and block level, but limitations in terms of reuse at subsystem and full-chip level, and lack of portability across execution platforms, required a fresh look at addressing the portable stimulus and test challenge.

The Accellera portable test and stimulus standard (PSS) specification permits the creation of a single representation, reusable by a variety of users across different levels of integration under different configurations, enabling the generation of different implementations that run on a variety of execution platforms, including, but not limited to, simulation, emulation, FPGA prototyping and silicon. With such a specification in place, EDA vendors can produce tools that automatically generate stimulus, results checks, and coverage metrics tuned for a particular target.

This tutorial will examine some of the challenges using a set of common usage examples that emphasize specific verification, reuse, and portability challenges, and how portable stimulus addresses them. Verification challenges include using randomization of both data and control flow to test all legal scenarios of system level use cases. Reuse challenges include migrating tests from IP level to SOC. Portability challenges include growing tests in a meaningful way that improves coverage when running on faster platforms and being able to execute at the full platform speed.

For example, an IP user might create a model that drives a unit-level UVM-based testbench. This same IP model can be incorporated into a system-on-chip (SoC) model that can be used to generate code to run on the embedded processors in simulation while coordinating with the testbench. The same SoC model can also be used to generate test cases tuned to run on hardware platforms. For example, a test case running in silicon is likely to be much longer than one run in simulation and to check results using a checksum or CRC approach rather than comparing outputs every clock cycle.

Attendees will learn how to:

- Understand how abstract, portable test and stimulus address many of today's critical verification, test reuse, and portability challenges
- How PSS abstraction allows the capture of a complex use case that seeds generation of many legal scenarios to verify the usage example
- How PSS can target use of existing low-level sequences or drivers in generation of tests
- How PSS tests can be executed across platforms from simulation, emulation, FPGA prototype, and silicon to verify a complete chip or multi-chip system
- How to specify and gather coverage metrics at every step to assess verification completenes

Speakers:

Larry Melling - *Cadence Design Systems, Inc.*
Staffan Berg - *Mentor Graphics Corp.*
Adnan Hamid - *Breker Verification Systems, Inc.*
Adiel Khan - *Synopsys, Inc.*
Karthick Gururaj - *Vayavya Labs Pvt., Ltd.*

Tutorial 4 - Formal Verification - Too Good To Miss

Time: 10:00am - 11:30am | Room: Forum 7

Organizers:

Jason Sprott - *Verilab Ltd.*
Jonathan Bromley - *Verilab Ltd.*

This tutorial provides the confidence and basic knowledge that a typical verification engineer needs to start using formal techniques for functional verification. By considering a small case study it shows what you need to do, and how to do it, through the entire lifecycle of a formal verification project for a block-level RTL design.

Taking a whole-project view, it addresses both strategic considerations and specific details of coding techniques and tool applicability. Supporting materials will round out the details and coding patterns that were mentioned in the presentations.

This tutorial is appropriate for engineers who have experience with simulation-based verification and are considering the use of formal verification, or have already begun to use it, on a real project. It will allow attendees to embark on a formal verification project with confidence, and will also be valuable for technical managers who need to understand what new skills their team must develop to be able to use formal techniques effectively. Some very basic knowledge of SystemVerilog Assertions (SVA) is a prerequisite.

Speakers:

Jason Sprott - *Verilab Ltd.*
Jonathan Bromley - *Verilab Ltd.*

Tutorial 5 - Advanced UVM tips & tricks - tutorial

Time: 11:30am - 1:00pm | Room: Forum 4

Organizers:

Srinivasan Venkataramanan - *CVC Pvt., Ltd.*
Ajeetha Kumari - *CVC Pvt., Ltd.*

Universal Verification Methodology (UVM) is the industry standard verification methodology for Verification using SystemVerilog (SV). UVM provides means of doing verification in a well-defined and structured way. It is a culmination of well-known ideas, thoughts and best practices. It is also supported by a standard set of base classes to help building structured verification environment faster. More details about the standard can be found at: http://www.accellera.org

Given the major adoption of UVM across the globe and across the industry, advanced users are looking for tips and tricks to improve their productivity.

In this tutorial we will begin with a quick introduction to basic UVM. Then we will present few of the advanced topics in UVM such as Factory, importance of hierarchical names in the UVM environment, Configuration Database use cases, mis-use traps, run time phasing covering both active & passive phasing, phase jumping etc.

Though UVM does bring in great deal of modularity and provides flexibility in configuring, overriding transactions and components, such a power comes with its own set of issues – especially when things do not work as expected (on the testbench side as far as UVM and this tutorial is concerned). While the industry has well understood the debug of design issues, debug fn the testbench especially with modern, OOP based components is not that well understood by the community. In this tutorial the authors share their long experience of assisting customers with run time debug of common UVM issues and potential solutions to them.

We have included abstract agenda in the PDF, will add more details to make it cohesive and free flowing

Speakers:

Srinivasan Venkataramanan - *CVC Pvt., Ltd.*
Ajeetha Kumari - *CVC Pvt., Ltd.*

Tutorial 6 - UVVM - A Game Changer for FPGA VHDL Verification

Time: 11:30am - 1:00pm | Room: Forum 5

Organizer:

Espen Tallaksen - *Bitvis*

Verification overview, readability, maintainability and reuse are all vital for FPGA development efficiency and quality. UVVM VVC Framework was released in 2016 as a free and open source methodology to handle exactly these aspects - and is a true game changer for VHDL testbenches.

According to the 'Wilson Research Group Functional Verification Study' VHDL is the most used language for FPGA design. In fact VHDL is also the most used language even for FPGA verification (testbenches).

Over the last few years the VHDL language (with VHDL 2008) and VHDL verification support (with OSVVM, Bitvis Utility Library, etc.) have improved a lot, making it far simpler and more efficient to make good VHDL testbenches. However, one critical aspect has always been missing. Most advanced testbenches have a terrible architecture, - and there has been no support or defined methodology for making a structured testbench. For that reason lots of testbenches have been pure horror to understand, and even worse to extend or reuse.

Even quite simple verification scenarios like verifying a low-end UART requires a more structured testbench than normally implemented – in order for instance to find cycle related corner cases. E.g. what happens if the RX register is read at the exact same cycle as data from the RX channel is just entering the RX buffer/FIFO (or 1 cycle before or 2 after). For lots of modules and FPGAs you need to verify simultaneous activity on multiple interfaces, and in most testbenches this leads to chaos.

In fact most modules and FPGAs have multiple interfaces that need some kind of controlled stimuli and output checking. Unfortunately almost all designers and companies make more or less ad-hoc testbench solutions to handle this – resulting in far too complex verification systems, wasting development time for both their current and future projects.

UVVM changes this completely. UVVM is a verification component system that allows the implementation of a very structured testbench architecture to handle medium complexity verification challenges and upwards. A key benefit of this system is the very simple software-like VHDL test sequencer that may control your complete testbench architecture with any number of verification components. This takes overview, readability and maintainability to a new level.

Some corner cases are easily covered by applying constrained random stimuli, but covering cycle related corner cases requires a more structured approach - as multiple interfaces of a DUT must be controlled simultaneously. The VVC Framework provides a major step improvement in handling such challenges and does of course also support constrained random stimuli and functional coverage.

This presentation will explain a UVVM testbench and the VVC architecture. It will also show the simplicity of the VHDL test sequencer and how debugging can be made far more efficient, - as well as examples on how UVVM can be used to verify both data and cycle related corner cases. Most important this presentation will show you how UVVM will help you significantly with respect to testbench overview, readability, maintainability, extensibility and reuse.

UVVM was released in February this year, and the feedback from the VHDL community has been great. There are already free and open source VVCs available for AXI4-lite, Avalon-MM, AXI4-stream, UART, I2C, GPIO and SPI. This is important as a kick start for new users, but the really great strength of UVVM is the simple VVC command structure allowing anyone to easily write and understand any UVVM test sequencer, and the VVC micro architecture allowing users to very efficiently make their own well structured VVCs.

UVVM is in many ways also the simplified UVM for VHDL, made easily understandable for FPGA & HW designers.

Speaker:

Espen Tallaksen - *Bitvis*

Tutorial 7 - Platform Level Design : IP-XACT and SoC Verification

Time: 11:30am - 1:00pm | Room: Forum 6

Organizer:

Vincent Thibaut - *Magillem Design Services*

In this tutorial Magillem will introduce its advanced SoC design, verification and flow automation solutions based on IP-XACT. IP-XACT is a XML schema, standardized in IEEE Std 1685-2014, that defines and describes electronic components and their designs, complemented with a generator interface for design and flow automation.

By means of several case studies, this tutorial will show how the unique capabilities of the IP-XACT standard, which are beneficial for Platform Level Design. In addition, the usage of IP-AXCT for SoC verification is presented.

Speaker:

Vincent Thibaut - *Magillem Design Services*

Thank You to Our Sponsor: magillem

Tutorial 8 - Simplified Assertion Abstraction to Code High-reliability Requirements for the Formal Verification of Safety Critical and Other Designs

Time: 11:30am - 1:00pm | Room: Forum 7

Organizer:

David Kelf - *OneSpin Solutions GmbH*

For a number of years, companies have attempted to incorporate Formal technologies in their verification methodologies, in an effort to improve the time-to-coverage metric. Safety Critical designs have lead the way in the application of formal methods for key design blocks with high reliability characteristics.

The writing of assertions has been a limiting factor in the adoption of Formal Methods. This tutorial will explain an abstract method that simplifies the writing of correct assertions for engineers familiar with simulation-based verification, while still leveraging SystemVerilog. The coding of Safety Critical design requirements that meet the ISO26262 regulations, and how to turn these into effective assertions will also be discussed.

This tutorial is aimed at providing an easy mechanism for simulation centric engineers to high quality code assertions for the most rigorous of verification problems. It will include:

- Discuss the elements of Verification Test Plans that might be better served using formal rather than simulation, or a combination of the two.
- A look at typical Safety Critical requirements, how these relate to requirements of other design types, and how they may be easily coded in assertions.
- Show simplified ways assertions can be easily written in a simulation centric form and applied to key blocks.
- Detail how coverage information from the formal tools may be correlated with simulation data, and reflected back to the Test Plan.

The aim of this tutorial will be to provide practical, simple examples to demonstrate that Formal ABV, as used in Safety Critical methodologies, may be picked up more easily than people think and can make the job of verification significantly easier.

Speakers:

Sven Beyer - *OneSpin Solutions GmbH*
Joerg Grosse - *OneSpin Solutions GmbH*

Thank You to Our Sponsor: onespin

Tutorial 9 - An Industry Proven UVM Reuse Methodology for Coverage Driven Block Level Verification to Software Driven Chip Level Verification Across Simulation and Emulation

Time: 2:00pm - 3:30pm | Room: Forum 4

Organizer:

Mike Baird - *Willamette HDL*

Three major characteristics of reusable components and environments are self-containment, compartmentalization and consistent initialization. These characteristics must be considered when architecting and implementing a reuse methodology.

Components that are self-contained require the user to know little to nothing about the inner workings of the component. They receive information about their encapsulating component then construct and initialize child components. Self-contained components also automatically make resources within themselves available to the rest of the test bench. The UVM reuse methodology presented in this tutorial uses the uvm_config_db to share resources. These resources include virtual interface handles, agent configuration handles, sequencer handles and shared monitor handles. These resources share a unique field name. This mechanism provides an automatic association between an interface, its virtual interface handle, configuration setting for the interface and the sequencer handle used to place traffic on the interface. This simplifies access to resources associated with an interface and allows test writers to create scenarios without any knowledge of the environment architecture. This allows engineers to quickly contribute to a projects test and sequence library. It also allows managers to move engineering resources between projects without the initial project learning curve.

Efficient reuse requires grouping related functionality into packages that are not dependent on content in unrelated packages. The UVM reuse methodology presented in this tutorial employs effective use of SystemVerilog packages to group related functionality into independent compilation units. These include interface packages, environment packages and top-level test and sequence packages. Interface packages include class definitions, typedefs, type specializations and interface BFM's required to drive and monitor an interface protocol. Interface packages are reusable horizontally across projects and vertically from block to top. Environment packages contain configuration, environment and sequence base class declarations. They also include predictor and coverage component class definitions. Environment packages are reusable vertically from block to top.

Consistent construction and initialization enables a simple configuration model that enables block to top reuse. The UVM reuse methodology presented in this tutorial employs a simple and consistent initialization model that passes information from top down through a function named initialize. Each level removes information intended for that level and passes down information required by lower levels. This information includes simulation level, interface field names, hierarchical information and UVM register model handles. The simulation level argument indicates to environment instantiations the sim level of the test for example BLOCK, SUBSYSTEM, CHIP, etc. This allows environments to configure agents accordingly. Interface field names are passed down through environments to agent configurations to allow agent configurations to retrieve virtual interface handles from uvm_config_db. Hierarchical information indicating encapsulating hierarchy is passed down through configuration levels. Each level appends hierarchical information down to the agent configuration. This builds the full hierarchical path to each agent used by an agent configuration. The UVM register model handle allows for construction of the full UVM register model at the top level. Register sub block handles are passed down to sub environment configurations. This enables block to top reuse of UVM register models.

The UVM reuse techniques presented in this tutorial have enabled dozens of companies to create reuse libraries for component reuse, environment reuse and bench reuse from simulation to emulation. The techniques presented enable verification engineers to build a verification reuse library. The methodologies presented enable verification managers to efficiently assign engineering personnel where required as required by dynamic and demanding project development schedules. This tutorial is intended for verification engineers, architects and managers.

Speakers:

Mike Baird - *Willamette HDL*
Bob Oden - *Mentor Graphics Corp.*

Tutorial 10 - Model Driven Approach to Software Driven Verification

Time: 2:00pm - 3:30pm | Room: Forum 5

Organizer:

Larry Melling - *Cadence Design Systems, Inc.*

The verification of electronic systems and subsystems is generally achieved today using software tests typicaly written in C. There are several reasons for this, including:

- A need to exercise system use cases from a programmer's view
- Portability of tests across platforms (simulation, emulation, fpga, post silicon)
- Ever-growing software layers that program hardware components to provide SoC and subsystem features that need to be verified
- The challenge of creating real-life scenarios in synthetic testbenches

With today's SoCs including more cores, more IP, complex power control, coherent interconnect, and complex software controlled operations, SW driven verification is essential to verifying SoC features, but it introduces unique challenges in terms of writing tests for complex interactions at the subsystem and SoC level.

This tutorial introduces an innovative approach and new concepts that are going to revolutionize the SW driven verification world. The technique builds on proven SW testing approaches such as model based testing and Unified Modeling Language (UML). It allows capturing system actions, pre-conditions, post conditions and resource requirements to validate SoC level features and generate portable stimuli in the language and for the platform of your choice.

Speakers:

Sharon Rosenberg - *Cadence Design Systems, Inc.*
Larry Melling - *Cadence Design Systems, Inc.*

Tutorial 11 - Shadow Simulation : A New Verification Methodology for Configurable Logic

Time: 2:00pm - 3:30pm | Room: Forum 6

Organizer:

Amit Gupta - *Xilinx Inc.*

Traditional Verification methods of configurable logic incur long runtimes owing to the necessity of configuring the logic before verifying its functionality. Furthermore, they suffer from inordinate memory requirements because of the need to preserve the state machine for configuration, as well as all unused portions of the configurable logic. In addition, they pose daunting challenges in debugging since they maintain the configurable logic as a gargantuan netlist with all its hardware design hierarchy rather than as a design-oriented netlist, and the verification engineer is required to trace design logic cones through this labyrinth.

Our new verification methodology proposes a solution to these three vexing issues. The long runtimes are eliminated by providing an alternate means of configuring the logic without having to preserve the configuration state machine paraphernalia [veam attribute settings]. The inordinate memory requirements are eliminated by pruning out the unused portions of the configurable logic [prunechip]. And debuggability is significantly improved by maintaining the configured logic in a design-oriented netlist that enables the automatic comparison of design simulation with configured logic simulation, thereby significantly narrowing the scope of the manual effort required and eliminating the design size from the equation altogether [shadow simulation].

Speakers:

Amit Gupta - *Xilinx Inc.*
Chandra Mulpuri - *Xilinx Inc.*

Tutorial 12 - Back to Basics: Doing Formal the Right Way

Time: 2:00pm - 3:30pm | Room: Forum 7

Organizer:
Rebecca Granquist - *Mentor Graphics Corp.*

Automated formal apps have introduced a new generation of D&V engineers to the power of formal verification without the pain. This success has inspired renewed interest in creating formal testbenches for DUT-specific verification challenges that are well suited to formal.

Thank You to Our Sponsor: Mentor Graphics®

Join Mentor Graphics for this tutorial to learn how to:

- Write assertions the right way – easy to learn SVA coding tricks that get the most out of the formal analysis engines AND ensure reuse with simulation and emulation
- Run formal the right way – simple tips to setup the analysis for rapidly reaching a solution
- Looking at coverage the right way – measuring "minimal sequential distance" as a way to measure formal coverage and judge "what's the correct number of assertions"

Speakers:
Joe Hupcey, Abdel Ayari - *Mentor Graphics Corp.*

Tutorial 13 - UVM-SystemC goes random - Introducing CRAVE in UVM-SystemC

Time: 4:00pm - 5:30pm | Room: Forum 4

Organizer:
Stephan Gerth - *Fraunhofer IIS*

Introduction/Motivation:
UVM-SystemC is an implementation of the UVM standard for SystemC and is based on the donation of a proof-of-concept UVM implementation in SystemC to Accellera in 2014. Standardization efforts of UVM for SystemC (named UVM-SystemC) have gained momentum to the point that a public review release was done in December. This first release excluded randomization features. The active development of CRAVE, a C++ and SystemC constraint randomization library, is a promising starting point for the randomization features in UVM-SystemC. This tutorial will introduce the basic concepts and will give a range of examples on how to apply CRAVE and UVM-SystemC to address the challenges in ESL design and verification. Furthermore, it will discuss the advantages compared to the current BDD-based implementation for SystemC and their effects on UVM-SystemC.

Summary, intended audience:
This tutorial will be presented in three sections. In the first introductory section, several key mechanisms of constraint randomization in UVM contexts are explained to bring the audience to a common basic knowledge level. The basic concepts of the Universal Verification Methodology (UVM) will be presented and how constrained randomization can improve verification. The knowledge on how to effectively combine and apply UVM and constrained randomization are the key to enable the verification of complex systems. Additionally, the re-use aspect optimal verification results will be shown, especially when the design-under-test changes into a real hardware implementation. The past and current standardization efforts within the Accellera Verification Working Group will be presented to show the evolution of UVM-SystemC within the working group. Further motivation and examples are given, showing how SystemC users can benefit from a standardized UVM implementation within their SystemC environment in their daily verification needs with an updated constrained randomization implementation. The current state of the proof-of-concept implementation will be shown and how it can be applied in current design flow setups. This will be exemplified using a state of the art SystemC IDE. Support from development environments is essential to aid the developers in creating complex UVM-SystemC testbenches.

Verification examples demonstrating the applications of constrained randomization in the UVM-SystemC implementation will be presented in the second part of the tutorial. This will motivate the audience for improved constrained randomization usage in UVM-SystemC for their own experiments or projects. Furthermore, an outlook will be given how constrained randomization verification can be used for different abstraction levels of the same design-under-test, including an outlook how hardware-in-the-loop systems can be supported. This part will provide reasoning why UVM-SystemC can bring advantages for the race of the shortest time-to-market for market-driven participants.

The final section will discuss the ongoing development of the proof-of-concept implementation and the language reference manual to show clearly where UVM-SystemC is headed and what has been already achieved in the past activities. As a closing item, future standardization topics, such as functional coverage, within the Accellera Verification Working Group and further application fields of UVM-SystemC will be discussed to give the audience an outlook.

The intended audience includes managers, system and verification engineers and architects with a basic knowledge in SystemC and/or UVM, which are interested to further improve their system-level verification practices.

Speakers:
Stephan Gerth - *Fraunhofer IIS*
Daniel Große - *Univ. of Bremen & DFKI GmbH*

Tutorial 14 - Applying UPF 3.0 for Early, System-level Power Analysis of SoCs with DDR Memories

Time: 4:00pm - 5:30pm | Room: Forum 5

Organizer:

Tim Kogel - *Synopsys, Inc.*

Energy efficient design is critical to the success of many electronic products and SoCs deploying the latest DDR memory technologies. However, applying low power design techniques and power management strategies will require trade-offs around power, performance, and cost that must be analyzed early in the development cycle.

This tutorial reviews the challenges faced by SoC architects, the motivation for dynamic simulation, and the benefits of power-aware virtual prototypes. We introduce the new IEEE 1801-2015 UPF 3.0 standard and present a case study demonstration on how to apply UPF 3.0 for early, system-level power analysis of SoCs with a state-of-the-art DDR memory and memory controller.

Target Audience: System Designers, SoC Architects, Power Architects

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Tutorial 15 - Advancing the SystemC Ecosystem

Time: 4:00pm - 5:30pm | Room: Forum 6

Organizer:

Lynn Bannister-Garibaldi - *Accellera Systems Initiative*

For more than a decade, SystemC has been used by system architects and design engineers. Not only since the inclusion of Transaction Level Modeling (TLM) into the IEEE 1666-2011 SystemC standard, SystemC is the language of choice for virtual prototyping across the industry. In order to meet the needs of today's and tomorrow's electronic systems, advanced system-level design methodologies and the evolution of SystemC-related standards are required.

This tutorial gives an overview on the recent advancements to the SystemC ecosystem, ranging from the IEEE 1666.1-2016 SystemC AMS standard, summarizing the progress on the UVM-SystemC enablement and covering ongoing topics around the core SystemC/TLM language.

Speakers:

Martin Barnasconi - *NXP Semiconductors*
Karsten Einwich - *COSEDA Technologies*
Trevor Wieman - *Intel Corp.*
Peter Frey, Ellie Burns - *Mentor Graphics Corp.*
Philipp Hartmann - *Intel Corp.*

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Tutorial 16 - Designing Safe Cars - How to Ensure Your Semiconductor Design Meets ISO-26262 Fault-Safety Requirements

Time: 4:00pm - 5:30pm | Room: Forum 7

Organizer:

Amir Rahat - *Optima Design Automation*

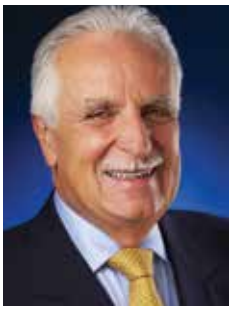
The automotive semiconductor market is expected to reach USD 48.78 Billion by 2022, at a CAGR of 5.8% between 2016 and 2022, according to a recent MarketsandMarkets report. But companies who consider entering this market find that it differs from most other markets in its safety focus. The stringent functional safety requirements, captured in the ISO-26262 standard, span both bug prevention, using proper design & validation methodologies, and fault resilience to protect against natural-occurring faults in the product.

In this tutorial we will focus on the latter, and discuss how to make a design safe from physical faults during its entire lifetime. The fault-resilience requirements for automotive products go far beyond the requirements of other fault-aware markets such as compute or storage servers, so a new methodology is required.

The tutorial will present a detailed methodology on the use of fault simulations for protection against faults. It is intended for people who are planning to design an automotive product or are already working on one, and who are interested in an easy-to-use way to meet the fault-safety requirements of the domain, such as ISO-26262.

Speaker:

Jamil Mazzawi - *Optima Design Automation*



Keynote: Gala Dinner Presentation - Supporting the Exponential Growth in New Application Areas

Time: 7:30pm - 7:50pm | Room: Ballsaal

Design and verification methodologies have been vital elements of the semiconductor ecosystem for more than 30 years and will be for the foreseeable future. The biggest challenge to semiconductor companies will evolve from supporting more advanced, leading-edge SoCs to extending their viability to support a variety of creative designs in unique application areas stretching process nodes in new ways.

Moore's Law kept familiar the exponential growth of the number of transistors on a chip. The new exponential is the number of new designs on a node. This means significant changes for design and verification flows, business models and development team cooperation. This explosion of new directions for electronic system design flows and the globally expanding design ecosystem will benefit from relatively independent, experienced design and verification experts.

They will help identify design applications to be supported at existing nodes and which of these will drive the requirements of new design and verification methodologies. Design IP will be created by communities of individuals and small entities in all geographies in the world rather than concentrated in traditional application leaders or semiconductor companies. Design and verification methodologies will be transformed to support this emerging community.

Speakers:

Lucio Lanza - *Lanza TechVentures*

THURSDAY'S AGENDA

7:30 - 8:30am	Attendee Coffee Break *Room: Foyer* *Thank You to Our Sponsor:* onespin				
8:30 - 9:45am	Keynote: The Road Ahead for the Securely Connected, Self- Driving Car *Room: Forum 6 & 7*				
9:45 - 10:30am	Panel *Room: Forum 6 & 7*				
10:30 - 10:45am	Attendee Coffee Break *Room: Foyer* *Thank You to Our Sponsor:* onespin				
10:45am - 12:15pm	Session 1 - TLM & IPXACT *Room: Forum 4*	Session 4 - UVM in Practice *Room: Forum 5*	Session 7 - Gate Level Simulation & Mixed-Signal Verification *Room: Forum 6*	Session 9 - Design Challenges *Room: Forum 7*	Special Session 11 - SystemC Evolution I *Room: Forum 8*
12:00 - 6:00pm	DVCon Europe Expo *Room: Exhibit Hall*				
12:15 - 1:15pm	Luncheon *Room: Exhibit Hall*				
1:15 - 2:45pm	Session 2 - AMS and Power *Room: Forum 4*	Session 5 - UVM Deep Dive *Room: Forum 5*	Session 8 - Mixed-Signal Verification *Room: Forum 6*	Session 10 - Functional Safety *Room: Forum 7*	Special Session 12 - SystemC Evolution II *Room: Forum 8*
2:45 - 3:15pm	Attendee Coffee Break *Room: Foyer* *Thank You to Our Sponsor:* onespin				
3:15 - 4:45pm	Session 3 - Verification Flow & Tools *Room: Forum 4*	Session 6 - Advanced Verification *Room: Forum 5*	Session 1 - Lightning Session 1 *Room: Forum 6*	Session 2 - Lightning Session 2 *Room: Forum 7*	Special Session 13 - Rethinking HDLs *Room: Forum 8*
4:45 - 5:30pm	Panel *Room: Forum 6 & 7*				
5:30 - 6:00pm	Closing Session & Best Paper Awards *Room: Exhibit Hall*				

Keynote: The Road Ahead for the Securely Connected, Self-Driving Car

Time: 8:30am - 9:45am | Room: Forum 6 & 7

Few industries are as primed for radical change in the years ahead as the worldwide automotive market. Advanced driver assistance system (ADAS) features are increasingly common in entry-level new car models, and today's high-end vehicles commonly receive over-the-air software updates and feature semi-autonomous driving functionality. Meanwhile, Silicon Valley start-ups and established auto OEMs alike are rushing to deliver the first true "self-driving" cars, thereby ushering a new era in transportation based on some of the most profound technical advancements this mature industry has seen since its inception more than 100 years ago. The U.S. are taking bold steps towards implementing V2X technologies with a planned mandate and a Smart City Challenge that fosters the rapid introduction of latest mobility innovations. Among the most critical technologies driving this revolution towards secure connected mobility and self-driving cars are:

- Highly integrated CMOS-based radar solutions that can replace today's bulky, power-consuming hardware for radar-based ADAS with sensors the size of postage stamps – for self-driving cars cocoons of such sensors are needed to enable a reliable 360 surround view of the vehicle environment, carmakers are also looking forward to replace existing ultra-sonic sensors for automated parking with modern radar technology.
- Advancements in vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I) technologies that support secure data exchanges between high-speed vehicles and roadside infrastructure.
- Sensor Fusion will be a critical component to self-driving cars. In May 2016, NXP announced a turnkey platform, BlueBox, ready to be plugged into the next car model. BlueBox uses two chips, the company's S32V vision processor and its LS2088A processor, the latter comprising eight 64-bit ARM Cortex-A72 cores. Four of the world's five largest car makers are already working with NXP's BlueBox.
- Gigabit Ethernet in-car communication technology enabling deterministic performance and real-time transport of massive data sets.

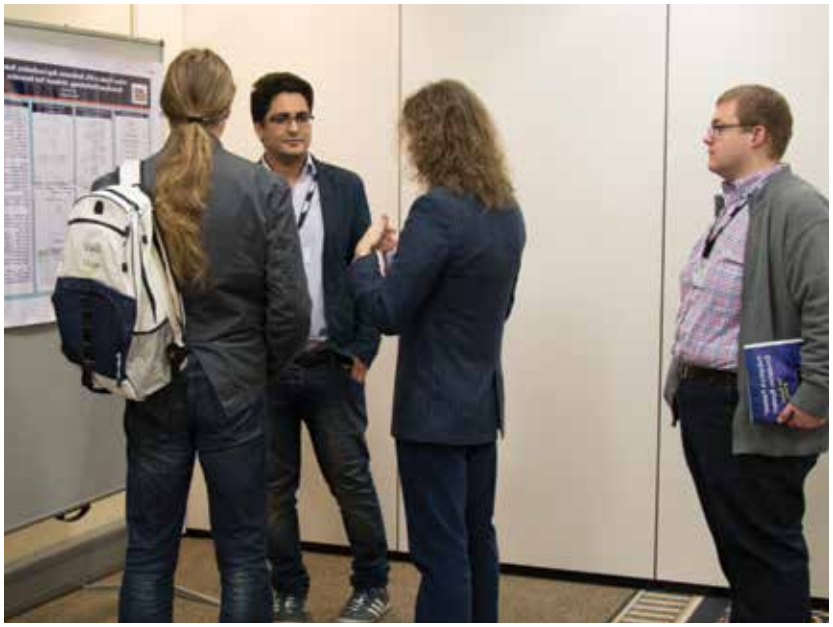
This discussion will present an in-depth examination of the specific technologies driving the autonomous vehicles revolution of the future, while detailing the security, reliability and safety requirements necessary to realize its full potential.

Speaker:

Juergen Weyer - *NXP Semiconductors*

Panel

Time: 9:45am - 10:30am | Room: Forum 6 & 7



Session 1 - TLM and IP-XACT

Time: 10:45am - 12:15pm | Room: Forum 4

Chair:
Trevor Wieman - *Intel Corp.*

1.1 Integrating Different Types of Models into a Complete Virtual System – The Simics SystemC* Library
Jakob Engblom, Andreas Hedström, Xiuliang Wang, Håkan Zeffer - *Intel Corp.*

1.2 TwIRTee Design Exploration with Capella and IP-XACT
Bassem Ouni, Pierre Gaufillet, Philippe Cuenot - *Institute of Technology Antoine de Saint Exupéry*

1.3 TLM-based Virtual Platforms at Ericsson – Challenges and Experiences
Ola Dahl, Michael Lebert, Eric Frejd - *Ericsson*

Session 4 - UVM in Practice

Time: 10:45am - 12:15pm | Room: Forum 5

Chair:
Harry Foster - *Mentor Graphics Corp.*

4.1 Reuse Doesn't Come for Free – Learnings from a UVM Deployment
Sumeet Gulati - *NXP Semiconductors*
Srinivasan Venkataramanan, Azhar Ahammad - *CVC Pvt., Ltd.*
Ketki Gosavi, Saumya Anvekar - *NXP Semiconductors*

4.2 Agnostic UVM-XX Testbench Generation
Jacob Sander S. Andersen - *SyoSil ApS*
Stephan Gerth - *Fraunhofer IIS*
Filippo Dughetti - *SyoSil ApS*

Session 7 - Gate Level Simulation and Mixed-Signal Verification

Time: 10:45am - 12:15pm | Room: Forum 6

Chair:
Matthias Bauer - *Infineon Technologies AG*

7.1 Addressing Renewed Gate Level Simulation Needs for 10nm-28nm and Below
Gagandeep Singh - *Cadence Design Systems, Inc.*

7.2 Validation of Timing Constraints on RTLReducing Risk and Effort on Gate-Level
Marcus Mueller, Peter Limmer, Dirk Moeller, Clemens Roettgermann - *NXP Semiconductors*

7.3 Modeling of Generic Transfer Functions in SystemVerilog. Demystifying the Analytic Model
Elvis Shera - *Dialog Semiconductor*

Session 9 - Design Challenges

Time: 10:45am - 12:15pm | Room: Forum 7

Chair:
Joachim Geishauser - *NXP Semiconductors*

9.1 Addressing the Complex Challenges in Low-Power Design and Verification
Madhur Bhargava, Durgesh Prasad - *Mentor Graphics (India) Pvt. Ltd.*
Jitesh Bansal - *Mentor Graphics (India) Pvt. Ltd.*
Gabriel Chidolue - *Mentor Graphics Corp.*

9.2 Yet Another Memory Manager (YAMM)
Ionut Tolea, **Andrei Vintila** - *AMIQ srl*

9.3 Safety-Verification Flow Sporting Gate-Level Accuracy and Near Virtual-Prototype Speed
Bogdan-Andrei Tabacaru, Moomen Chaari, Wolfgang Ecker, Thomas Kruse, Cristiano Novello - *Infineon Technologies AG*

Special Session 11 - SystemC Evolution I

Time: 10:45am - 12:15pm | Room: Forum 8

The SystemC Evolution Special Sessions focus on proposals to extend SystemC standards to advance the SystemC eco-system. In several presentations, selected current and future standardization topics around SystemC will be discussed in order to accelerate their progress for Accellera/IEEE standard's inclusion. The SystemC Evolution Special Session is intended as a lean, user-centric, hands-on forum bringing together experts from the SystemC user community and the Accellera Working Groups to advance the SystemC standards.

The session consists of a number of invited papers, including detailed proposals and reports on topics around virtual prototyping, how timing and events are handled for quantums, the future of TLM-2.0, multi-threading in SystemC, the relationship with C++11/14, how to better connect UVM, CCI and TLM, and developments in high-level synthesis. Each paper is designed to illicit feedback from the audience, and trigger constructive discussion which will be feedback into the Accellera working groups to help the standardization effort.

11.1 Introduction

Speaker:
Trevor Wieman - *Intel Corp.*

Author:
Trevor Wieman - *Intel Corp.*

11.2 TLM Beyond Memory Mapped Busses

Speaker:
Bart Vanthournout - *Synopsys, Inc.*

Authors:
Bart Vanthournout - *Synopsys, Inc.*
Trevor Wieman - *Intel Corp.*
Mark Burton - *GreenSocs Ltd*

11.3 The Missing SystemC and TLM Asynchronous Features Enabling Inter-Simulation Synchronisation

Speaker:
Guillaume Delbergue - *GreenSocs Ltd*

Authors:
Guillaume Delbergue, Mark Burton - *GreenSocs Ltd*
Bertrand Le Gal, Christophe Jego Bordeaux - *INP North America, Inc.*

11.4 SystemC Gaps Encountered in Virtual Platform Development

Speaker:
Eyck Jentzsch - *MINRES Technologies GmbH*

Author:
Eyck Jentzsch - *MINRES Technologies GmbH*

Session 2 - AMS and Power

Time: 1:15pm - 2:45pm | Room: Forum 4

Chair:
Wolfgang Ecker - *Infineon Technologies AG*

2.1 SystemC Extension for Power Specification, Simulation and Verification
Mikhail Moiseev, Ilya Klotchkov - *Intel Corp.*
Kirill Gagarski, Maxim Petrov - *St. Petersburg Polytechnic Univ.*

2.2 High-Performance Mixed-Signal ESL Design of a Magneto Resistive Sensor Application
Martin Barnasconi - *NXP Semiconductors*
Sumit Adhikari - *NXP Semiconductors*

2.3 Dynamic Fault Injection Library Approach for SystemC AMS
Thomas Markwirth - *Fraunhofer IIS*
Paul Ehrlich - *COSEDA Technologies*
Dominik Matter - *Hella Aglaia Mobile Vision GmbH*

Session 5 - UVM Deep Dive

Time: 1:15pm - 2:45pm | Room: Forum 5

Chair:
Jasminka Pasagic - *Texas Instruments, Inc.*

5.1 1,2,3,...8 Simple Steps Towards a Single Digital Signal Processing Testbench Supporting Heterogeneous Interfaces and Datatypes
Nico Lugil - *Keysight Technologies*

5.2 Go Figure - UVM Config - The Good, The Bad, The Debug
Rich Edelman - *Mentor Graphics Corp.*
Dirk Hansen - *Mentor Graphics Corp.*

5.3 Extending UVM Register Abstraction Layer for Verification of Register Access via Serial Bus Interface
Darko M. Tomusilovic - *Elsys Eastern Europe d.o.o.*

Session 8 - Mixed-Signal Verification

Time: 1:15pm - 2:45pm | Room: Forum 6

Chair:
Manfred Thole - *Infineon Technologies AG*

8.1 Towards a UVM-based Solution for Mixed-signal Verification
Alexander W. Rath, Sebastian Simon, Volkan Esen Wolfgang Ecker - *Infineon Technologies AG*

8.2 AMS Verification in a UVM Environment
Silvia Straehle - *Infineon Technologies AG*

8.3 Model Validation for Mixed-Signal Verification
Carsten Wegener - *Dialog Semiconductor*

Session 10 - Functional Safety

Time: 1:15pm - 2:45pm | Room: Forum 7

Chair:
Clemens Roettgermann - *NXP Semiconductors*

10.1 Institutionalizing a Certified ISO26262 Safety Process
Michael Rohleder, Clemens Roettgermann, Marcus Mueller - *NXP Semiconductors*

10.2 Fault Proof: Using Formal Techniques for Safety Verification and Fault Analysis
Adrian Traskov, Thorsten Ehrenberg, Sacha Loitz - *Continental Teves AG & Co oHG*
Abdelouahab Ayari, Avidan Efody, Joseph Hupcey III - *Mentor Graphics Corp.*

10.3 Efficient Exploration of Safety-Relevant Systems Through a Link Between Analysis and Simulation
Moomen Chaari, **Wolfgang Ecker**, Thomas Kruse, Cristiano Novello, Bogdan-Andrei Tabacaru - *Infineon Technologies AG*

Special Session 12 - SystemC Evolution II

Time: 1:15pm - 2:45pm | Room: Forum 8

The SystemC Evolution Special Sessions focus on proposals to extend SystemC standards to advance the SystemC eco-system. In several presentations, selected current and future standardization topics around SystemC will be discussed in order to accelerate their progress for Accellera/IEEE standard's inclusion. The SystemC Evolution Special Session is intended as a lean, user-centric, hands-on forum bringing together experts from the SystemC user community and the Accellera Working Groups to advance the SystemC standards.

The session consists of a number of invited papers, including detailed proposals and reports on topics around virtual prototyping, how timing and events are handled for quantums, the future of TLM-2.0, multi-threading in SystemC, the relationship with C++11/14, how to better connect UVM, CCI and TLM, and developments in high-level synthesis. Each paper is designed to illicit feedback from the audience, and trigger constructive discussion which will be feedback into the Accellera working groups to help the standardization effort.

12.1 Moving SystemC to a New C++ Standard

Speaker:
Philipp A. Hartmann - *Intel Corp.*

Authors:
Ralph Görgen - *OFFIS – Institute for Information Technology*
Philipp A. Hartmann - *Intel Corp.*

12.2 What is Next for SystemC Synthesizable Subset?

Speaker:
Peter Frey - *Mentor Graphics Corp.*

Authors:
Peter Frey - *Mentor Graphics Corp.*
Philipp A. Hartmann - *Intel Corp.*

12.3 Building a Coherent ESL Design and Verification Eco-system with SystemC, TLM, UVM-SystemC, and CCI

Speaker:
Martin Barnasconi - *NXP Semiconductors*

Author:
Martin Barnasconi - *NXP Semiconductors*

Session 3 - Verification Flow and Tools

Time: 3:15pm - 4:45pm | Room: Forum 4

Chair:
Raik Brinkmann - *OneSpin Solutions GmbH*

3.1 **How to Verify Complex FPGA Designs for Free**
Sebastian Dreßler, Nikos Anastasiadis, Thomas Richter - *Swarm64 AS Zweigstelle Hive*

3.2 **A Metric-driven Methodology For Firmware Verification In Simulation/Emulation Environments**
Goran P. Savic - *Elsys Eastern Europe d.o.o.*

3.3 **Increased Regression Efficiency with Jenkins Continuous Integration**
Thomas Ellis, **Darron K. May** - *Mentor Graphics Corp.*

Session 1 - Lightning Session 1

Time: 3:15pm - 4:30pm | Room: Forum 6

Chair:
Adiel Khan - *Synopsys, Inc.*

1L.1 **Verification Challenges for Deep Color Mode in HDMI**
Snigdha Arora - *Synopsys India Pvt. Ltd.*
Apoorva Mathur - *Synopsys India Pvt. Ltd.*

1L.2 **Slicing Through the UVM's Red Tape: a frustrated user's survival guide**
Jonathan Bromley - *Verilab, Inc.*

1L.3 **How Far Can You Take UVM Code Generation and Why Would You Want To?**
John Aynsley - *Doulos*

1L.4 **Catching the low hanging fruits in Intel® Graphics Designs : Arbiter FV**
Achutha Kiran Kumar V. Madhunapantula, Aarti Gupta, Bindumadhava S. Singanamalli - *Intel Corp.*
Abhijith A. Bharadwaj, Savitha Manojna - *Intel Technology India Pvt. Ltd*

Session 2 - Lightning Session 2

Time: 3:15pm - 4:30pm | Room: Forum 7

Chair:
Clemens Roettgermann - *NXP Semiconductors*

2L.1 **Requirement Driven Safety Verification**
Ranga Kadambi - *Infineon Technologies AG*
Vladimir Litovtchenko, Jens Rosenbusch, **Antonio Vilela** - *Infineon Technologies AG*

2L.2 **Enhancements of Metric Driven Verification for the ISO26262**
Michael Rohleder, Clemens Roettgermann, Stephan Ruettiger - *NXP Semiconductors*
John Brennan, Matt Graham, Riccardo Oddone - *Cadence Design Systems, Inc.*

2L.3 **An Open and Flexible SystemC to VHDL Workflow for Rapid Prototyping**
Bastian Farkas, Syed Abbas Ali Shah, Jan Wagner, Rolf Meyer, Rainer Buchty, Mladen Berekovic - *Technische Univ. Braunschweig*

Session 6 - Advanced Verification

Time: 3:15pm - 4:45pm | Room: Forum 5

Chair:
Thomas Klotz - *Bosch Sensortec GmbH*

6.1 **Efficient Clock Monitoring System for SoC Clock Verification**
Van Nam Pham, Bernhard Braun, Dirk Moeller, Clemens Roettgermann - *NXP Semiconductors*

6.2 **A Structured Approach to verify Ties, Unconnected Signals and Parameters**
Saurabh Singh, Peter Limmer, Thomas Luedeke - *NXP Semiconductors*

6.3 **Complete Formal Verification of a Family of Automotive DSPs**
Rafal A. Baranowski, Marco Trunzer - *Robert Bosch GmbH*

Special Session 13 - Special Session: Rethinking HDLs

Time: 3:15pm - 4:45pm | Room: Forum 8

Chair:

Wolfgang Ecker - *Infineon Technologies AG*

HDLs are the backbone of today's digital design. They are supported by a bunch of different tools and EDA companies even if there is some difference in their interpretation and usage. However, the HDLs haven't evolved substantially since the last 10 years – and in many aspects even since the last 25 years. The main players are VHDL - the HDL Zombie, SystemVerilog - the Frankenstein, and SystemC - the C++ library.

Their contribution in closing the so called design gap is in best case ignorable if not negative, so an often heard opinion! Is this true and if yes, what are alternatives? More focus on design, a formal instead a simulation based semantic, a language suite, object oriented or functional features, or generation languages?

These and other aspects shall be presented and discussed. The expected output is a summary of potential scenarios helping to improve the HDL based design flow. These scenarios shall act as crystallization point for co-operations and further activities as research projects in this area.

Panel

Time: 4:45pm - 5:30pm | Room: Forum 6 & 7

Closing Session - Best Paper Awards

Time: 5:30pm - 6:00pm | Room: Exhibit Hall

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Thursday, October 20 --------- 12:00 - 6:00pm

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* As of 9/28/2016

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Wednesday, October 19

7:30 - 8:30am
9:30 - 10:00am
3:30 - 4:00pm

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Thursday, October 20

7:30 - 8:30am
10:30 - 10:45am
2:45 - 3:15pm

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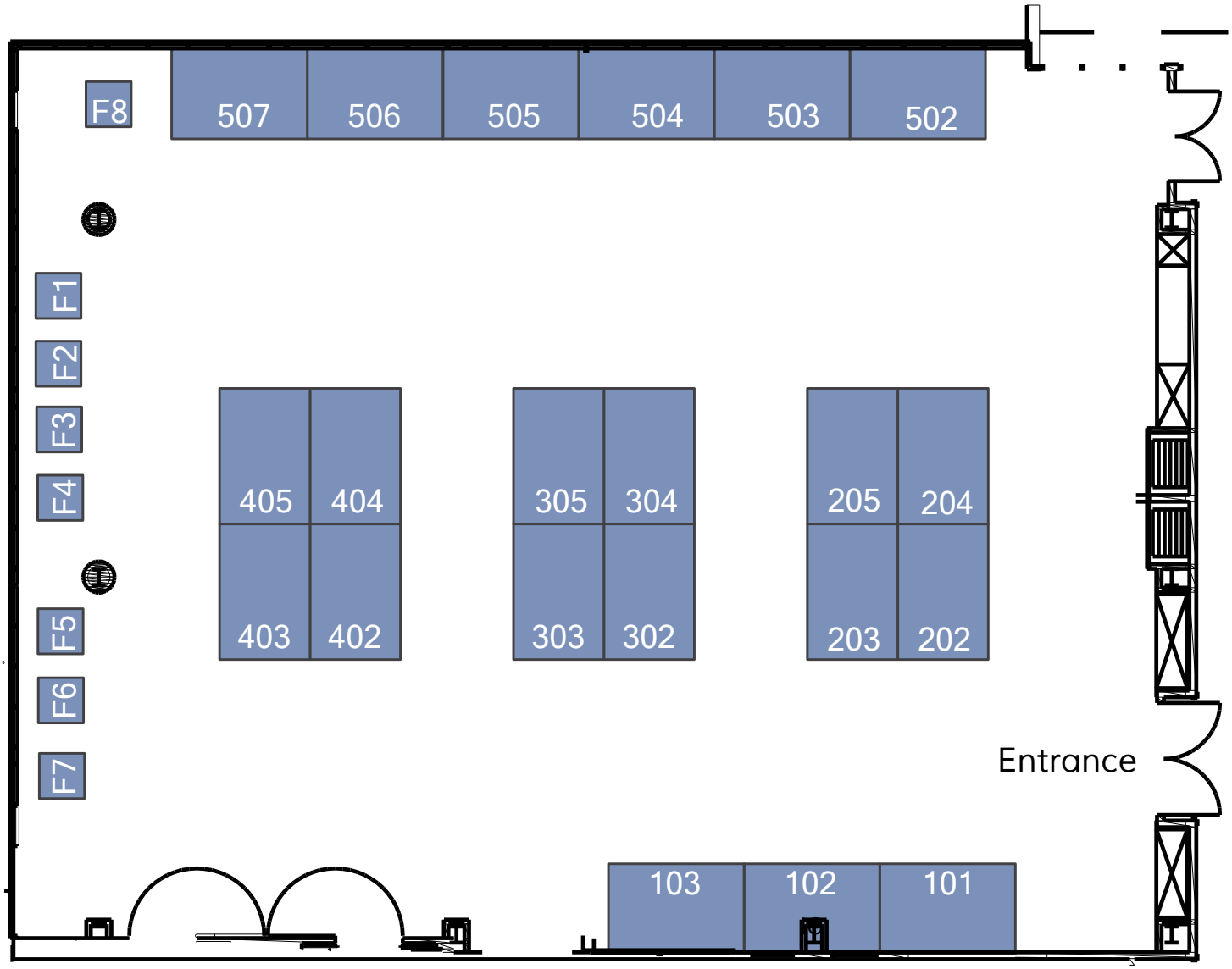
EXHIBITOR FLOORPLAN



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Aldec Inc., established in 1984 and headquartered in Henderson, Nevada, is an industry leader in Electronic Design Verification and offers a patented technology suite including: RTL Design, RTL Simulators, Hardware-Assisted Verification, SoC and ASIC Prototyping, Design Rule Checking, IP Cores, Embedded, Requirements Lifecycle Management, DO-254 Functional Verification and Military/Aerospace solutions. www.aldec.com

AMIQ EDA

Booth: 202 | www.amiq.com

AMIQ EDA provides software tools that enable design and verification engineers to increase the speed and quality of code development, simplify maintenance, improve testbench reliability, and implement best coding practices. The company serves customers around the world and its solutions - DVT Eclipse IDE, DVT Debugger Add-On, Verissimo Linter and Specador Documentation Generator - have been recognized for their high level of quality.

ANKASYS

Booth: F1 | http://www.ankasys.com

ANKASYS is a microelectronic design and verification company providing advanced design and verification services to its customers from specification to final ASIC GDS or FPGA based embedded systems. The two co-founders bring more than two decades of ASIC/FPGA design and verification experience. The company provides design and verification trainings targeting mainly FPGA-based design, Verilog/ SystemVerilog language and the application of the OVM/UVM methodology.

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A leader in Verification IP providing robust models, compliance testsuites, and services for PCI Express, USB/xHCI, UFS/UFSHCI, NVMe/f, SATA Express, SATA, UniPro, Soundwire, Sensewire, CSI/DSI, HDMI, DP, eMMC, SDIO, DDR4/LPDDR4, HBM, HMC, ONFI/Toggle, CAN FD, LIN, FlexRay, and ACE/AXI3/AXI4/AHB. A leader in verification tools. SimXACT automatically eliminates X bugs in RTL and gate-level simulation. ResetOPT minimizes reset/ retention design overhead.

Blue Pearl Software

Booth: 405 | www.bluepearlsoftware.com

Blue Pearl Software, Inc., an industry leading provider of design automation software for ASIC, FPGA and IP RTL verification, offers Linting, debug, and CDC solutions proven to improve quality of results, accelerate RTL error find/fix rates while ensuring uniform coding styles. Blue Pearl provides out-of-the-box consistent results, easy setup, SDC generation, management dashboard views and runs on Linux and Windows.

Cadence Design Systems, Inc.

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Cadence enables global electronic design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence software, hardware, IP and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. The company is headquartered in San Jose, Calif., with worldwide sales offices, design and research centers.

CircuitSutra Technologies Pvt. Ltd.

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CircuitSutra is an ESL design IP and services company, headquartered in India, having offices in Noida and Bangalore, and serves the customers worldwide. It enables customers to adopt advanced methodologies based on C, C++, SystemC, TLM, IP-XACT, UVM-SystemC, SystemC-AMS, Verilog-AMS. Its core competencies include Virtual Prototype (Development, Verification, Deployment), Architecture & Performance modeling, Co-simulation, Co-emulation, HLS, SoC & System verification.

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Design is at the heart of what we do at Cyient. Visit our booth (#404) to discuss how we can help your business utilize our capabilities in key areas, such as design verification and validation, digital verification, and analog mixed-signal verification. We are an acknowledged leader in engineering design services, design led manufacturing, networks and operations, data transformation, and analytics.

Dizain-Sync

Booth: 204 | www.dizain-sync.com

Dizain-Sync is an independent consultancy organisation in electronic design & development, with more than 25 years experience. With our knowledge we offer a unique perspective on the combination of PLM, EDA, Design and Training services. Dizain-Sync's mission is to maximize customer productivity by improving Design Methodology, Design Flow, Design and Designers.

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Doulos has set the industry standard for high quality training and KnowHow for 25 years in design and verification languages and methodologies for system, hardware, and embedded software designers. The essential choice for 3000+ companies across 60+ countries, Doulos provides scheduled classes across North America and Europe, and delivers on-site and live online training worldwide.

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Booth: F2 | http://www.edalab.it

EDALab is a software house committed in the development of the HIFSuite Tools (www.hifsuite.com), a set of tools for the automatic manipulation and translation in SystemC/C++ of VHDL and Verilog IPs. EDALab also provides design services and consultancy based on HIFSuite tools and targeted for Virtual Platforms and ESL domain."

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ElectraIC provides D&V services especially for Advanced Verification for Safety Critical Digital Hardware Development. ElectraIC can work with you in your DO-254 projects, support you as an independent verification team for your DAL-A and DAL-B product verifications or help you deploying methods, tools and templates required in a DO-254 certification process like configuration management, requirements traceability, verification procedures and records, etc.

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Mentor Graphics Corp.

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Mentor Graphics delivers the most comprehensive Enterprise Verification PlatformT (EVP), which combines QuestaR for high performance simulation, verification management and coverage closure, low-power verification with UPF, CDC, Formal Verification, accelerated functional coverage, and processor-based hardware verification, Velocer OS3 global emulation technology, and the VisualizerT debug environment, to deliver performance and productivity improvements ranging from 400X to 10,000X.

OneSpin Solutions

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OneSpin demonstrates formal technology leadership through a range of advanced verification solutions. These include agile design evaluation, advanced, coverage-driven ABV, and automated DV apps. Leading-edge challenges are addressed, including safety critical, high-reliability verification, SystemC/C++ algorithm analysis, and FPGA Equivalency Checking. OneSpin has grown dramatically in the last three years and may be found at many electronics companies worldwide.

Sigasi

Booth: 402 | www.sigasi.com

To radically redefine digital design that is what Sigasi aims for. Our design entry tool, Sigasi Studio, drastically improves hardware designer productivity by helping to write, inspect and modify digital circuit designs in the most intuitive way. It supports advanced features such as intelligent autocompletes and code refactoring. VHDL and Verilog design have never been easier, more efficient and fun. Sigasi was founded in 2008 in Belgium and has customers worldwide in all fields of industry.

SmartDV Technologies

Booth: 101 | www.smart-dv.com

SmartDV creates standard and custom verification intellectual property (VIP), memory models and simulation acceleration VIPs designed to work with coverage-driven verification flows. All SmartDV VIPs ship with compliance test-suite and comprehensive functional coverage models. All VIPs are native UVM or language of customer choice. For more information on SmartDV's products, see http://www.smart-dv.com/products.html

Synopsys, Inc.

Booth: 303 | www.synopsys.com

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SyoSil ApS

Booth: F5 | www.syosil.com

SyoSil is a leader in FPGA/ASIC design and verification solutions, including device firmware and tool development. We advice our clients on how to improve their design and verification methodologies, and deliver turn-key verification flows and Verification IP, based on industry standards such as SystemVerilog/UVM. Our clients include top European and U.S. semiconductor companies.

TRIAS Mikroelektronik GmbH

Booth: F7 | www.trias-mikro.de

TRIAS Mikroelektronik GmbH, founded in 1989, is focused on EDA solutions for FPGA/IC Design and advanced verification solutions. Our experienced engineers advise and provide training for FPGA/IC developers in SystemVerilog / UVM, VHDL-2008 / OSVVM and UVVM amongst others. We provide Clock-Domain Crossing Analysis, Formal Verification, Verification IP and an easy entry into UVM especially for more complex FPGA designs.

Truechip Solutions Pvt. Ltd.

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