



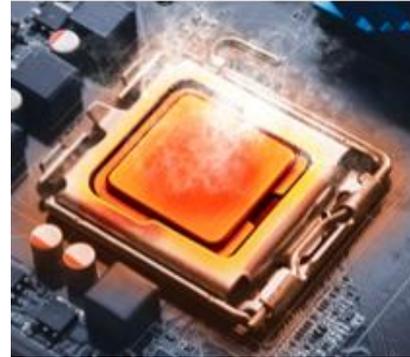
Taming Operational Power in Early Design Stage

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Importance of Low Power Design

- **Longer batter life** for smartphone, wearable, IoT, electric car
- **Reliability and longevity** of device (EM, device aging)
- **Smaller operating cost** for data center and AI/HPC
- **Sustainable computing** with lower energy footprint

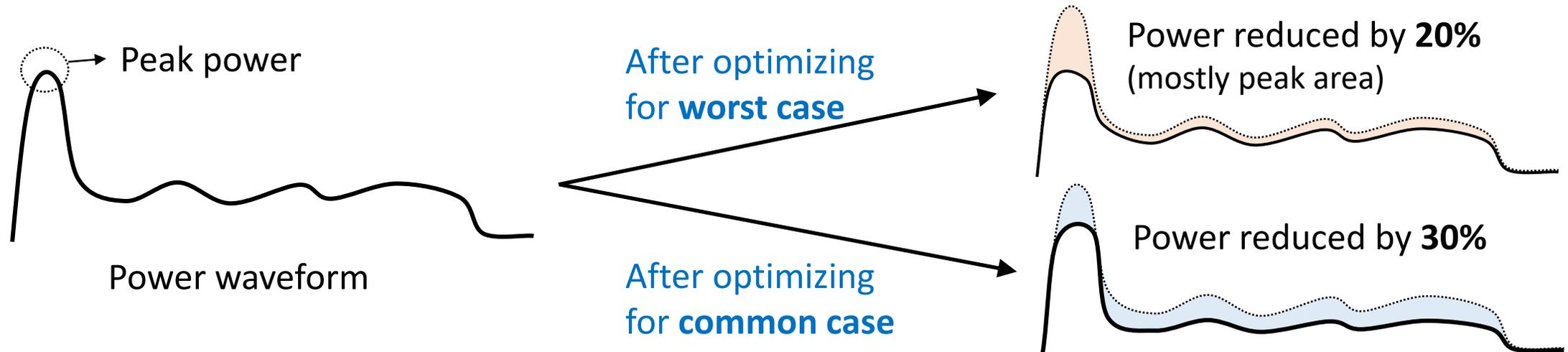


Low Power Design Challenges

- Early power prediction is hard
 - Early estimates can be off by **>30%**
 - Power is highly **workload-dependent**, and synthetic testcases often produce unrealistic results
- Slow and inefficient power verification
 - Accurate gate-level analysis is **too slow**, and often comes **too late** to drive meaningful design changes
 - A focus on **worst-case power** can mislead optimization efforts and mask real operational issues

Worst-Case Power Optimization Falls Short

- Focus on **worst-case power** is common practice, **but**
 - Accurate worst-case power become available **too late** – slow and inflexible for exploring power trade-off
 - Optimizing for worst-case (often unrealistic) can result in **sub-optimal power in real workloads**

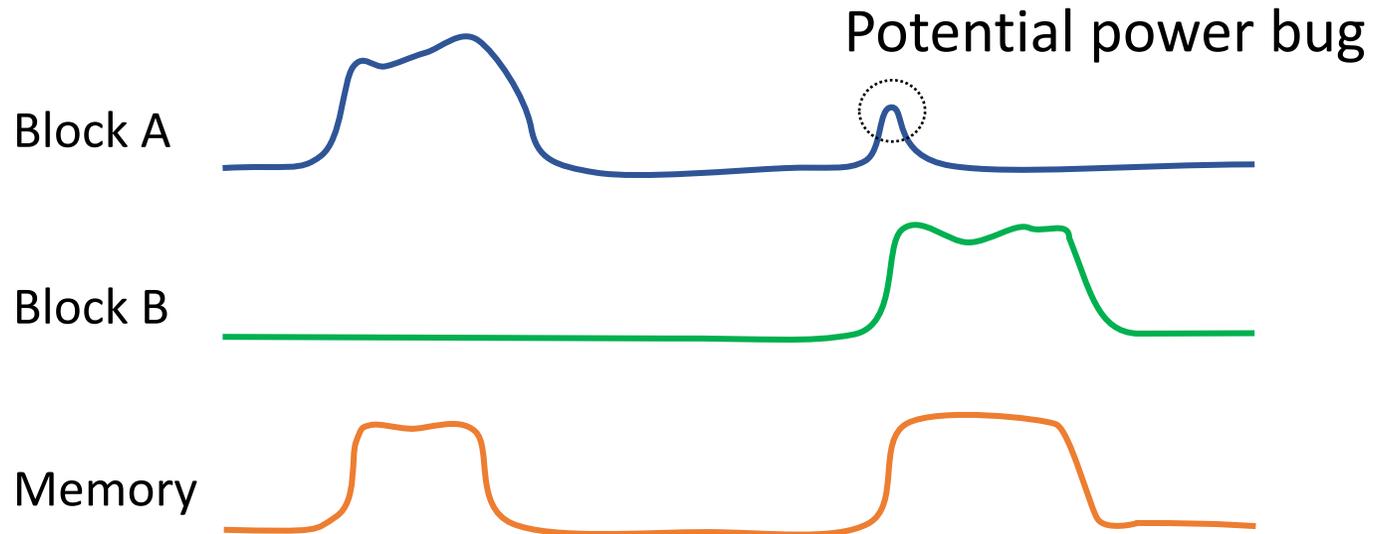
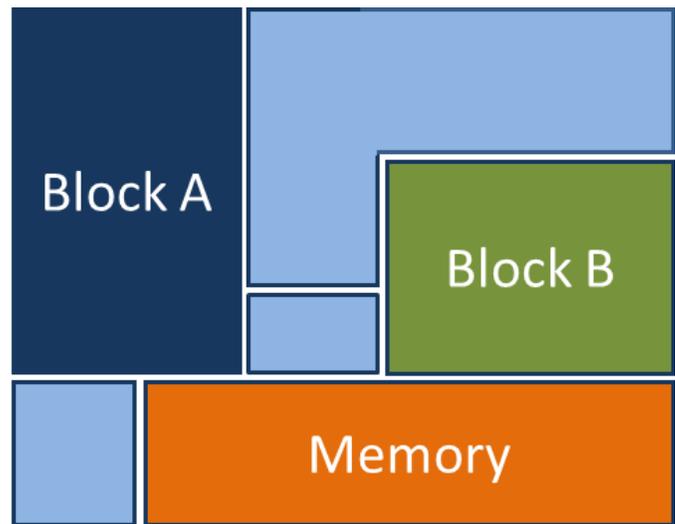


Shift Toward Operational Power Optimization

- What is good low-power solution?
 - One that delivers **lowest power silicon with actual workload**
 - Power needs to be monitored and optimized through out design flow using **realistic workload** (operational power)
- Worst-case power analysis is necessary
 - Reliability, IR drop, power distribution network, ...
 - But not sufficient for making informed power decisions
- What's needed is **actionable analysis early in the design cycle** to drive operational power optimization before silicon

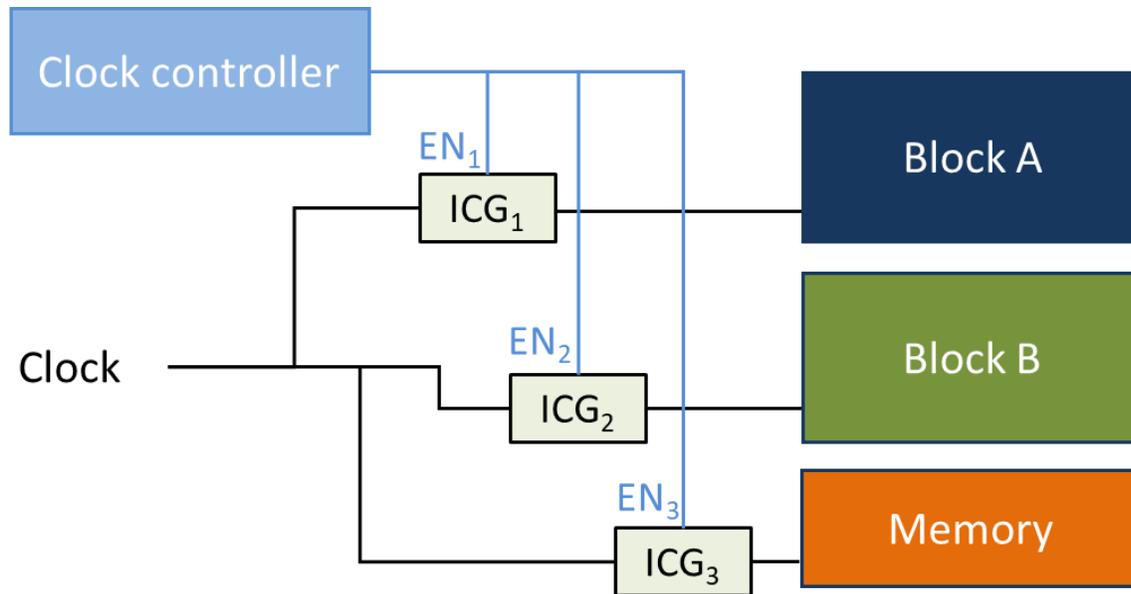
Activity as Power Proxy

- Available in **early stage** with strong **late-stage correlation**
- **Fast monitoring** of activity patterns under real workloads
- **Easy** anomaly detection (e.g. power bug)

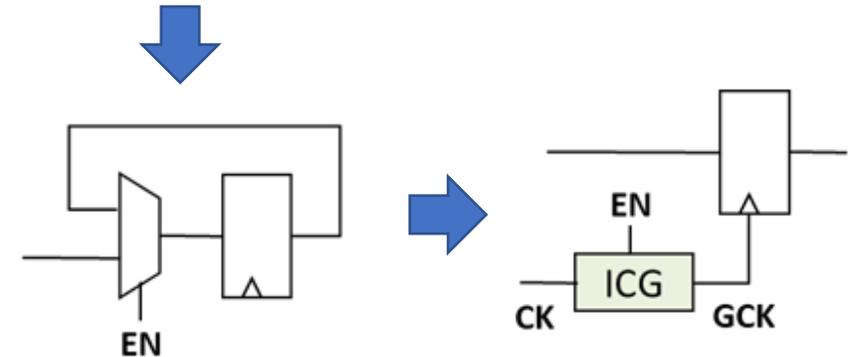


RTL Clock Gating

- Clock gating is pervasively used in modern chip
 - Clock attributes 30~60% of total dynamic power
 - Coarse- & fine-grained clock gating opportunities determined in RTL



```
always @(posedge clk) begin
  if (EN)
    Q <= D;
  else
    Q <= Q;
end
```



Clock Gating Activity as Power Proxy

- Clock gating activity correlates well with total power



* Active Clock Ratio (ACR) plots ratio of registers whose clock is active

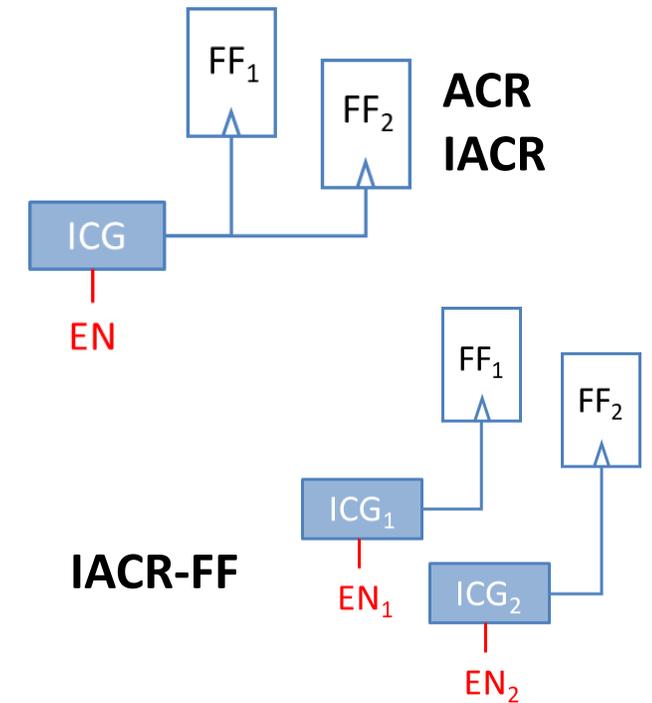
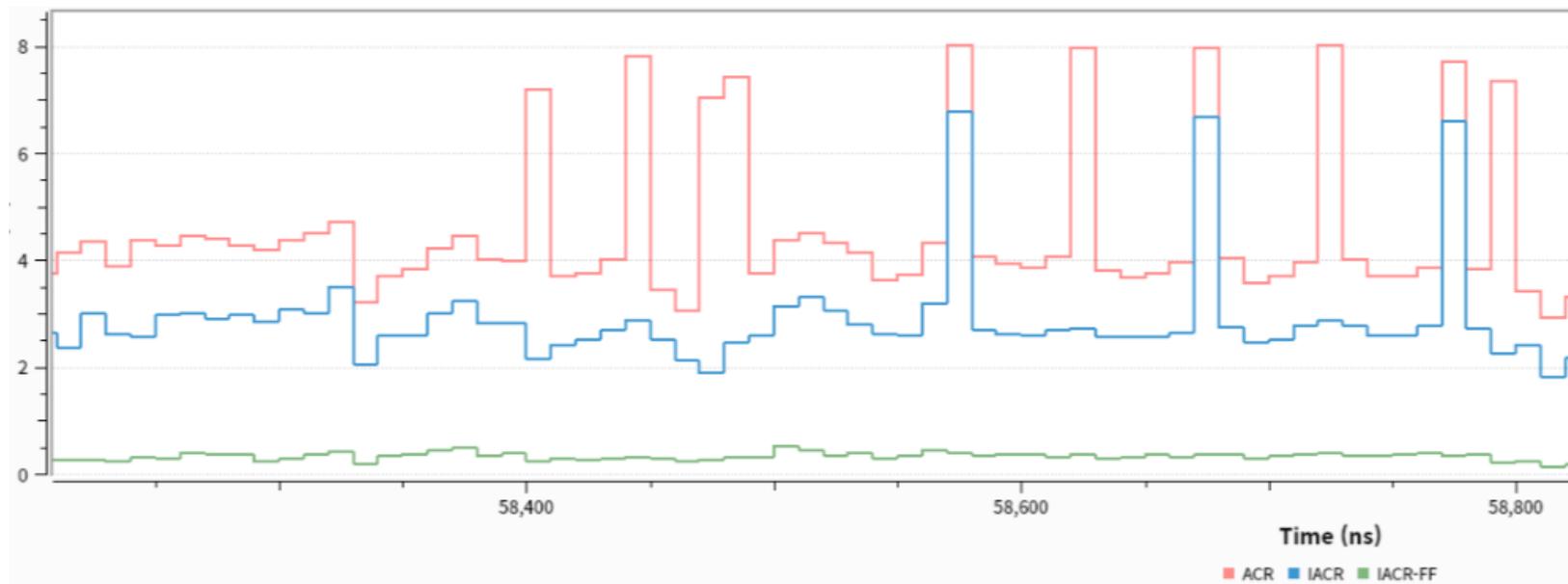
PowerSpion

- Super fast clock-gating analyzer (>10x faster vs other RTL tools)
+ power-proxy waveform for power insights

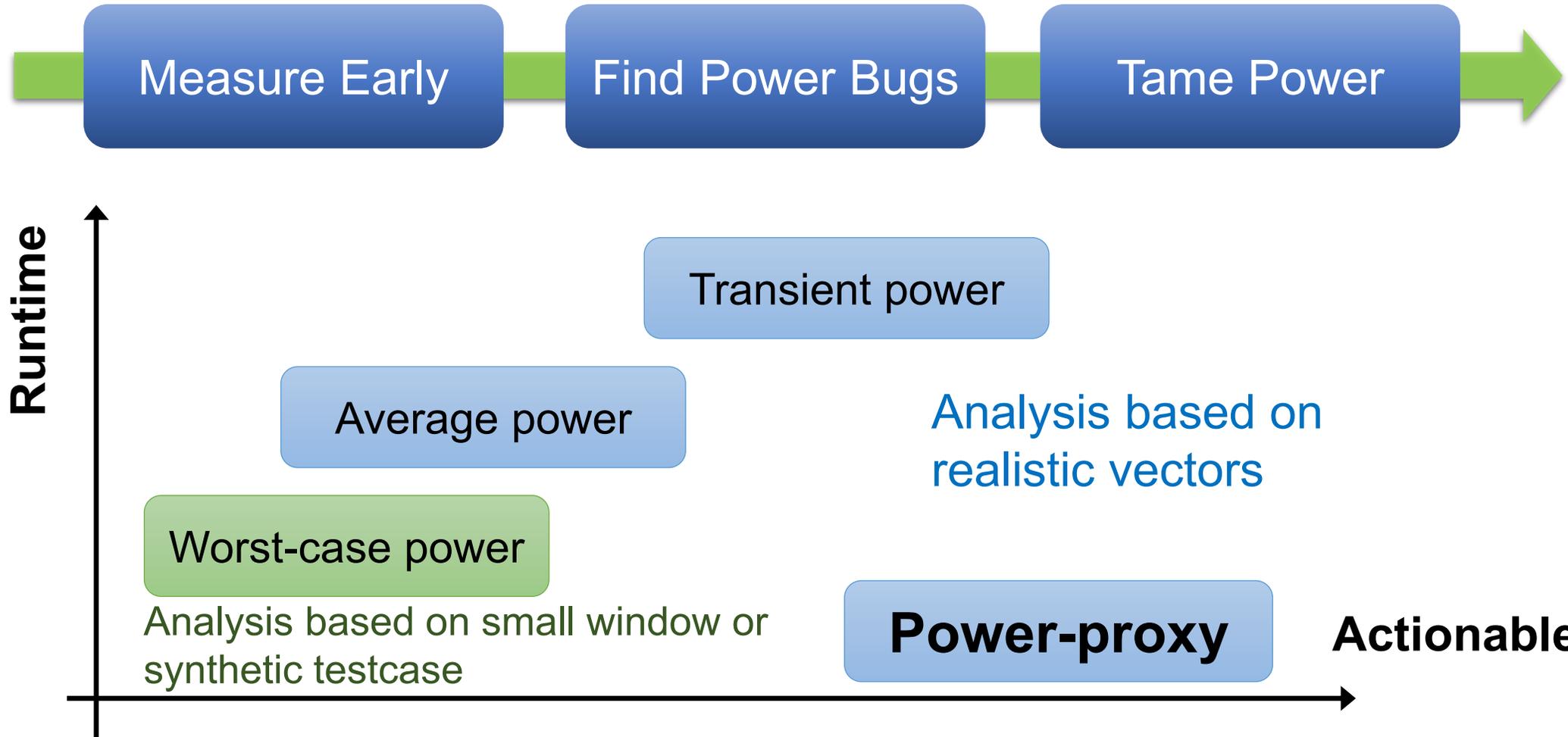
	Power waveform	Power-proxy waveform
Approach	Power analysis on internally-synthesized netlist from RTL	Clock-gating analysis on RTL
Runtime	Slow (e.g. 24h)	Very fast (e.g. 1~2h)
Accuracy	30% error is common; category power does not correlate well even after calibration	Clock activity information is preserved through P&R
Use case	RTL power signoff Detect power anomaly	Optimize CGE & operational power Detect power anomaly

PowerSpion: Power-Proxy Waveforms

- Power-proxy waveforms provide actionable power insights
 - **Ideal ACR (IACR)** is empirical lower-bound of ACR
 - **Ideal ACR per FF (IACR-FF)** is empirical lower-bound of ACR w/ ideal clock-gating group



Shift Left Power Optimization



Summary

- Tackling **worst-case power** is not enough – **real-world operational power** must be managed
- Low power design is challenging, especially in early stage; **PowerSpion** bridges this gap by offering various **actionable RTL power-proxy**, with order-of-magnitude faster runtime
- Shift-left, measure early, and tame power before it becomes a silicon problem

Questions