AutoDV - Click, Verify and Relax

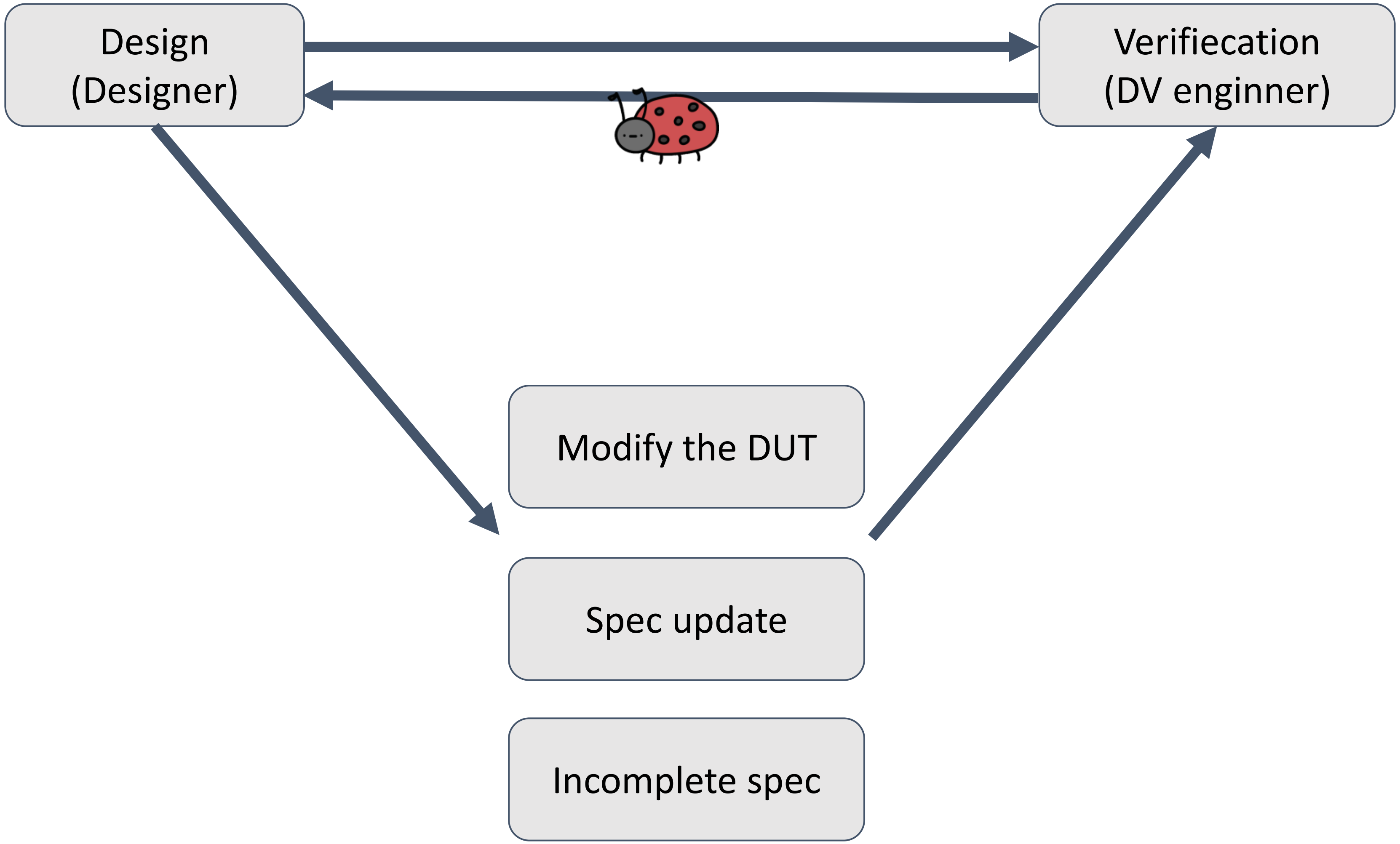
TESDA – Allen Chen, Eric Cheng

70%

70% of a project time spend on verification

WHY?

WHY SUFFER?



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Are we working efficiently?

Is it effective?

Slow?

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33%

33% success rate

WHAT IF?

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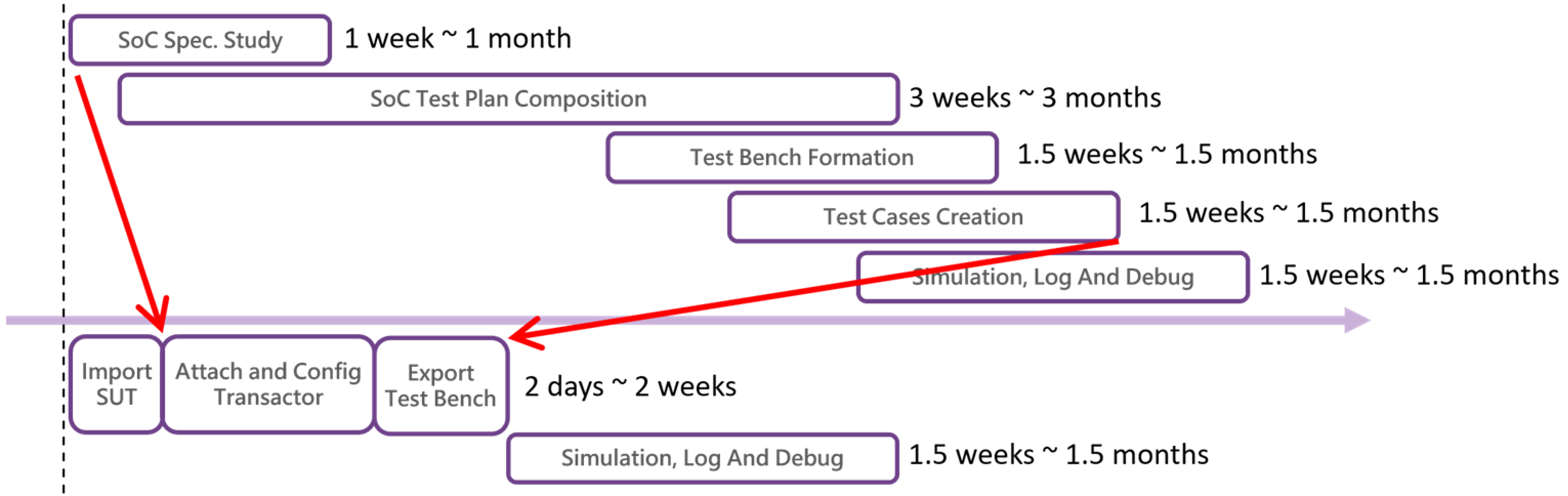
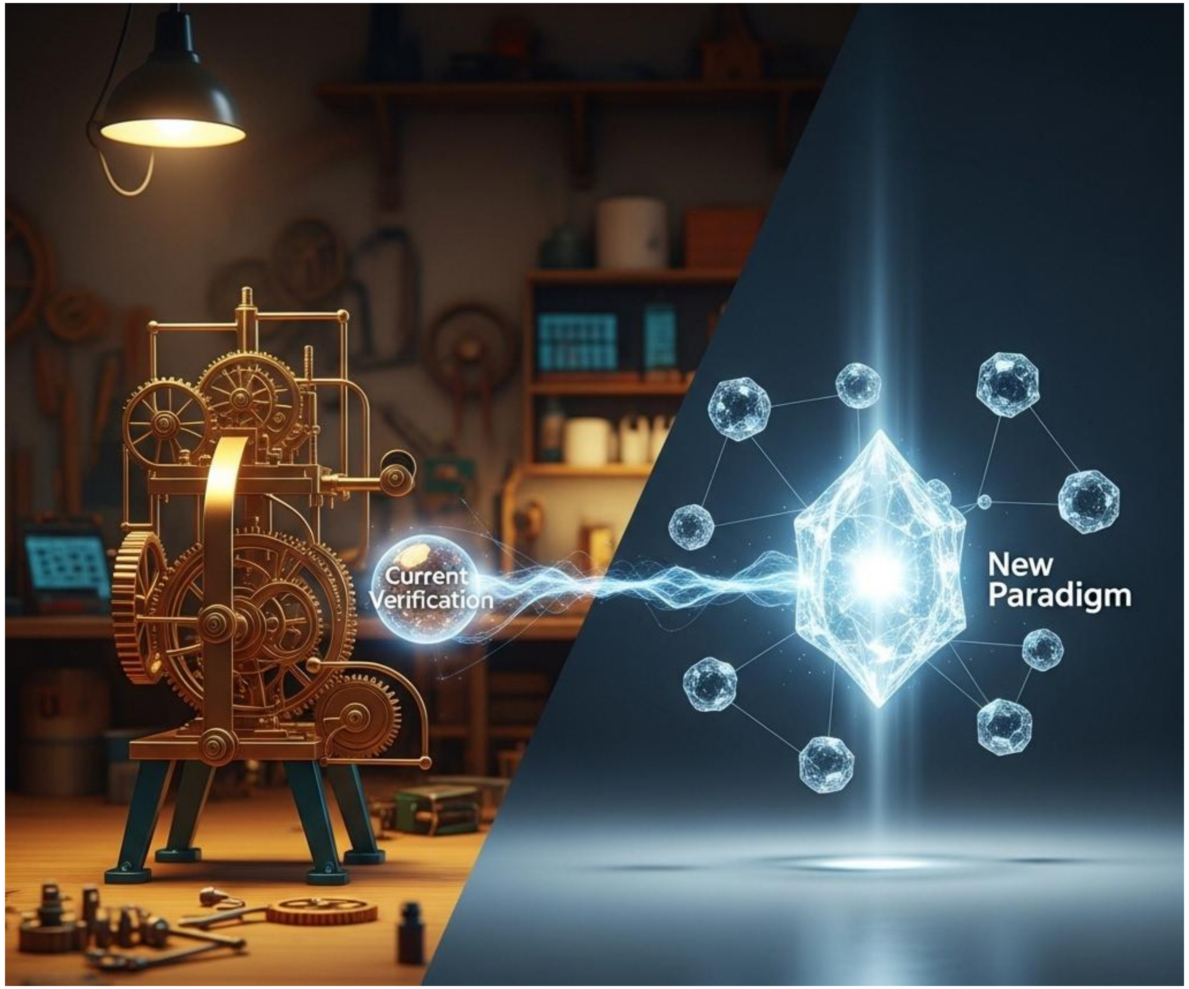


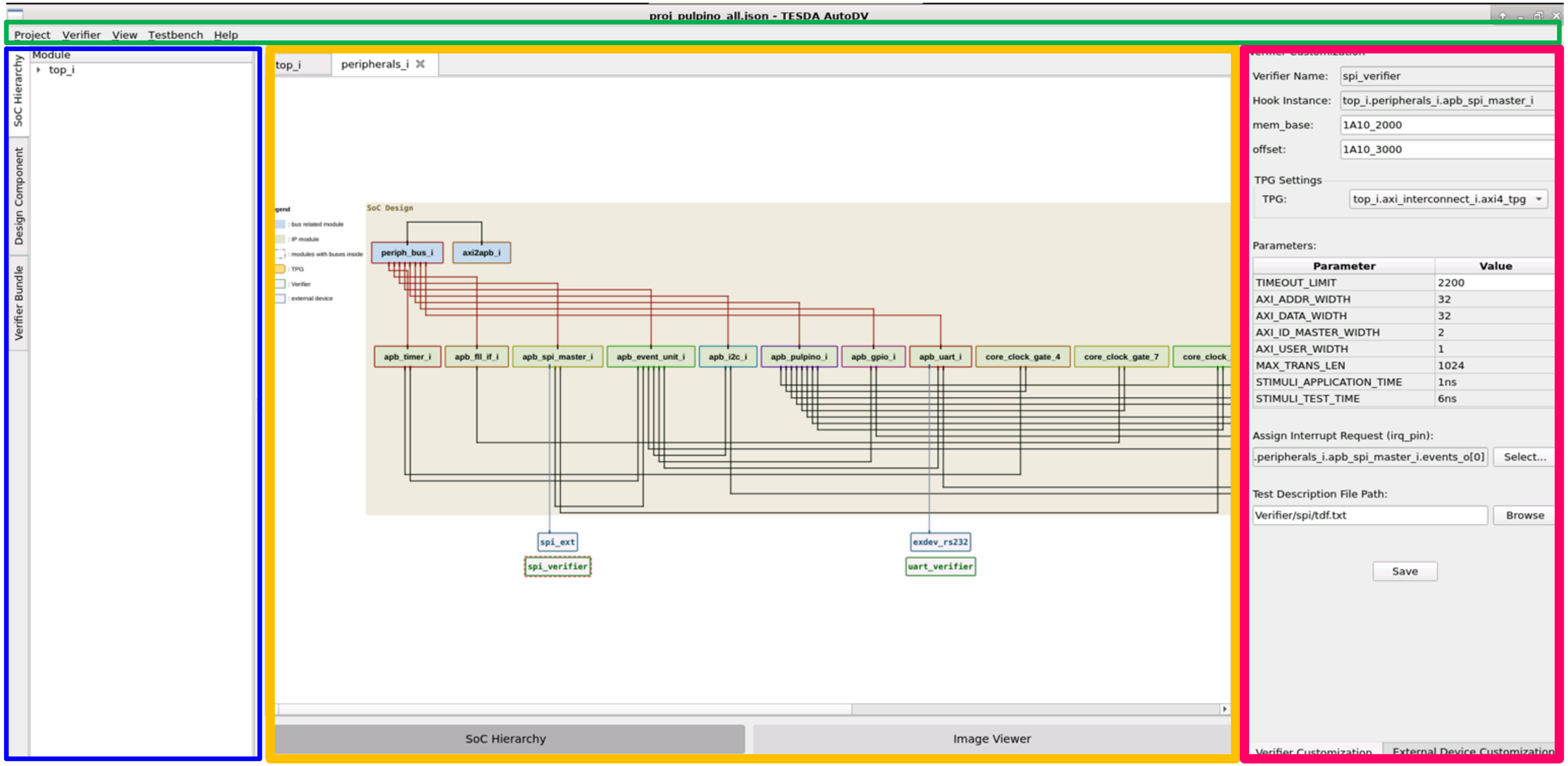
- **Encapsulate and reuse knowledge**

Before: 7 weeks ~ 7 months → After: 2 days ~ 2 weeks


Current
Verification
New
Paradigm

AutoDV

Overview

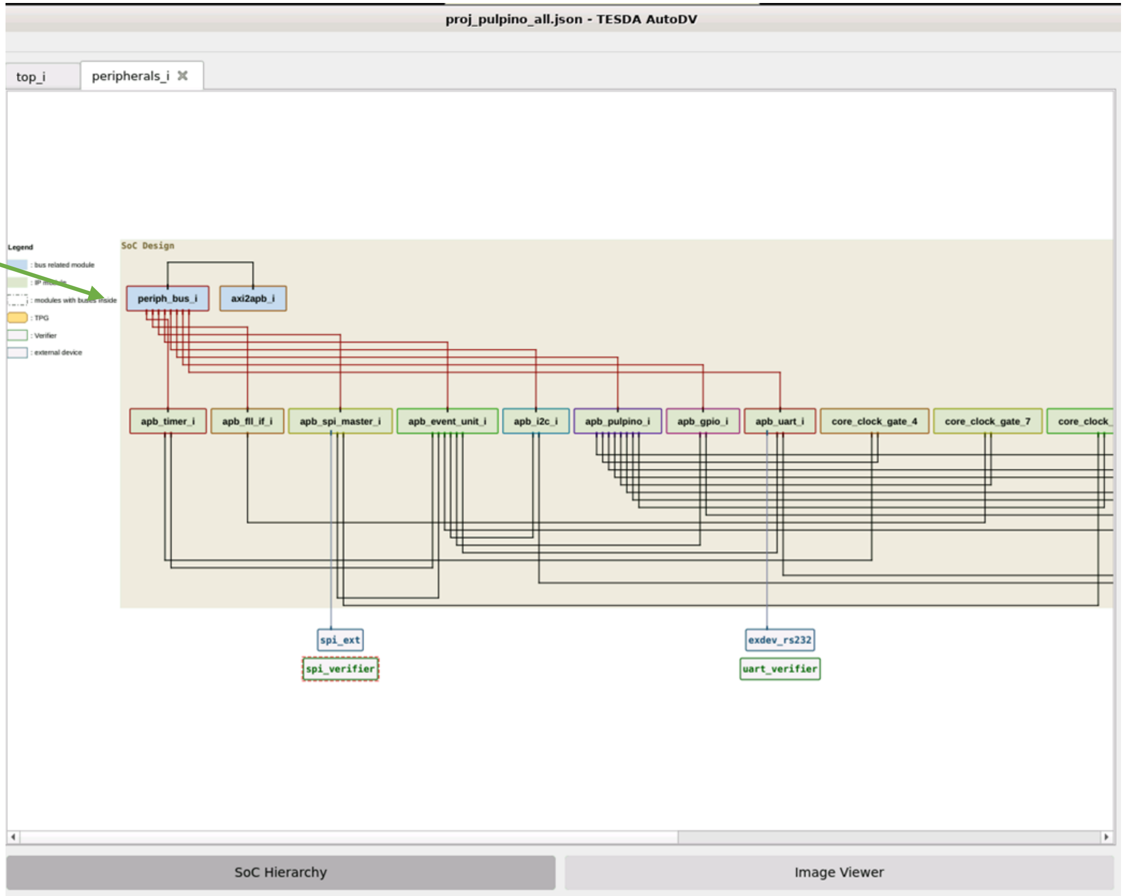


proj_pulpino_all.json - TESDA AutoDV
Project Verifier View Testbench Help
SoC Hierarchy
Design Component
Verifier Bundle
Module
top_i
top_i
peripherals_i
SoC Design
periph_bus_i
axi2apb_i
apb_timer_i
apb_fll_if_i
apb_spi_master_i
apb_event_unit_i
apb_i2c_i
apb_pulpino_i
apb_gpio_i
apb_uart_i
core_clock_gate_4
core_clock_gate_7
spi_ext
spi_verifier
exdev_rs232
uart_verifier
SoC Hierarchy
Image Viewer
Verifier Name: spi_verifier
Hook Instance: top_i.peripherals_i.apb_spi_master_i
mem_base: 1A10_2000
offset: 1A10_3000
TPG Settings
TPG: top_i.axi_interconnect_i.axi4_tpg
Parameters:
Parameter | Value
TIMEOUT_LIMIT | 2200
AXI_ADDR_WIDTH | 32
AXI_DATA_WIDTH | 32
AXI_ID_MASTER_WIDTH | 2
AXI_USER_WIDTH | 1
MAX_TRANS_LEN | 1024
STIMULI_APPLICATION_TIME | 1ns
STIMULI_TEST_TIME | 6ns
Assign Interrupt Request (irq_pin):
.peripherals_i.apb_spi_master_i.events_o[0]
Select...
Test Description File Path:
Verifier/spi/tdf.txt
Browse
Save
Verifier Customization
External Device Customization

Instant Testbench Setup

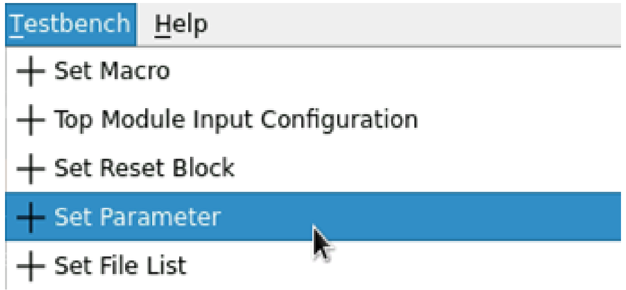
SoC design

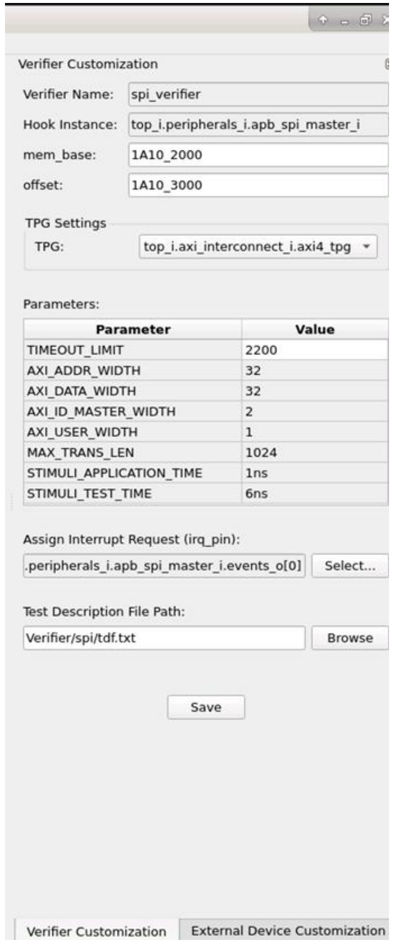
Import Design



Instant Testbench Setup

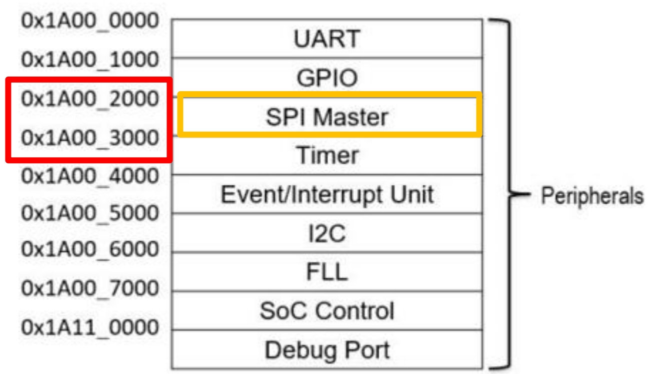
Configuration

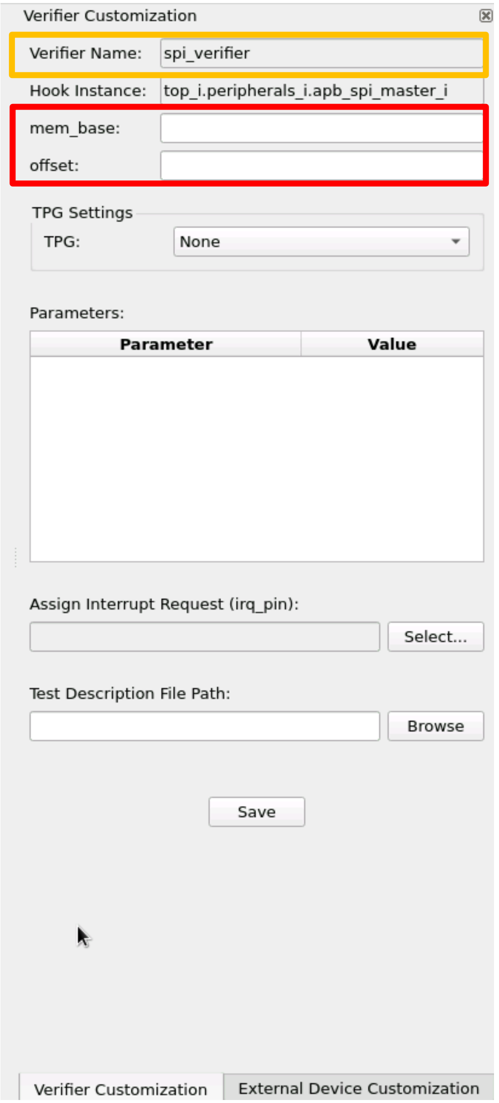


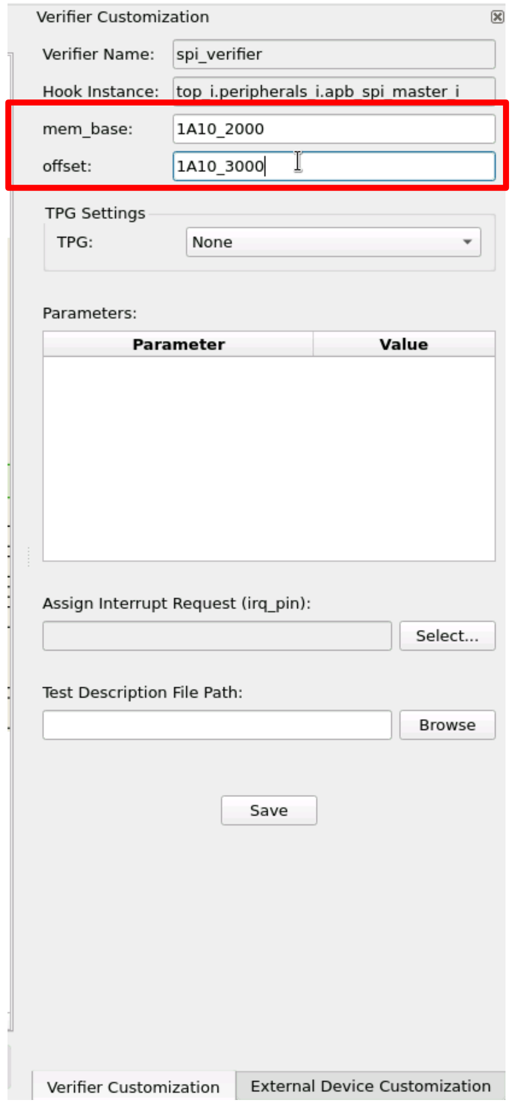


Memory Mapping Configuration

Memory map







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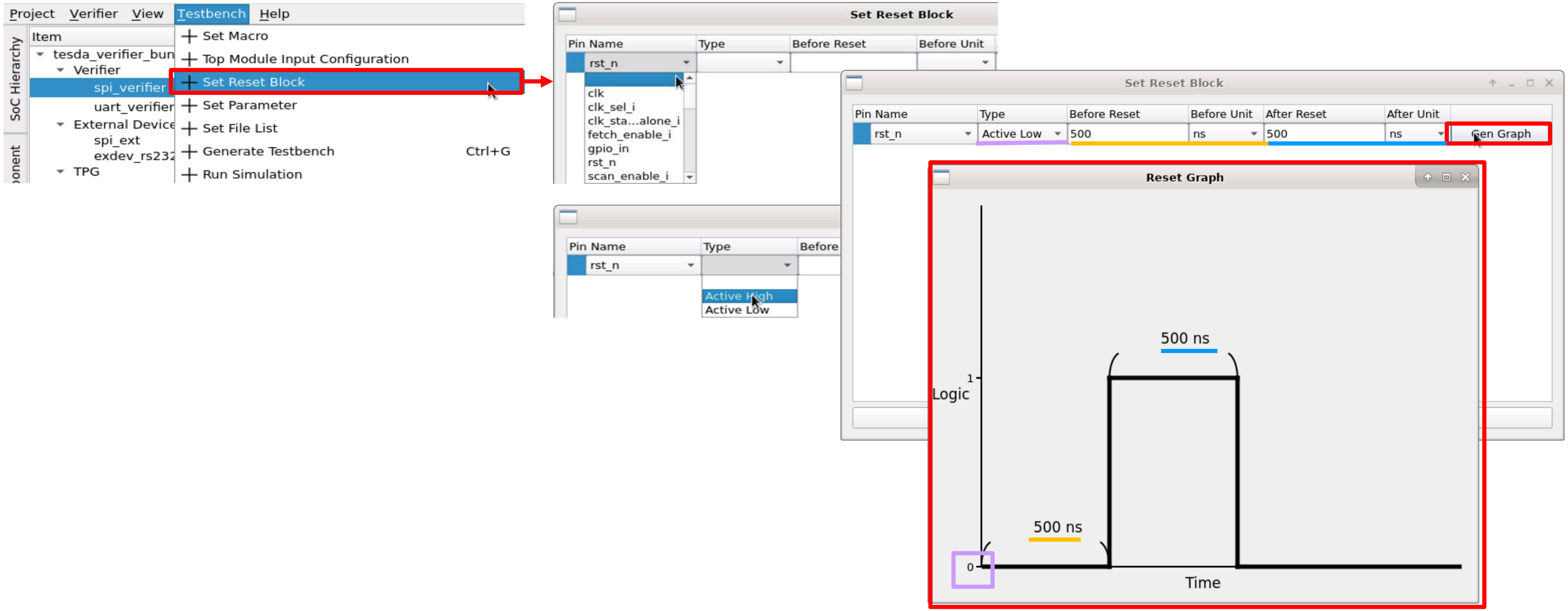
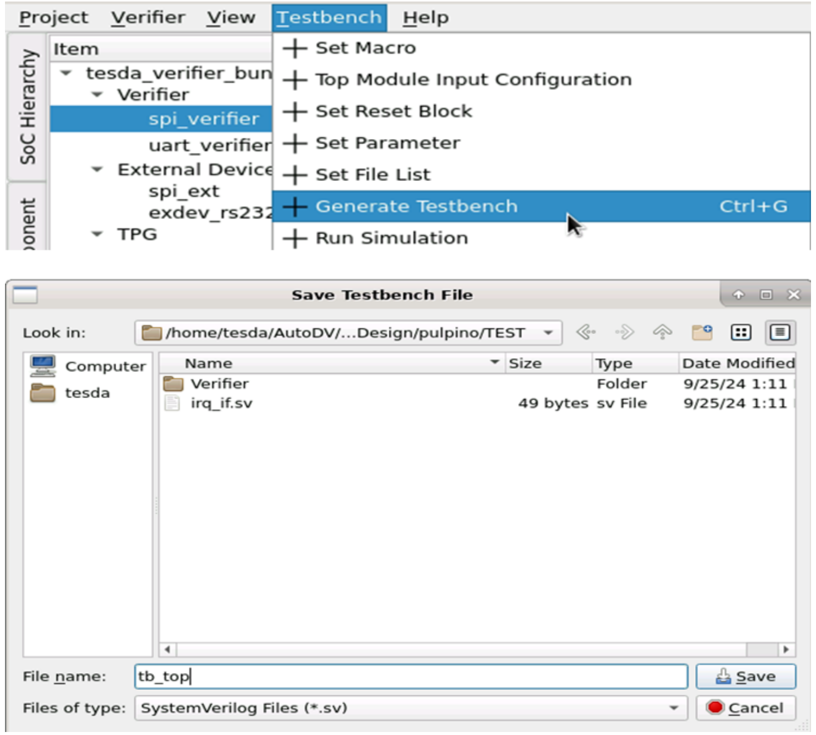
Reset Timing Setup

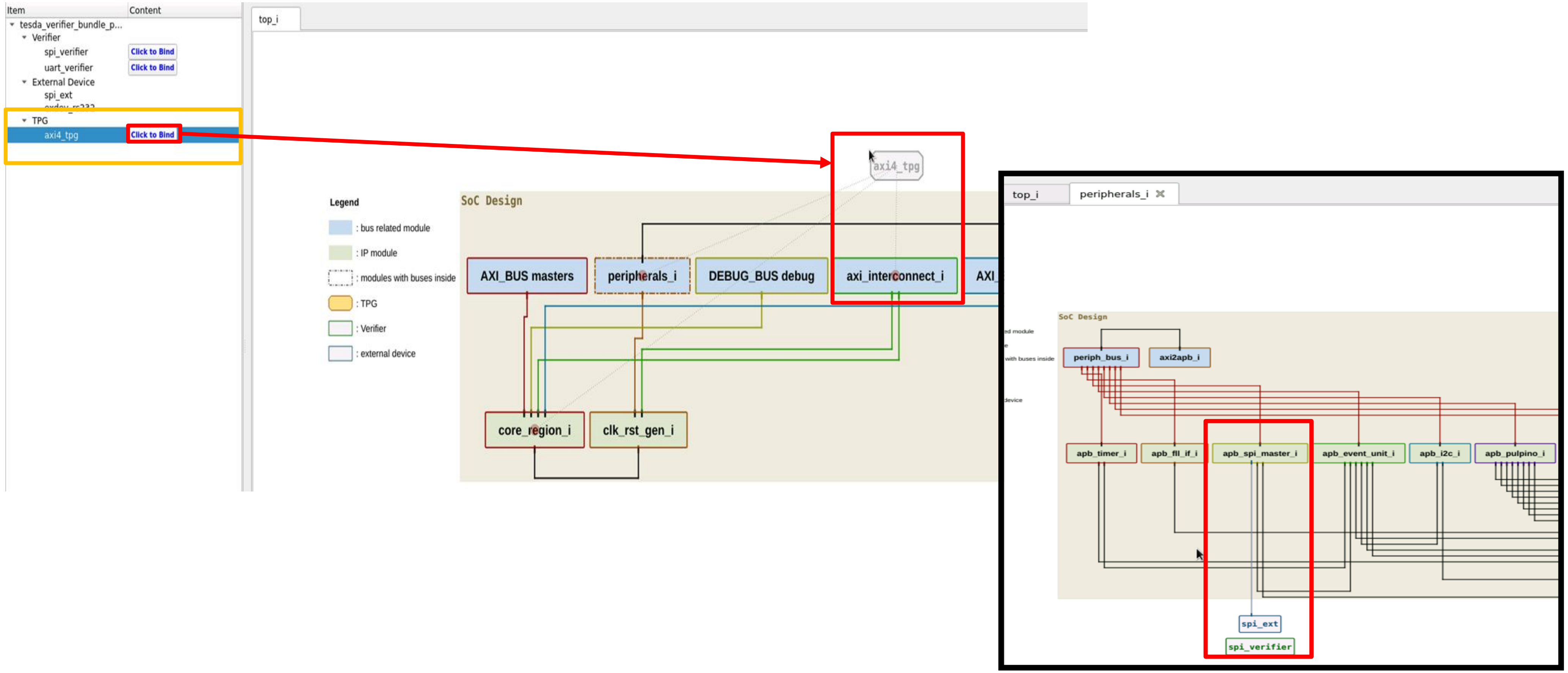


Instant Testbench Setup

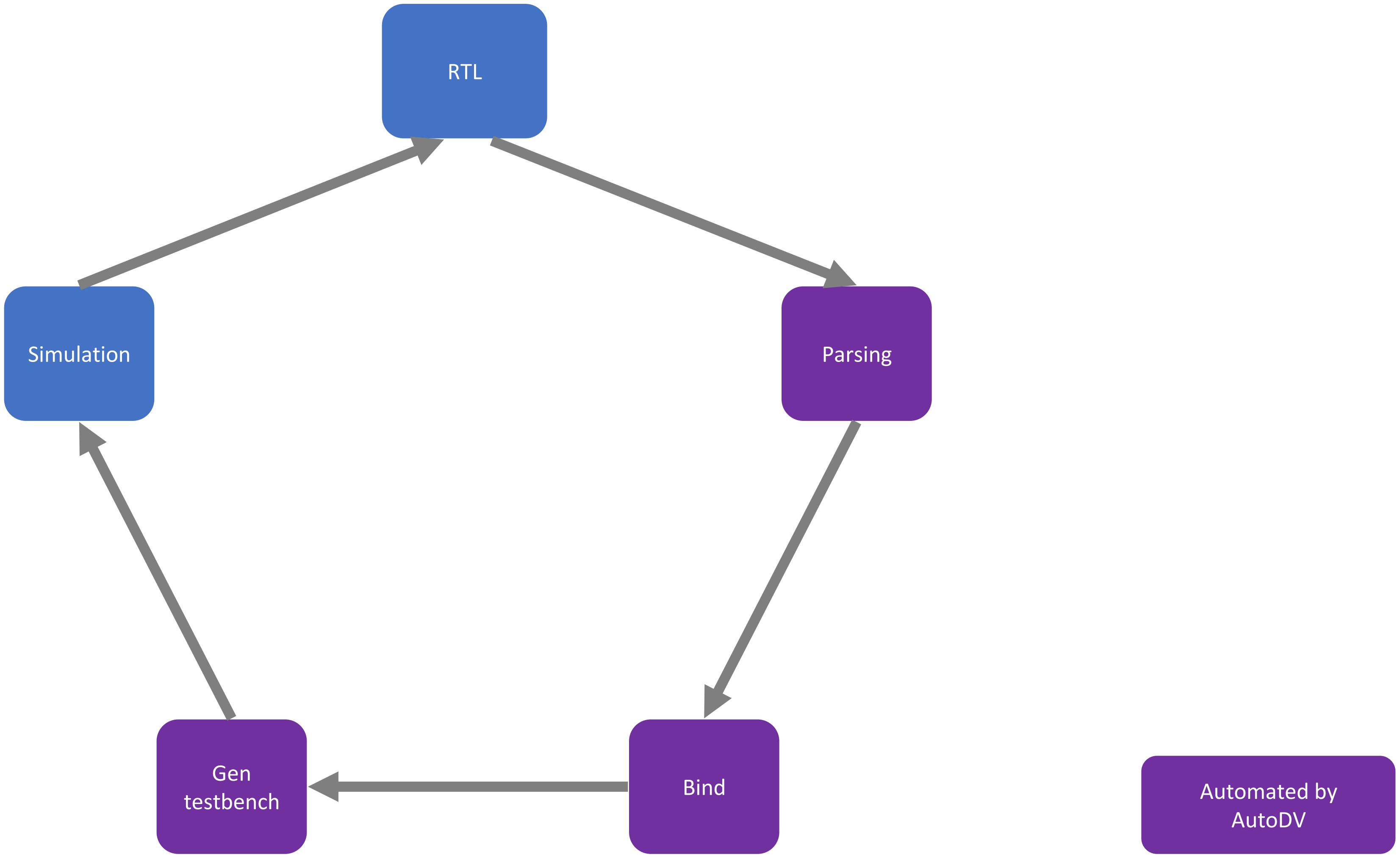


Generated Testbench

Knowledge Encapsulation



Fast turn-around time



AutoDV

Knowledge Encapsulation

Instant Testbench Setup

Fast Turn-around Time

Q&A