AI-DRIVEN DESIGN AND VERIFICATION

Scaling Complexity with (→) Intelligence

11 SEPTEMBER 2025

///DVCON INDIA 2025 | BENGALURU

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VLSI DESIGN ENGINEERING

SANDISK™

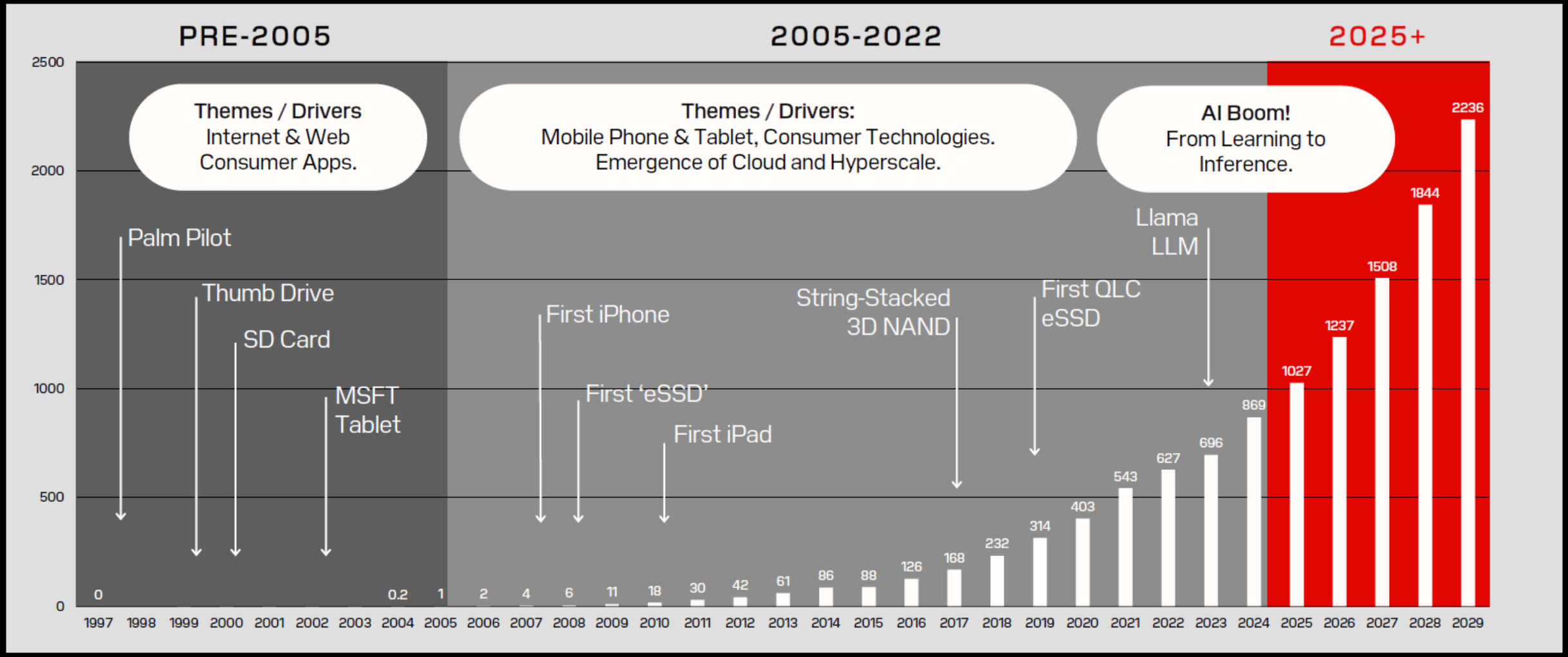
Disclaimers

FORWARD-LOOKING STATEMENTS

This presentation contains forward-looking statements within the meaning of federal securities laws, including, but not limited to, statements regarding expectations for Sandisk Corporation’s (the “Company’s”) products and technology; data growth and storage demand trends; and the availability, performance, potential and characteristics of the Company’s products and technologies. These forward-looking statements are based on management’s current expectations and are subject to risks and uncertainties that could cause actual results to differ materially from those expressed or implied in the forward-looking statements.

Key risks and uncertainties that could cause actual results to differ materially from those expressed or implied in the forward-looking statements include: risks related to the development and productization of High Bandwidth Flash; adverse changes in global or regional economic conditions, including the impact of evolving trade policies, tariff regimes and trade wars; volatility in demand for the Company’s products; pricing trends and fluctuations in average selling prices inflation; changes in interest rates and a potential economic recession; future responses to and effects of global health crises; the impact of business and market conditions; the impact of competitive products and pricing; the Company’s development and introduction of products based on new technologies and management of technology transitions; risks associated with strategic initiatives, including restructurings, acquisitions, divestitures, cost saving measures and joint ventures; risks related to product defects; difficulties or delays in manufacturing or other supply chain disruptions; our reliance on strategic relationships with key partners, including Kioxia Corporation; hiring and retention of key employees; the Company’s level of debt and other financial obligations; changes to the Company’s relationships with key customers or consolidation among our customer base; compromise, damage or interruption from cybersecurity incidents or other data system security risks; our reliance on intellectual property; fluctuations in currency exchange rates; actions by competitors; risks associated with compliance with changing legal and regulatory requirements; future material impairments in the value of our goodwill and other long-lived assets; our ability to achieve some or all of the expected benefits of the separation from Western Digital Corporation; and other risks and uncertainties listed in the Company’s filings with the Securities and Exchange Commission (the “SEC”), including the Registration Statement on Form 10, initially filed with the SEC on November 25, 2024, as further amended thereafter and declared effective on January 31, 2025, the Company’s Quarterly Report on Form 10-Q for the quarter ended December 27, 2024, as initially filed with the SEC on March 7, 2025 and amended on March 17, 2025, and the Company’s Quarterly Report on Form 10-Q for the quarter ended March 28, 2025, as filed with the SEC on May 12, 2025, to which your attention is directed. You should not place undue reliance on these forward-looking statements, which speak only as of the date hereof, and the Company undertakes no obligation to update or revise these forward-looking statements to reflect new information or events, except as required by law.

FLASH HAS TRANSFORMED THE WORLD



SOURCE: SANDISK ANALYSIS; TECH INSIGHTS DATA.

SANDISK™

SANDISK (→)

Innovative Flash solutions and advanced memory technologies

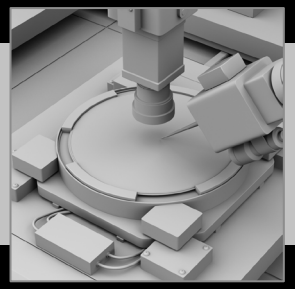
DECADES OF FLASH INNOVATION

12,000+ EMPLOYEES WORLDWIDE

DEEP MEMORY & STORAGE SEMICONDUCTOR EXPERTISE

OVER 11,000 TOTAL PATENT ASSETS WORLDWIDE

OUR STRATEGIC FOUNDATION



INNOVATION

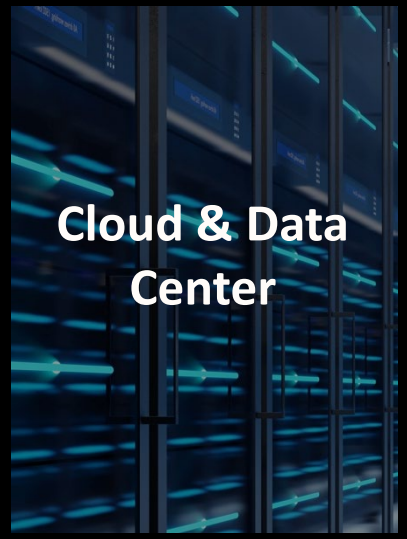
SCALE

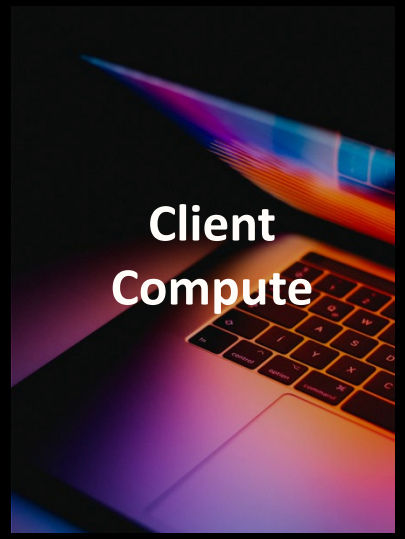
AGILITY

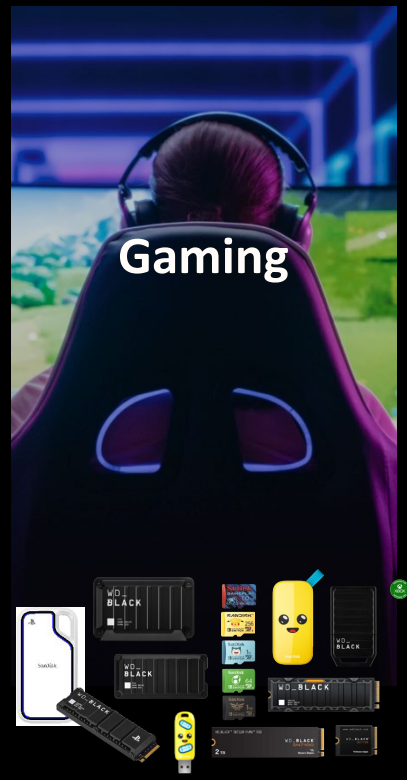
RESILIENCE

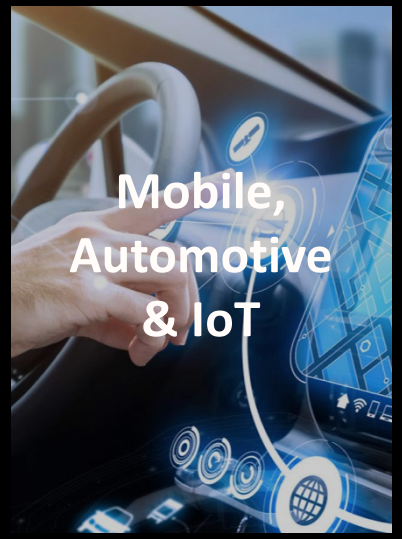
ONE OF THE INDUSTRY’S BROADEST PORTFOLIOS

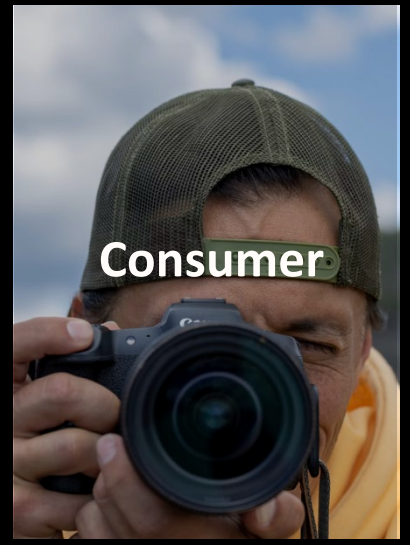
From Cloud Providers to Enterprises and Consumers

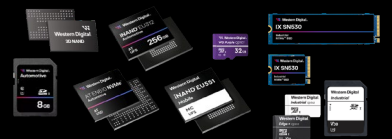












MEMORY TECHNOLOGY

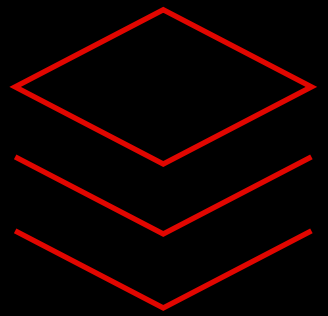
What We Do

OUR Mission

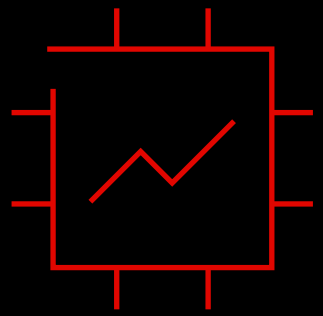
(→) We invent, develop, and deliver best in class Flash Memory to solve people’s data storage challenges

OUR VISION

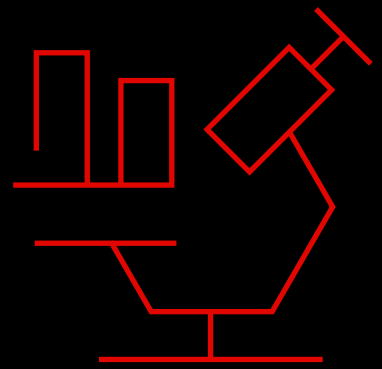
(→) We lead the digital world transformation through continuous innovation in flash memory solutions



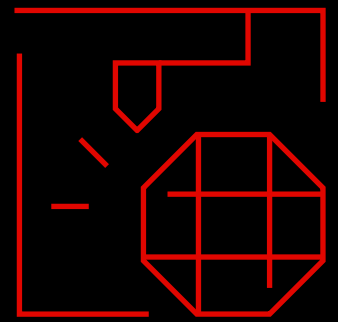
MEMORY DESIGN



TECHNOLOGY DEVELOPMENT



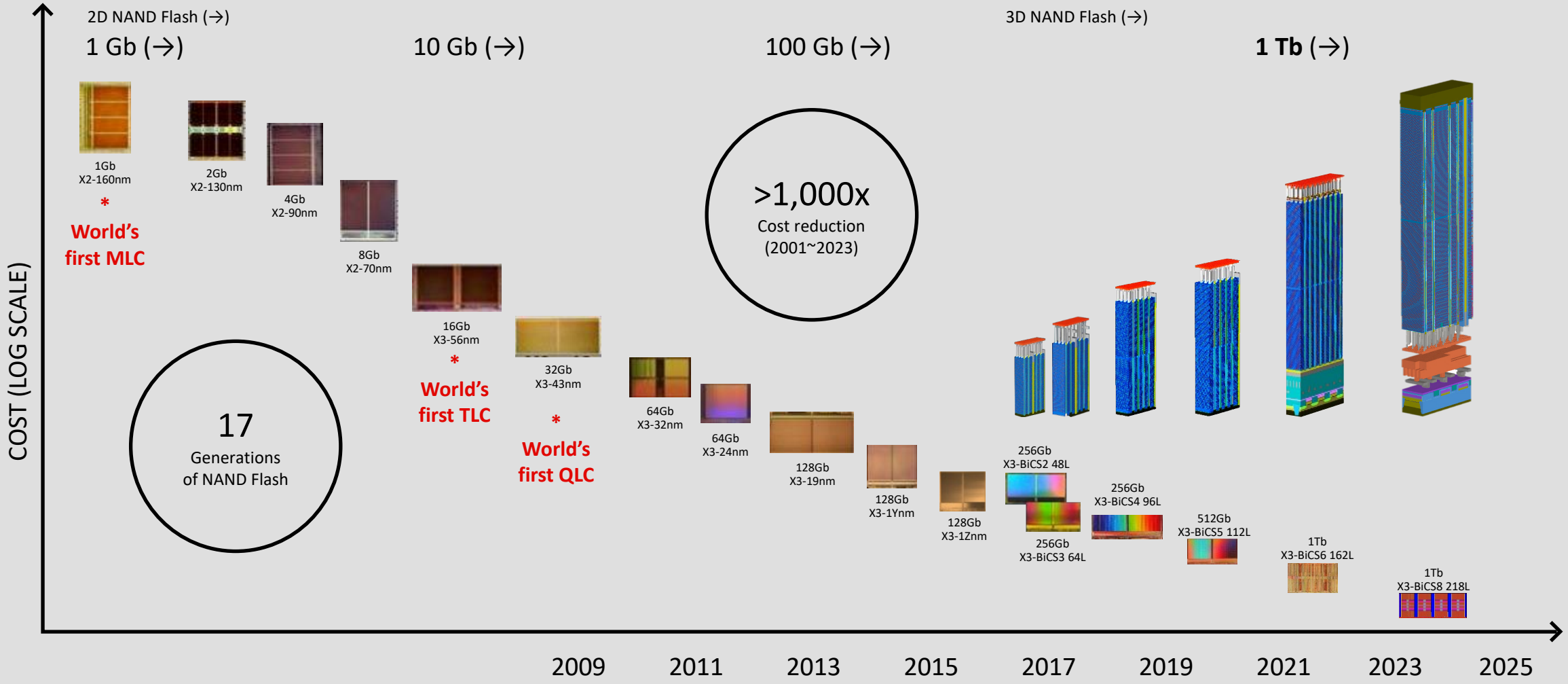
QUALIFICATION & FAILURE ANALYSIS



PRODUCTIZATION & TEST

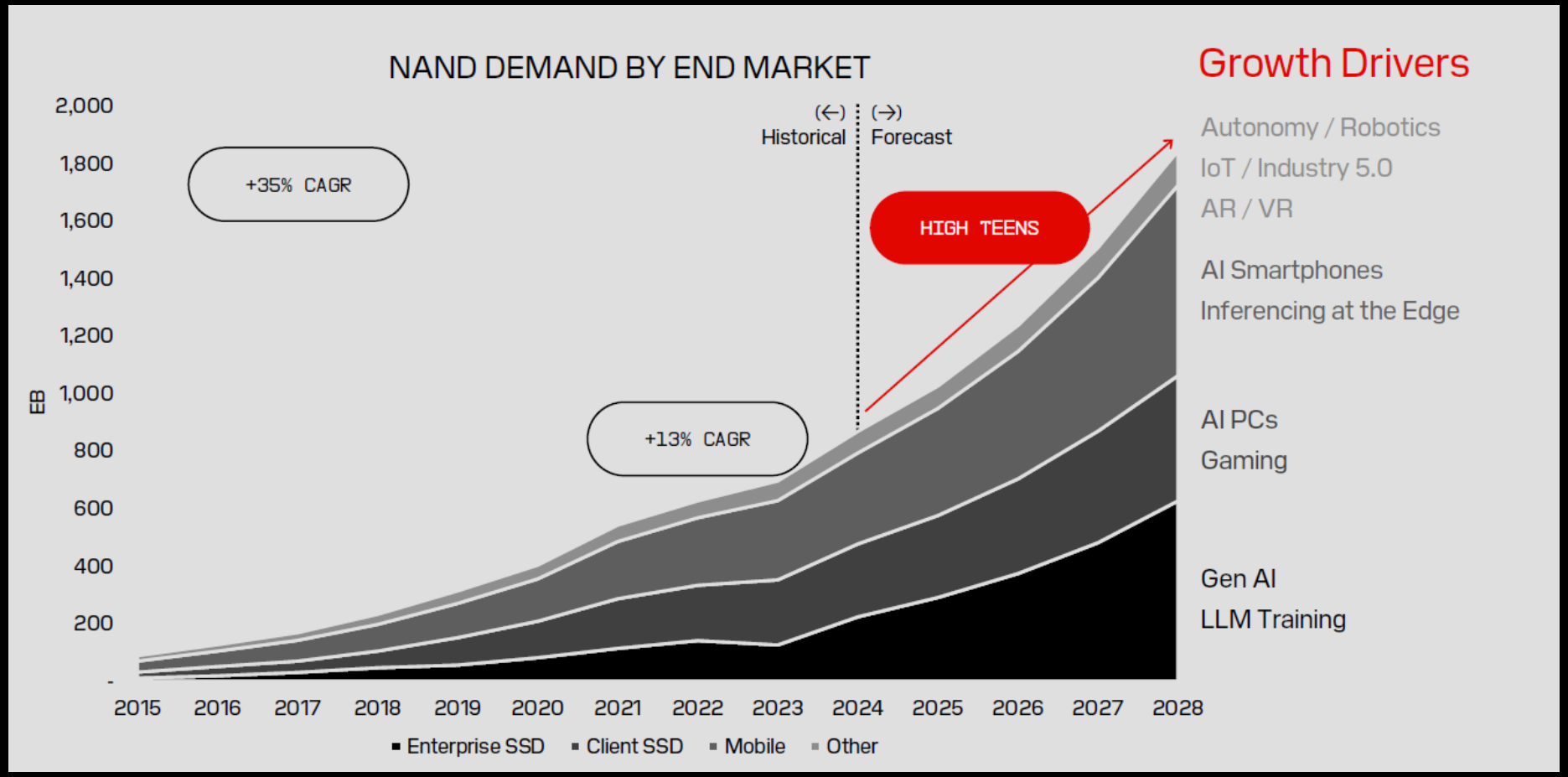
SANDISK™

OUR LEGACY OF INNOVATION



NOTE: IMAGES ARE NOT TO SCALE.

AI Driven Demand for Storage is Accelerating



SOURCE: TECH INSIGHTS NAND MARKET REPORT Q4 2024.

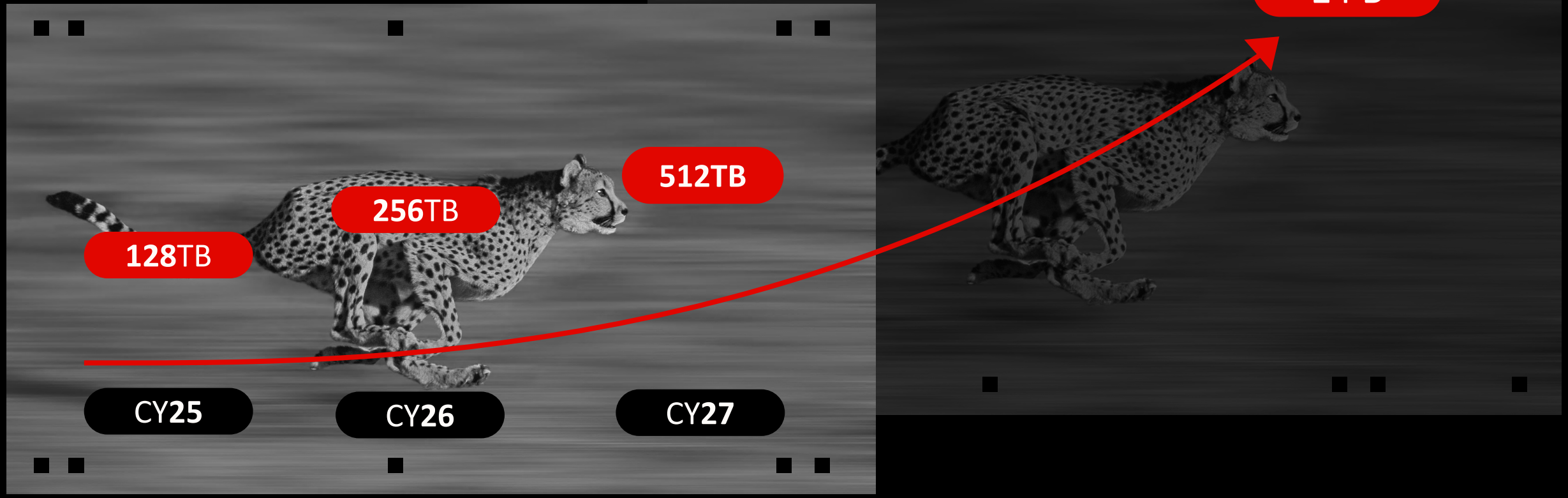
How do we keep up with this?

NAND Technology & Products Designed to Support Various Features Across Different Market Applications

- Capacity
- Performance
- Power

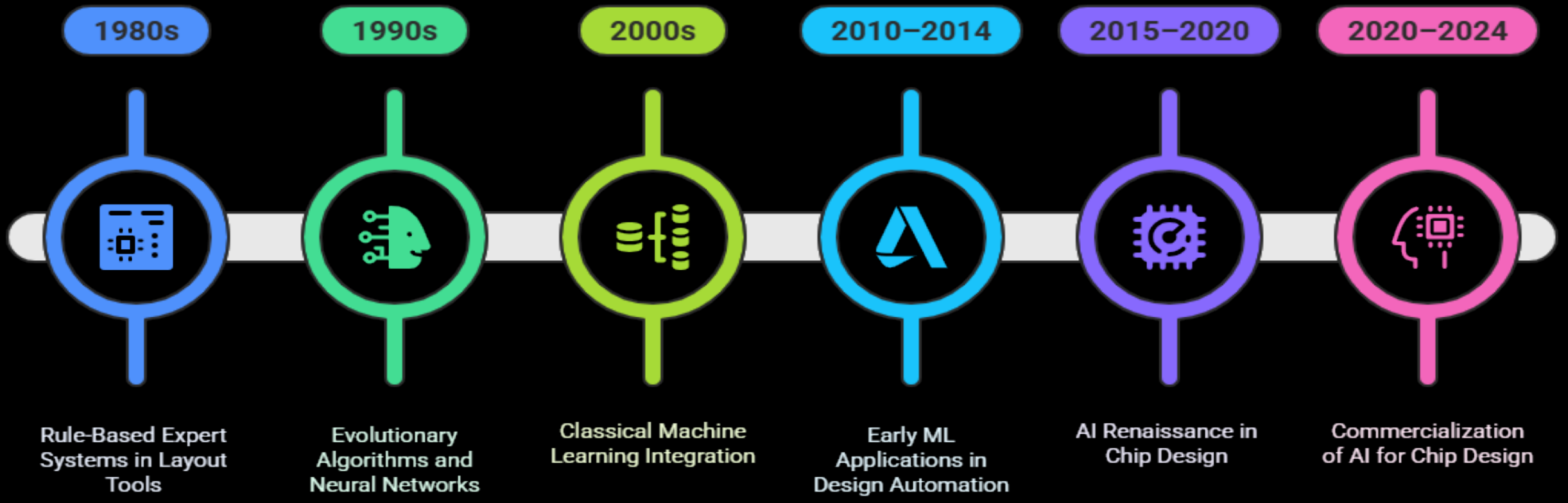
The world is getting closer to PB SSDs

..and we need to scale Development → Test at the same rate



So, CAN AI HELP??

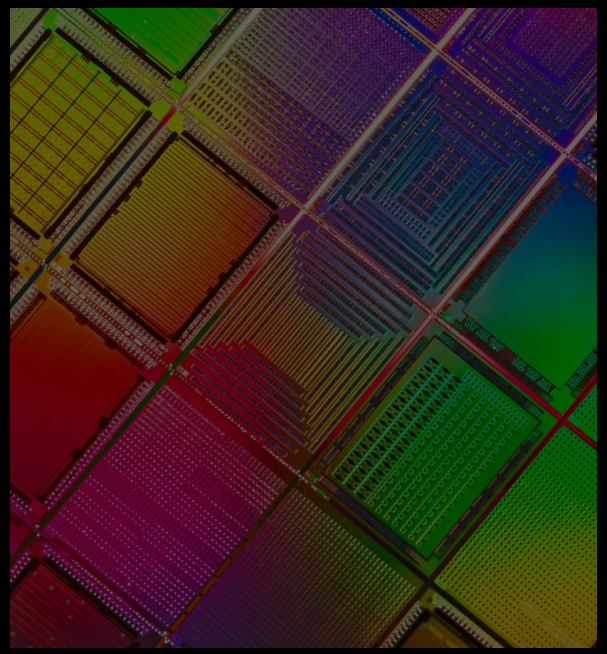
Evolution of AI/ML in VLSI Chip Design



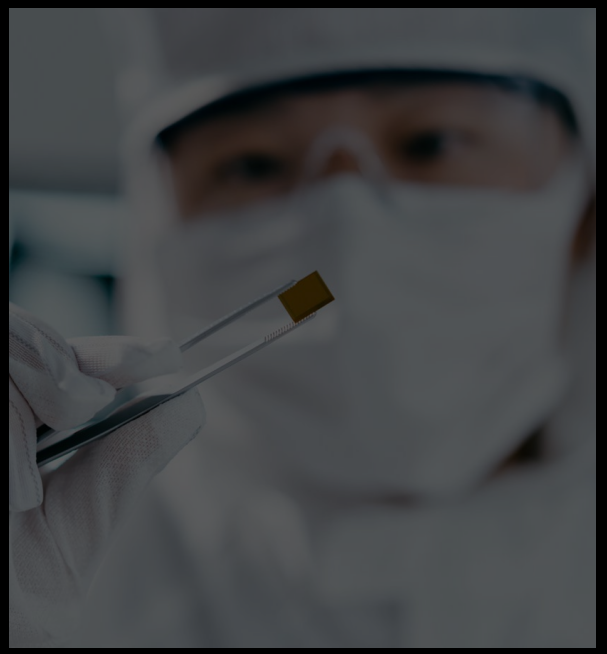
SANDISK™

The Design & Development Cycle
Opportunities to Leverage AI

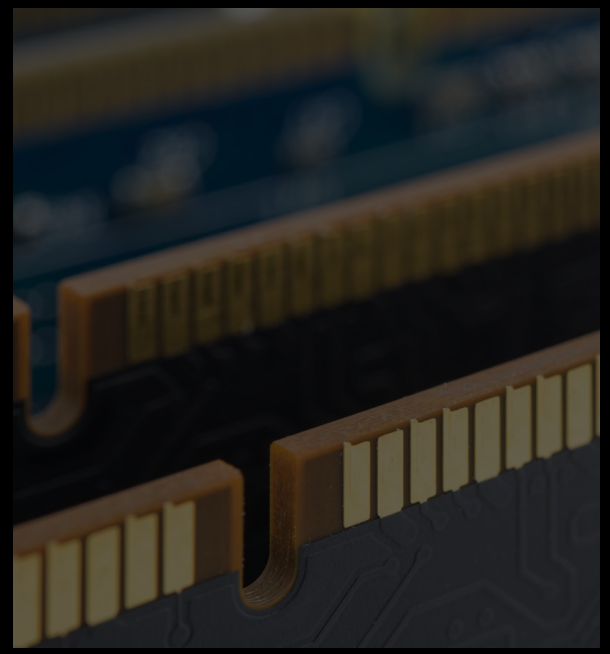
TIME & COST → TIME → COST



MEMORY DESIGN



PRE & POST SI VALIDATION



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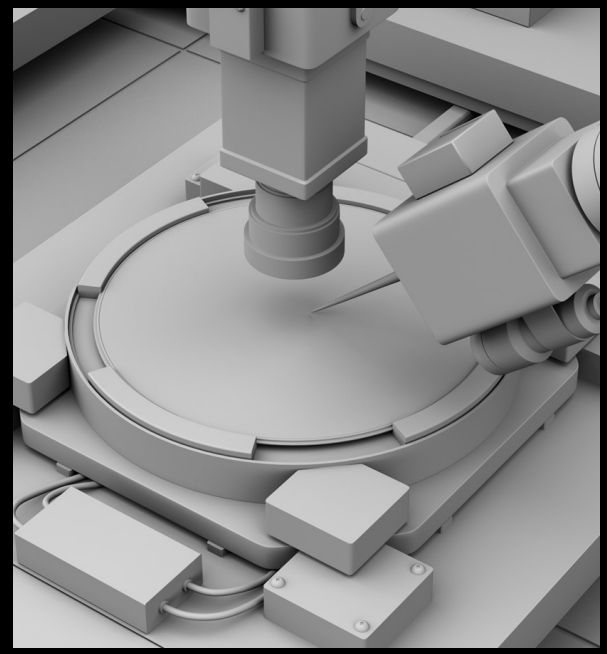


PRODUCTION TEST & YIELD MANAGEMENT

SANDISK™

Transforming Test Technology

(→) AI Assisted Manufacturing

(→) Maximize Bit Consumption

(→) Internal Test Platforms

Wafer Level

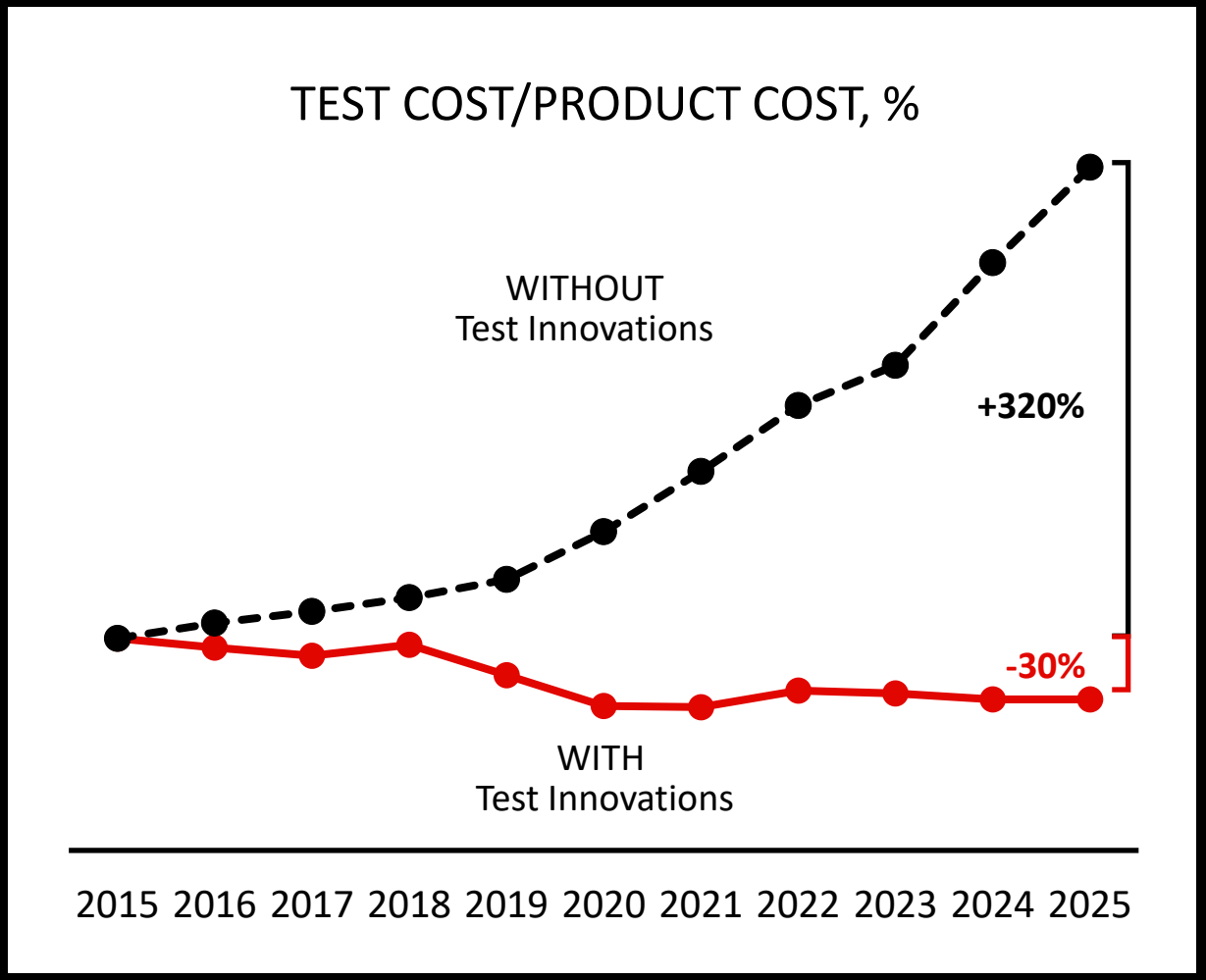
Gross Die Per Wafer, Die Capacity, Yield Interface Speed (WHS)

Component Level

Packaged Die Capacity, IF Speed

System Level

Drive Capacity, Host Interface



SOURCE: SANDISK TESTING.

The Design & Development Cycle
Opportunities to Leverage AI

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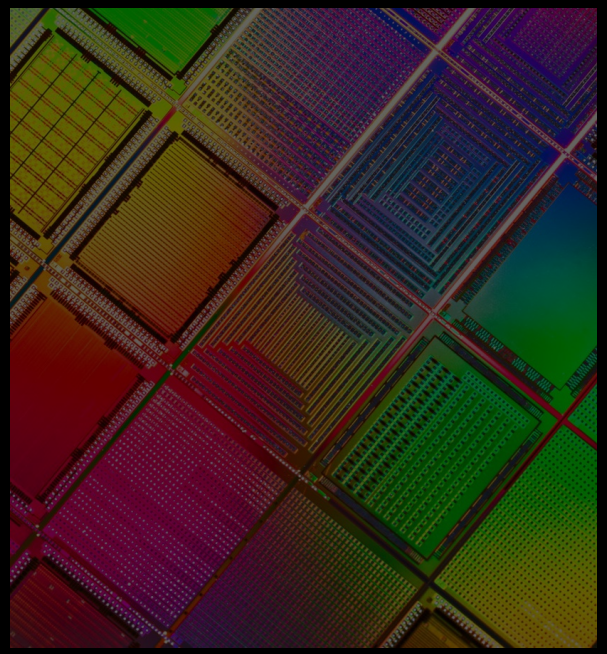

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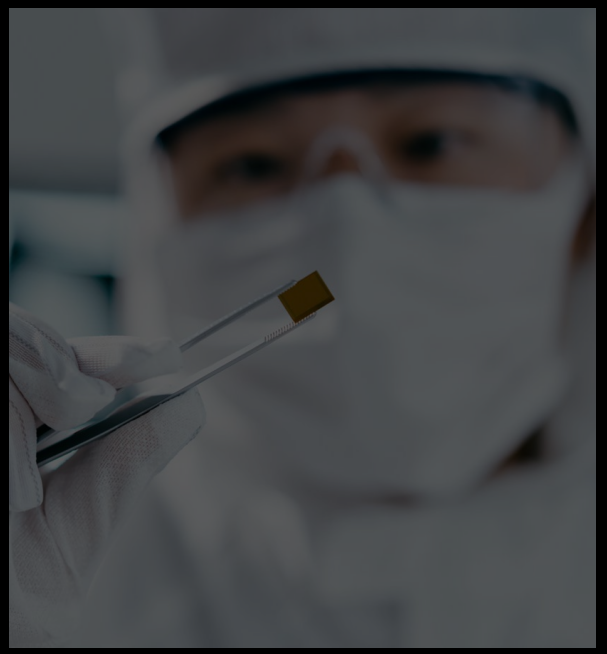

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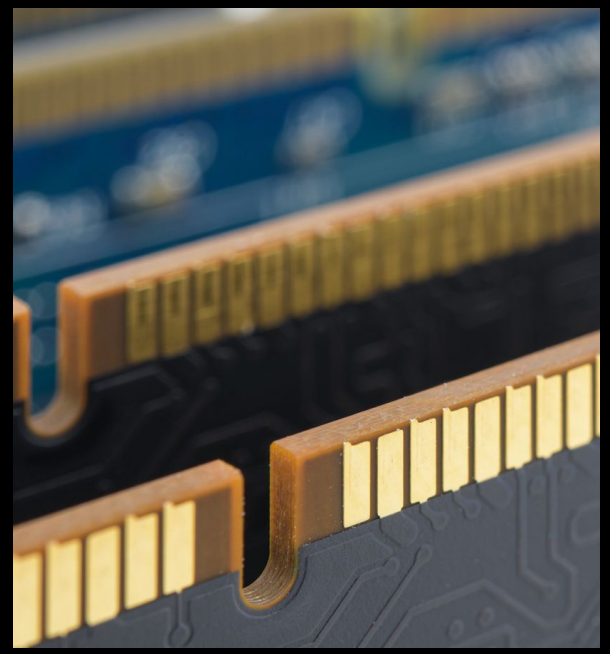

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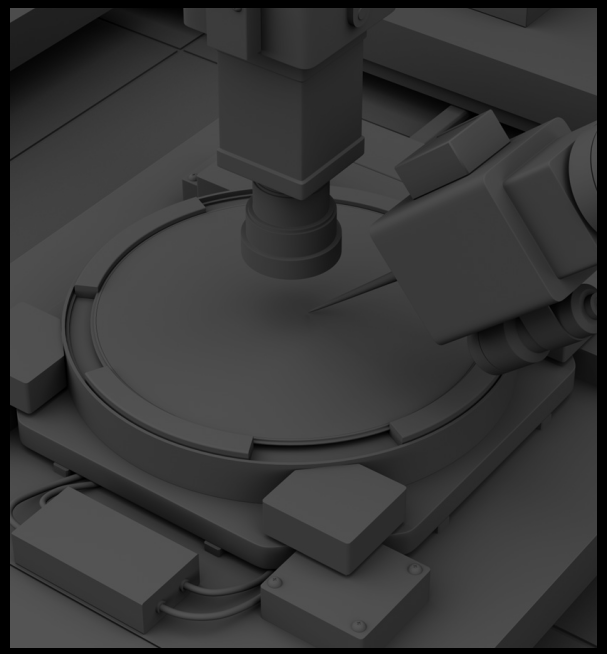

PRODUCTION TEST & YIELD MANAGEMENT

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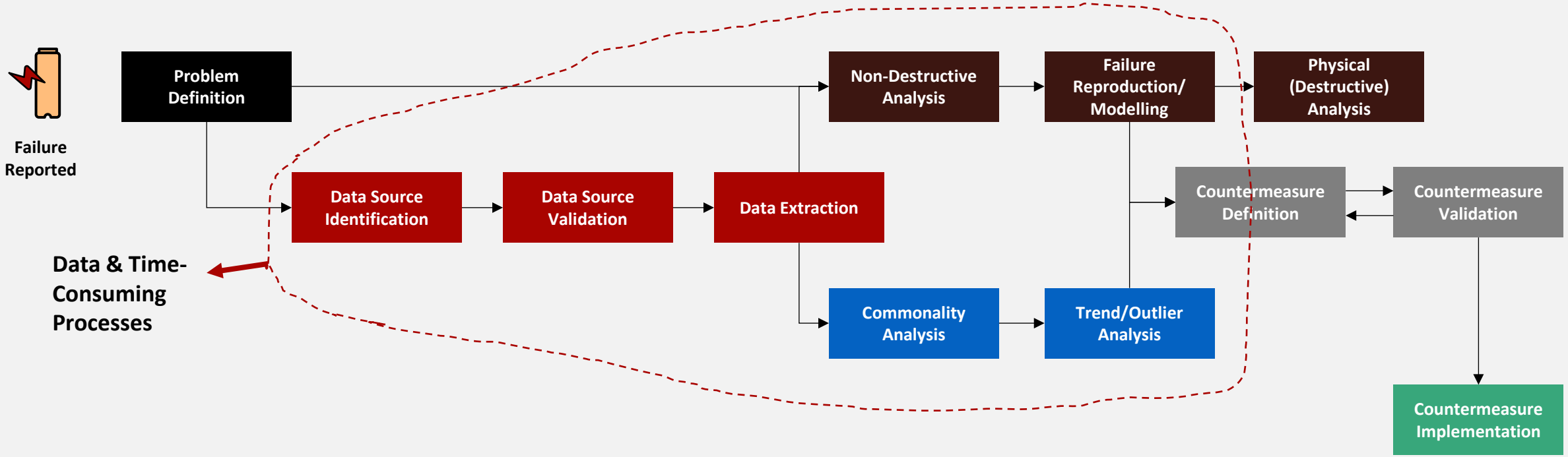
Failure Analysis Process



Challenges

- Highly complex process interactions & multiple data sources (text, logs, images, graphs etc.) in current systems
- Specialized & Proprietary Knowledge Domains
- Unstructured historical data sources → The farther you go, the more unstructured the data is

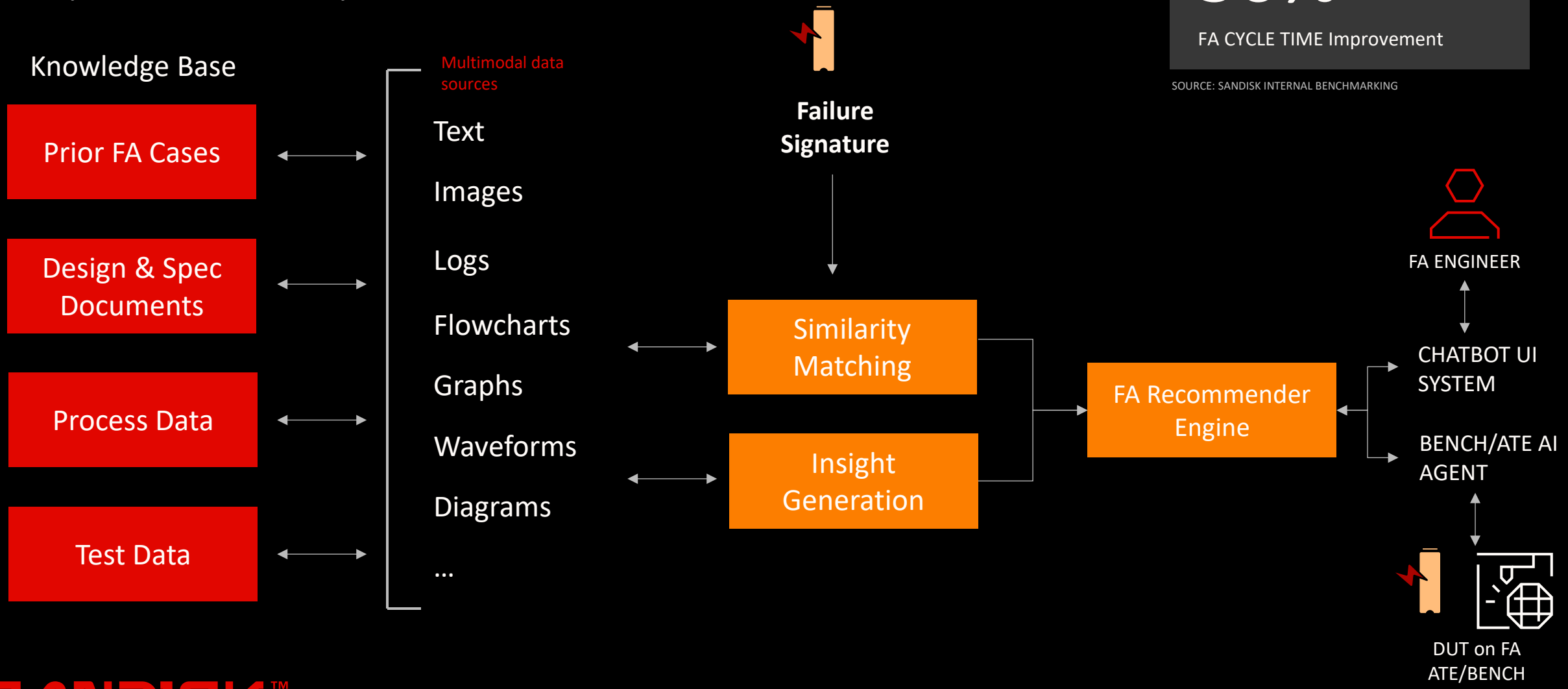
Rapid Failure Analysis

GenAI powered Failure Analysis Acceleration

30%+

FA CYCLE TIME Improvement

SOURCE: SANDISK INTERNAL BENCHMARKING



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The Design & Development Cycle
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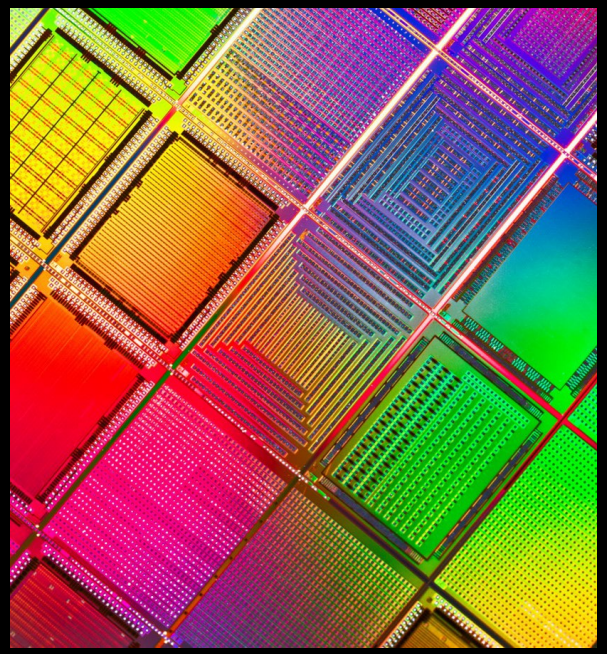
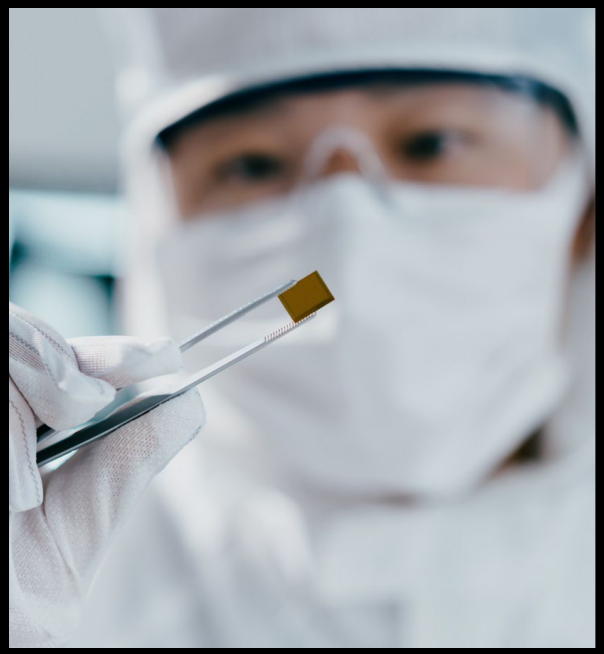


MEMORY DESIGN



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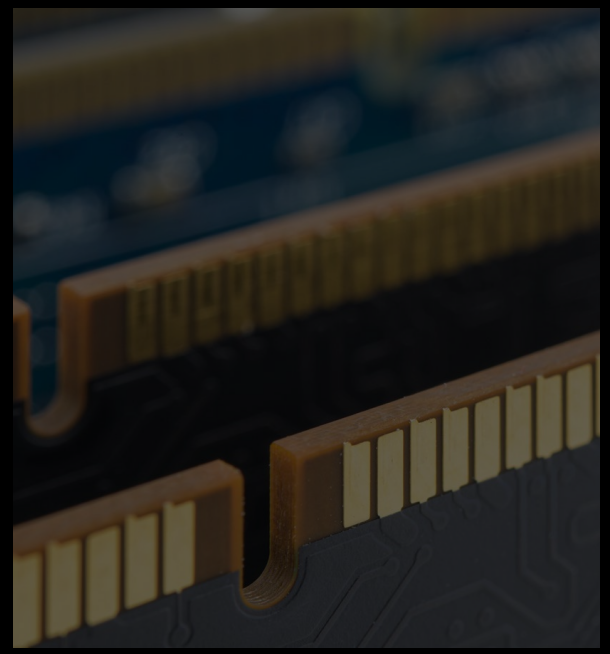

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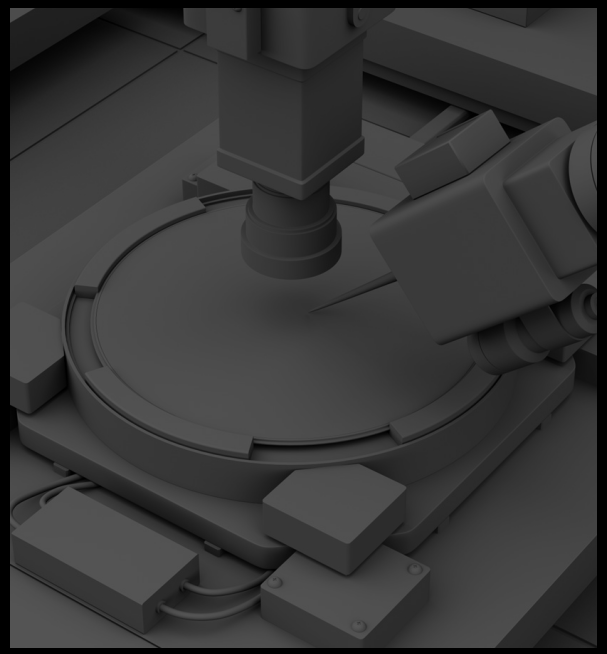

PRODUCTION TEST & YIELD MANAGEMENT

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AI Augmented Smart Verification

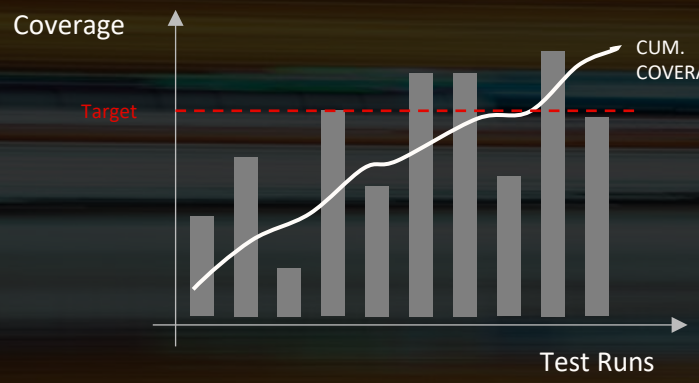
Enable Faster Coverage Detection & Intelligent FA

80%+

CODE COVERAGE with <20% TEST CASES

SOURCE: SANDISK INTERNAL BENCHMARKING

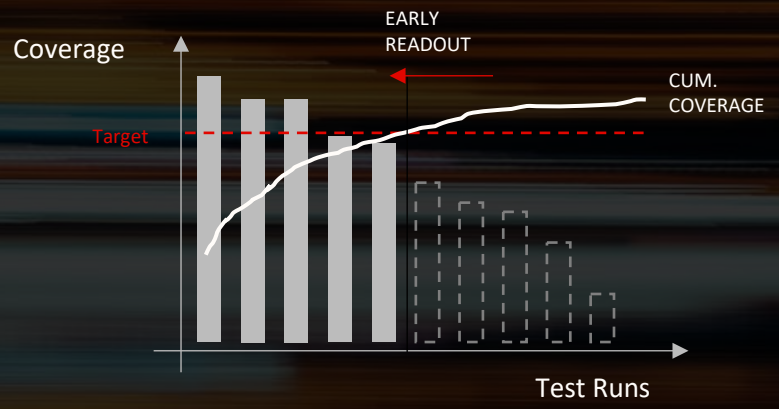
Traditional Verification



(→) Randomized Regressions tend to eventually achieve target coverage → But take longer duration/higher computation

(→) Design issues found later in the verification cycle costs precious time

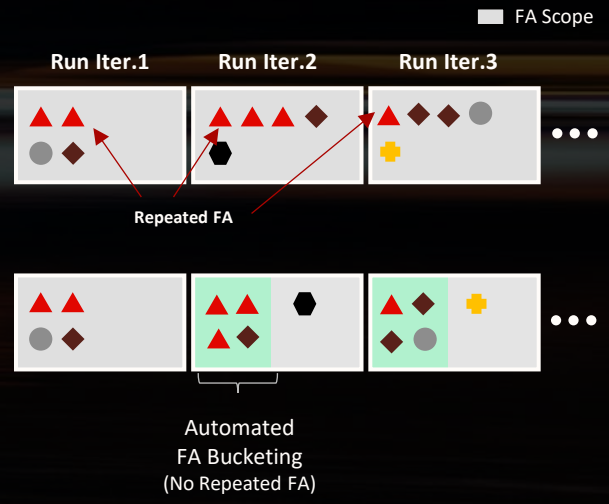
Smart Verification



(→) Smart Verification utilizes AI based ranking algorithms mapped to affected changes and prioritize test cases for faster readout

(→) Early readout enables faster design changes & time saving on verification

Intelligent FA



(→) AI driven classification of failures and automated closure

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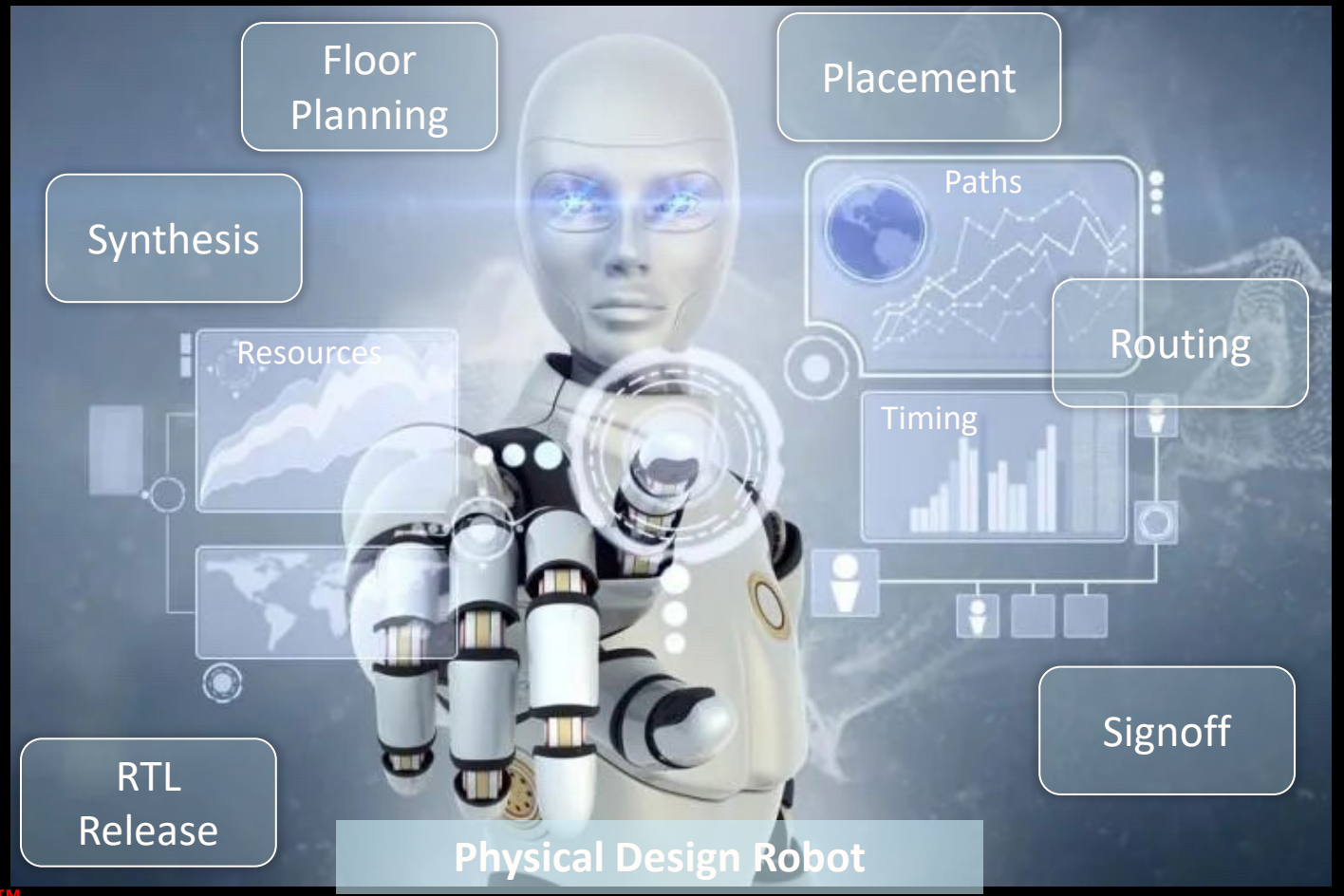
Autonomous Physical Design

Enable Automated & Efficient Layout

Goal Significantly Reduce Typical Physical Design Time & Cost

Learns from years of past PD data across multiple projects and process nodes

+ Continuous Learning from its own autonomous PD execution (RL)



Searches through 1000s of setup variables per tool for optimized setting to achieve QoR target

Predicts results for thousands of designs, narrowing down setup for high probability targets

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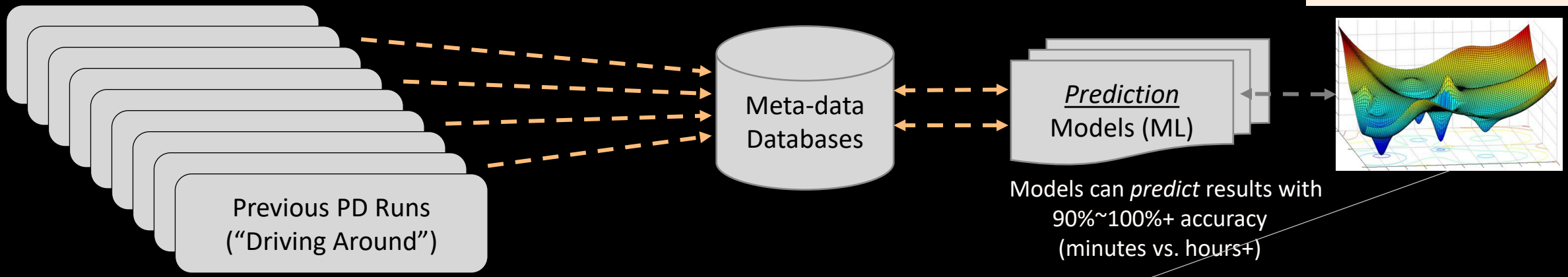
Autonomous Physical Design

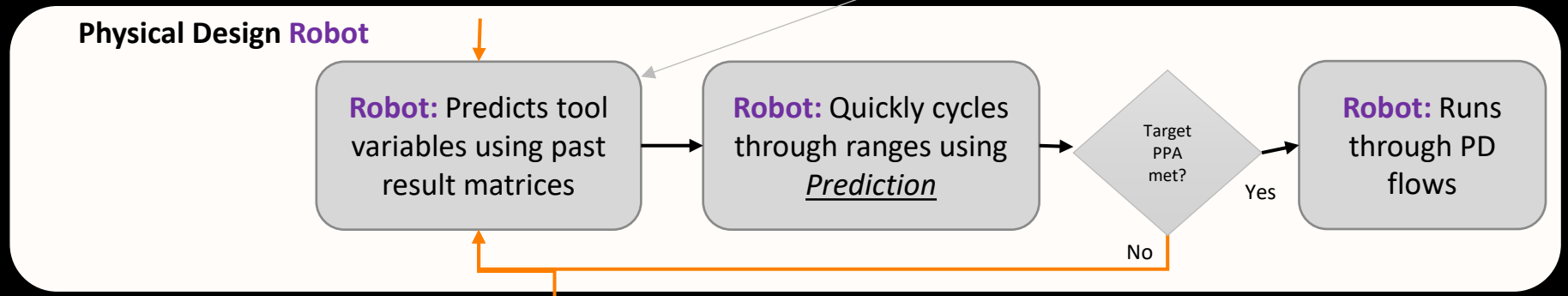
Architecture

Maps QoR* to Multi-Dimensional Matrices



New PD Runs: Executing ("Inference" based)

Human: Design Target "Destination" (i.e. PPA)



Other Human Inputs

Benefits:

- High accuracy *Predicted* results save a lot of $ & time
- Robotic operator minimizes human intervention
- Faster convergence to target QoR* ('shift left')

*QoR = Quality of Results

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Autonomous Physical Design

Results

Design Name /Project	Design A/Project X	Design B/Project Y	Design C /Project Y
Release Version	V1	V2	V3 (tapeout version)
Instance Count	Small	Medium	Large
Area	Medium	Medium	Large

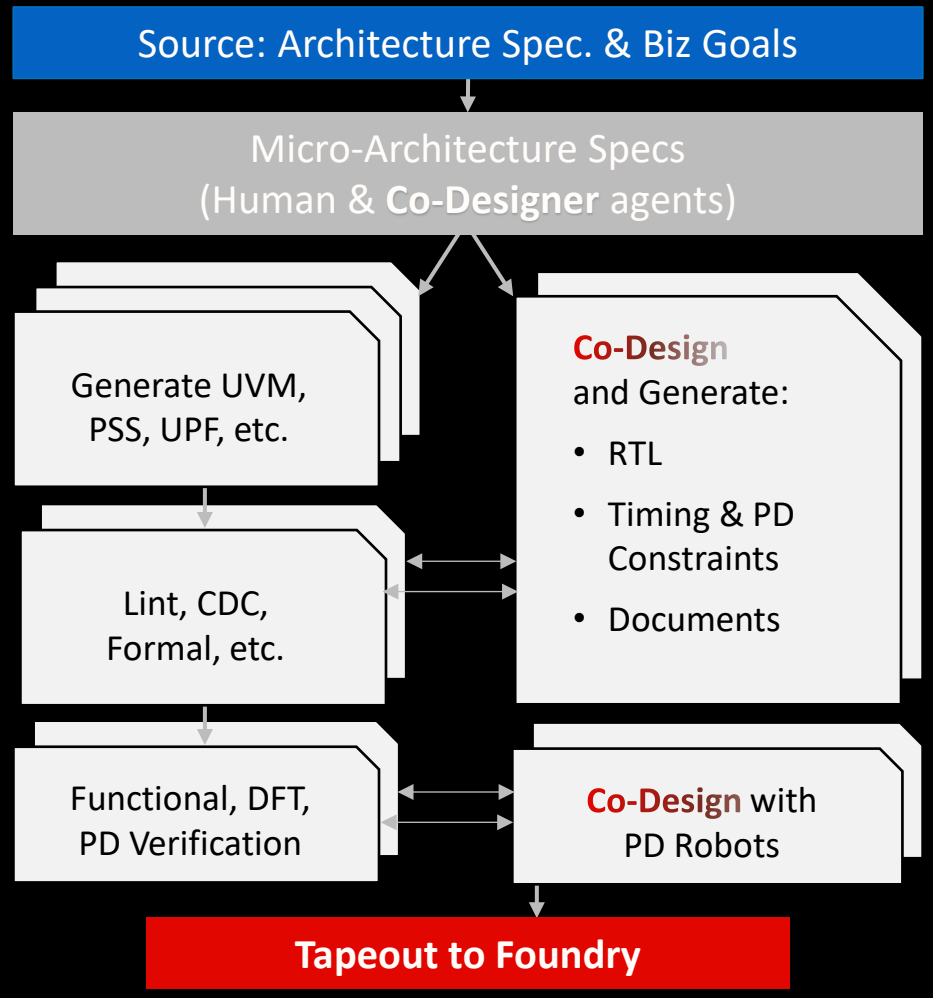
Metric	Improvement	Improvement	Improvement
Total Execution Time improvement for design	**29X**	**21X**	**12X**
Total License Usage for design (less runs to get same/better QoR)	**30X**	**20X**	**15X**
Disk Footprint for design (less runs to get same/better QoR)	**30X**	**20X**	**15X**
Timing QoR improvements for design	**Up to 97% better**	**Up to 18% better**	**Up to 24% better**

SOURCE: SANDISK INTERNAL BENCHMARKING – PRESENTED IN ISCAS 2025

SANDISK™

(→) THE FUTURE IS FOR AI, BY AI

Co-Designer GenAI agents to support various design steps with Human designers



Train a New VLSI Language (e.g. UVM, PSS, UPF) using Prompt Engineering

"Translates" spec to RTL with hyper-trained LLM inference model

Reconfirms accuracy through standard tool flows

Uses co-pilots/co-designers for remaining steps

Autonomous Cross Verification

Autonomous PD Robots

Human Verification, Inspections and Design Reviews using analytics

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