Accellera Overview

October 2024

Dennis Brophy | Accellera Vice Chair

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SYSTEMS INITIATIVE™

2024
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
INDIA

Accellera Systems Initiative

Our Mission

To provide a platform in which the electronics industry can collaborate to innovate and deliver global Electronic Design Automation and IP standards that improve design and verification productivity for today's advanced integrated circuits and embedded systems. In addition, we strive to promote the widespread adoption of these standards.

PORTABLE STIMULUS
SYSTEM C™
SystemVerilog
VHDL
UVM
IP-XACT™
SystemRDL™
UPF UNIFIED POWER FORMAT

Broad Industry Support

Corporate Members

- AMD
- arm
- cādence
- ERICSSON
- Ford
- intel
- NXP
- QUALCOMM
- SIEMENS
- ST
- SYNOPSYS

Start-Up and University

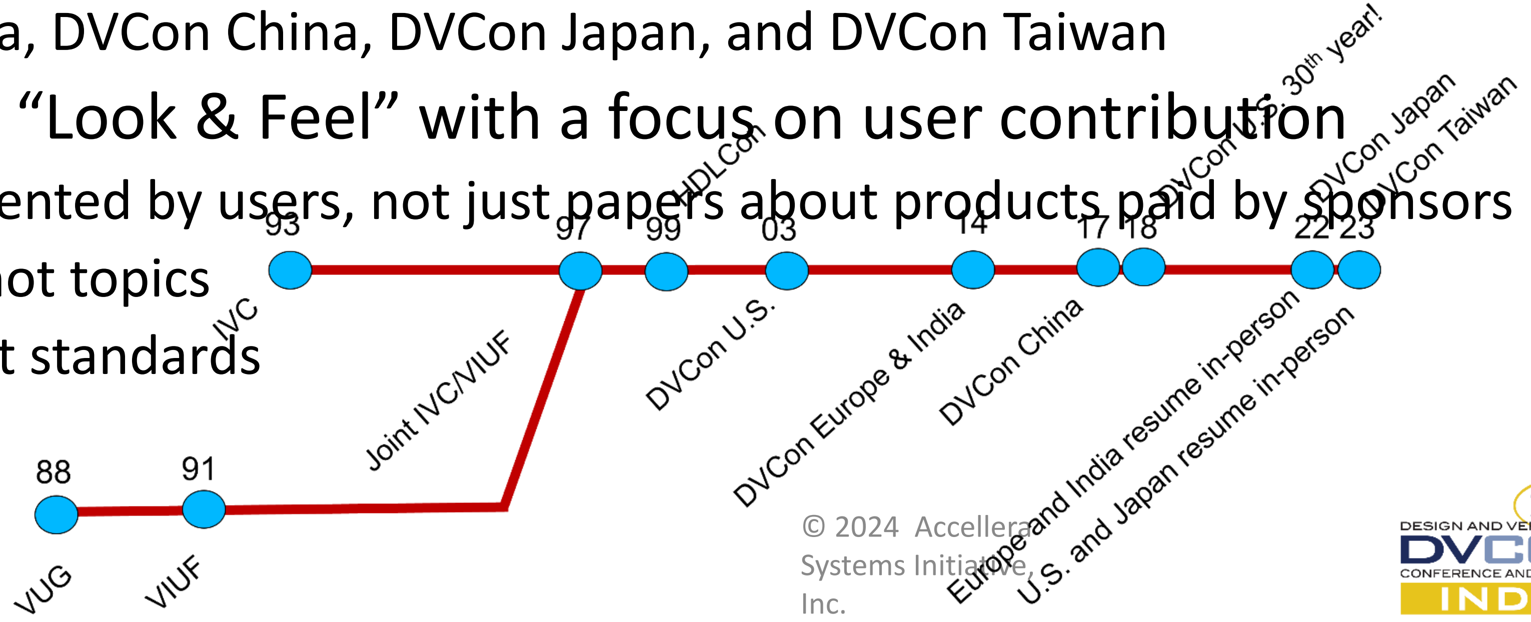
- SCIENCES SORBONNE UNIVERSITÉ
- KÄRNTEN University of Applied Sciences
- MACHINEWARE
- 合见工软 UNIVISTA

Associate Members

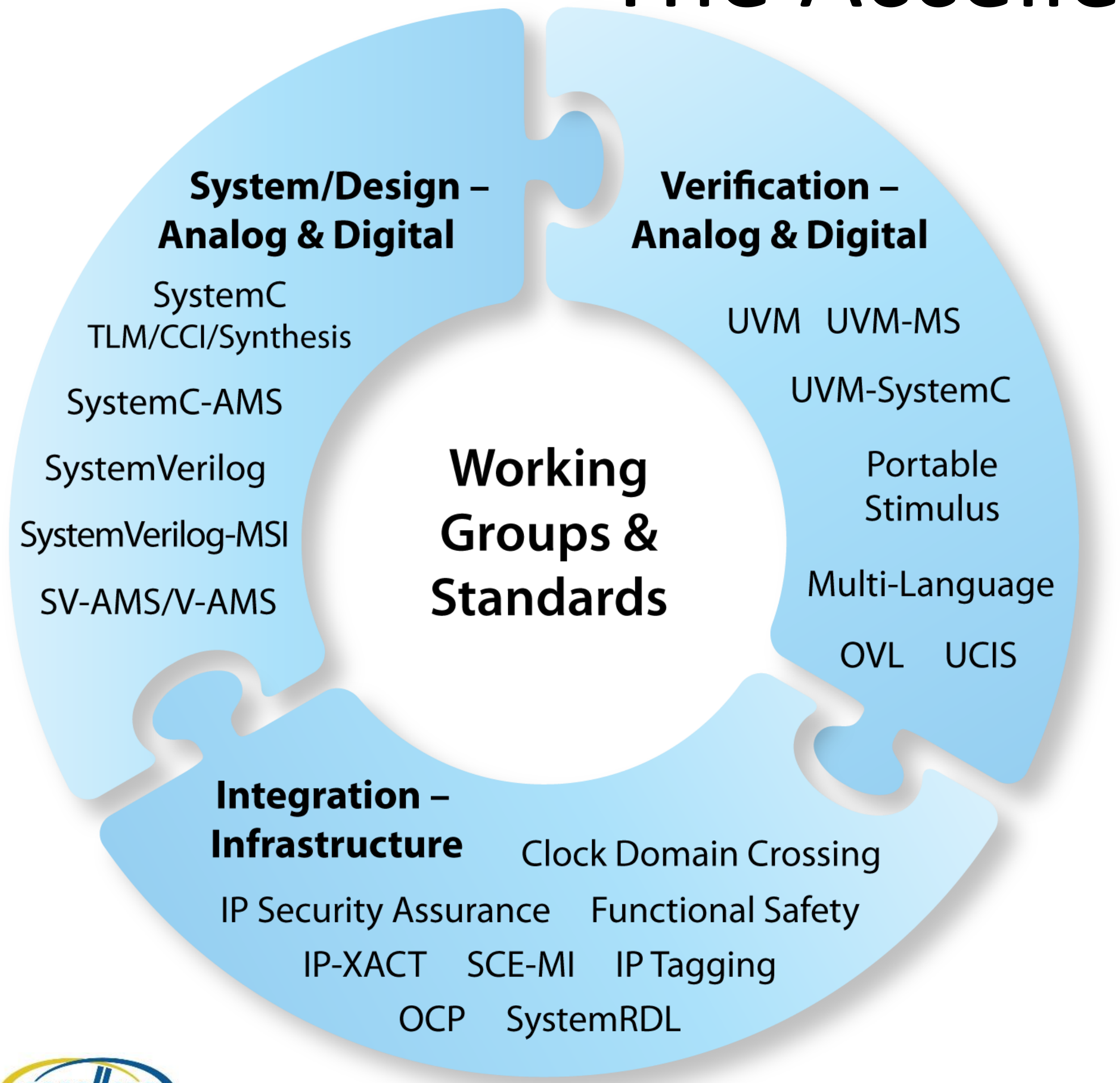
- ADVANTEST
- AGNISYS
- ALDEC THE DESIGN VERIFICATION COMPANY
- AMIQ
- ANALOG DEVICES
- ARTERIS IP
- ausdia
- Blue Pearl Software
- BOSCH Invented for life
- BREKER
- COSEDA technologies
- DOULOS
- Fraunhofer IIS
- HUAWEI
- infineon
- MARVELL
- MICROCHIP
- Microsoft
- NVIDIA
- RENESAS
- S2C EDA SOLUTIONS
- scientific analog
- Vayavya Labs Pvt. Ltd.
- Verific Design Automation
- verilab
- Western Digital

Accellera and DVCon

- Accellera has been successfully sponsoring Design & Verification Conference & Exhibition in the US for over 35 years
  - Original events had different names and were tied to VHDL International and Open Verilog International
  - Eventually VHDL and Verilog-focused groups merged into a single conference and became DVCon in 2003
- Global expansion started in 2014
  - DVCon Europe, DVCon India, DVCon China, DVCon Japan, and DVCon Taiwan
- Every DVCon has a similar "Look & Feel" with a focus on user contribution
  - Papers written by and presented by users, not just papers about products paid by sponsors
  - Panel sessions on current hot topics
  - Tutorials related to relevant standards



The Accellera Ecosystem



Working Groups & Standards

System/Design – Analog & Digital

SystemC TLM/CCI/Synthesis

SystemC-AMS

SystemVerilog

SystemVerilog-MSI

SV-AMS/V-AMS

Verification – Analog & Digital

UVM UVM-MS

UVM-SystemC

Portable Stimulus

Multi-Language

OVL UCIS

Integration – Infrastructure

Clock Domain Crossing

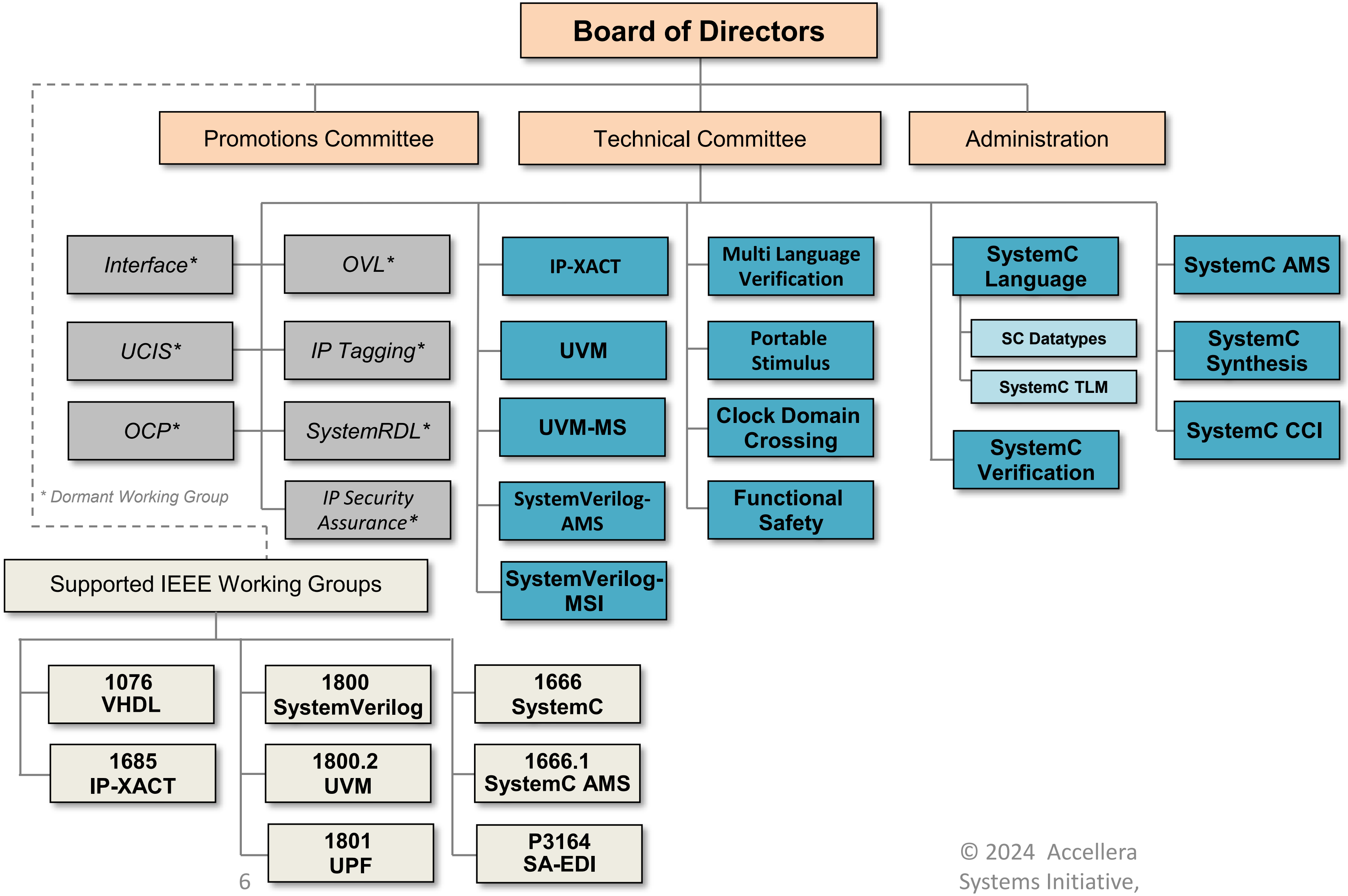
IP Security Assurance Functional Safety

IP-XACT SCE-MI IP Tagging

OCP SystemRDL

Helping you bring all the pieces together

Accellera Systems Initiative



Accellera Standards and Activities

Current Standards and Supplemental material

Standards

- Intellectual Property (IP) Tagging 1.0
- IP-XACT - Update of IEEE P1685 and Vendor Extensions
- Multi-Language (ongoing)
- Open Verification Library (OVL) 2.8.1
- Portable Stimulus 2.1
- Security Annotation for Electronic Design Integration 1.0
- Standard Co-Emulation Modeling Interface (SCE-MI) 2.3
- SystemVerilog-AMS & SystemVerilog-MSI (ongoing)
- SystemRDL 2.0
- SystemC Analog Mixed-Signal (AMS) 2.3
- SystemC Configuration, Control & Inspection (CCI) 1.0
- SystemC Core Language 2.3.3 (includes TLM 2.0)
- SystemC Synthesis 1.4.7
- Unified Coverage Interoperability Standard (UCIS) 1.0
- Universal Verification Methodology 2020-1.1
- Verilog-AMS 2023

Supplemental material

- IP-XACT Users Guide
- SystemC AMS Users Guide and Application Examples
- SystemC CCI 1.0 Proof-of-Concept Kit
- SystemC Reference Implementation and Regression Test Suite 3.0
- SystemC Core Language and Examples
- SystemC Verification Library (SCV) 2.0.1
- UVM 2020.3.0 Reference Implementation
- UVM-SystemC Library 1.0-beta4

Whitepapers

- IP Security Assurance
- Functional Safety

IEEE Standards Access at No Charge

- Accellera relationship with the IEEE-SA
- Accellera will release 10 standards for 10 years under an extended IEEE Get program

n 187,000 downloads to date!

IEEE GET EDA Standards

Download IEEE Standards

http://ieeexplore.ieee.org/Xplore/home.jsp

- or find links to specific standards at -

www.accellera.org/downloads/ieee

Recent Accellera News

- Portable Test & Stimulus Standard 3.0 – August 2024
- Federated Simulation Standard Working Group Formed – June 2024
- Verilog-AMS 2023 Standard – March 4, 2024
- IEEE 1800™-2023 Availability in GET Program – March 4, 2024
- Distinguished Service Award - Shalom Bresticker – February 26, 2024
- SystemC 3.0.0 Fully Compatible with IEEE 1666™-2023 – February 5, 2024
- SystemVerilog Mixed-Signal Interface (MSI) Working Group – February 7, 2024

Looking Forward

- Clock Domain Crossing Working Group
  - Team on fast track to develop standard
- SystemC Synthesis Working Group Restarted
  - New Chair - Frederic Doucet, Qualcomm
- Functional Safety Working Group
  - LRM to be released later this year
- SystemVerilog Mixed-Signal Interface (MSI) Working Group
  - Recently approved as formal working group
  - Planning to release standard this year

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Presenters Bio

- Ashish Soni
  - Ashish Soni is working as a Principal Engineer at ST Microelectronics, where he leads the Front-End methodology activities within the Automotive Group.
  - With nearly 18 years of experience, he specializes in Digital Design, CAD flows, and Methodology development.
  - He also leads ST’s global static checks forums, focusing on Hierarchical CDC, RDC, and Lint.
  - He has authored over 15 papers on static checks and Hierarchical flows, presented at various international conferences and internal forums.
  - He holds a BTech degree in Electronics and is an alumnus of IIM, Indore. His hobbies include reading books, traveling, and he is an avid car enthusiast

Presenters Bio

- Jebin Vijai Mohandas
  - 19+ Years of experience in RTL Design and Verification Methodologies
  - Verification using Specman, OVM, UVM, Verdi, Coverage and Simulators
  - Qualification of Test Bench objectively using Certitude
  - Established flow and methodology to validate and effective debug of assertions and DPPM reduction.
  - Currently working on Methodology focusing on RTL Quality Static checks in Clock Domain Crossing, Reset Domain crossing, RTL Linting, Low Power, RTL Constraints Verification, Power Estimation and Formal.

Presenters Bio

- Manish Bhati
  - Manish is working as an Application Consultant with Siemens EDA and prior to Siemens he has worked with Synopsys.
  - His EDA experience as Application Engineer spans over 14 years. He is an expert in Lint and CDC/RDC verification technology.
  - He has also worked as FPGA/ASIC designer for 4 years. Manish is active in writing papers for DVCON and has published 6 papers in DVCON US/Europe/India in last 3 years.

Presenters Bio

- Suman Chalana:
  - Suman is currently working as a Principal Engineer/manager at Qualcomm India Private Limited. She has 16+ Years of work experience in VLSI Front end flows eg: Static Verification(CDC, Lint, RDC) Automotive flow development, Synthesist, FV.
  - Currently she is working as Static Verification Lead in CAD team, Qualcomm India Private Limited, leading Static verification methodology / tool-flow deployment globally. Along with Static, she is also driving & managing the team for overall automotive GCAD charter worldwide.
  - She is Qualcomm Accellera CDC work group lead. She has written more than 10+ papers in various external/internal conferences and won Best Poster/Paper awards.
  - She also serves as reviewer and member of technical program committees of IEEE-Win Contech conferences & internal conferences.
  - She has done her M.Tech in VLSI & Embedded system, from IIIT Hyderabad.

Presenters Bio

- Devender Pal Khari:
  - Devender is a seasoned industry professional having more than two and a half decades of experience in EDA Product Development
  - As Engineering Director at Agnisys, he is currently leading the R&D team providing direction and guidance to the team besides being involved hands on himself
  - He has been an active contributor in Accellera IP-XACT and CDC Working groups and have represented the working groups in different DVCon events
  - He completed his M.E. in Computer Science from BITS – Pilani (1997)

Bridging the Gap: Standardizing CDC and RDC Closure with Interoperable Abstract Models

Accellera CDC Working Group

Authors

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SYSTEM DEVELOPMENT WITH CERTAINTY

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Jan HAYEK
BOSCH

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JAPAN

Standardizing CDC and RDC abstract models

Accellera CDC Working Group

Anupam BAKSHI	Ping YEUNG	Chetan CHOPPALI SUDARSHAN	Farhad AHMED	Iredamola OLOPADE	Sean O'DONOHUE	Bill GASCOYNE	Kranthi PAMARTHI
AGNISYS SYSTEM DEVELOPMENT WITH CERTAINTY	NVIDIA	MARVELL	SIEMENS	intel	SYNOPSYS	Blue Pearl Software	RENESAS

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2024

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CONFERENCE AND EXHIBITION

UNITED STATES

SAN JOSE, CA, USA
MARCH 4-7, 2024

Hierarchical CDC and RDC closure with standard abstract models

Accellera CDC Working Group

Ping YEUNG	Chetan CHOPPALI SUDARSHAN	Farhad AHMED	Iredamola OLOPADE	Sean O'DONOHUE	Bill GASCOYNE	Kranthi PAMARTHI	Anupam BAKSHI
NVIDIA	MARVELL	SIEMENS	intel	SYNOPSYS	Blue Pearl Software	RENESAS	AGNISYS SYSTEM DEVELOPMENT WITH CERTAINTY

2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE 10 YEAR ANNIVERSARY

Making the impossible possible: CDC and RDC closure with abstracts from different tools

Accellera CDC Working Group

Diana KALEL
Jean-Christophe BRIGNONE

Farhad AHMED

Eldad FALIK
Jebin Mohandes

Jerome AVEZOU

Bill GASCOYNE

Kranthi PAMARTHI

ST SIEMENS intel SYNOPSYS Blue Pearl Software RENESAS accellera SYSTEMS INITIATIVE

Presenter Introduction

- Companies
  - Ashish Soni
    - Principal Engineer at ST Microelectronics
    - 18+ years of experience
    - Leading the Front-End methodology activities within the Automotive Group
  - Jebin Vijai
    - Methodology expert at Intel
    - 19+ years of experience
    - Expert in RTL Design and Verification Methodologies
  - Suman Chalana
    - Principal Engineer/manager at Qualcomm
    - 16+ years of experience
    - Leading static verification methodology / tool-flow deployment globally
    - driving & managing the team for overall automotive GCAD charter worldwide

- EDA Vendors
  - Devender Khari
    - Engineering Director at Agnisys
    - 26+ years of experience
    - Leading R&D team developing solutions for spec to SoC development
  - Manish Bhati
    - Application Consultant with Siemens EDA
    - 18 years of experience
    - Expert in Lint and CDC/RDC verification technology

Agenda

	Topic	Slide update/create	Presenter	Time
#0	**Accellera updates**		Dennis Brophy	5m
#1	**CDC-RDC**			55m
	CDC-RDC Basic Knowledge	Bill Gascoyne (Blue Pearl), Jan Hayek (Bosch)	Ashish Soni (ST Micro)	10m
	Setup Constraints & Verification	Ping Yeung (Nvidia)	Jebin Vijai (Intel)	10m
	Structural CDC/RDC	Chetan Choppali Sudarshan (Marvell)	Suman Chalana (Qualcomm)	10m
	CDC Assertion-Based Verification	Kranthi Pamarthi (Renesas Electronics)	Manish Bhati (Siemens EDA)	10m
	CDC-RDC Hierarchical Flow	Farhad Ahmed (Siemens EDA), Ashish Soni (ST Micro)	Ashish Soni (ST Micro)	10m
	Q & A			10m
#2	**Accellera CDC**			20m
	Standard	Iredamola Olopade (Intel)	Jebin Vijai (Intel)	3m
	Format	Devender Khari (Agnisys)	Devender Khari (Agnisys)	3m
	Output	Sean O'Donohue (Synopsys), Joachim Voges (Infineon)	Devender Khari (Agnisys)	3m
	Assertion	Kranthi Pamarthi (Renesas Electronics)	Manish Bhati (Siemens EDA)	3m
	Testing	Farhad Ahmed (Siemens EDA)	Suman Chalana (Qualcomm)	3m
	Training	JC Brignone, Diana Kalel (ST Micro)	Ashish Soni (ST Micro)	3m

- Synchronous vs. asynchronous clocks
- Problems related to Clock Domain Crossing (CDC)
- CDC Synchronization
- Problems related to Reset Domain Crossing (RDC)
- RDC Synchronization

1.1 CDC-RDC BASIC KNOWLEDGE:

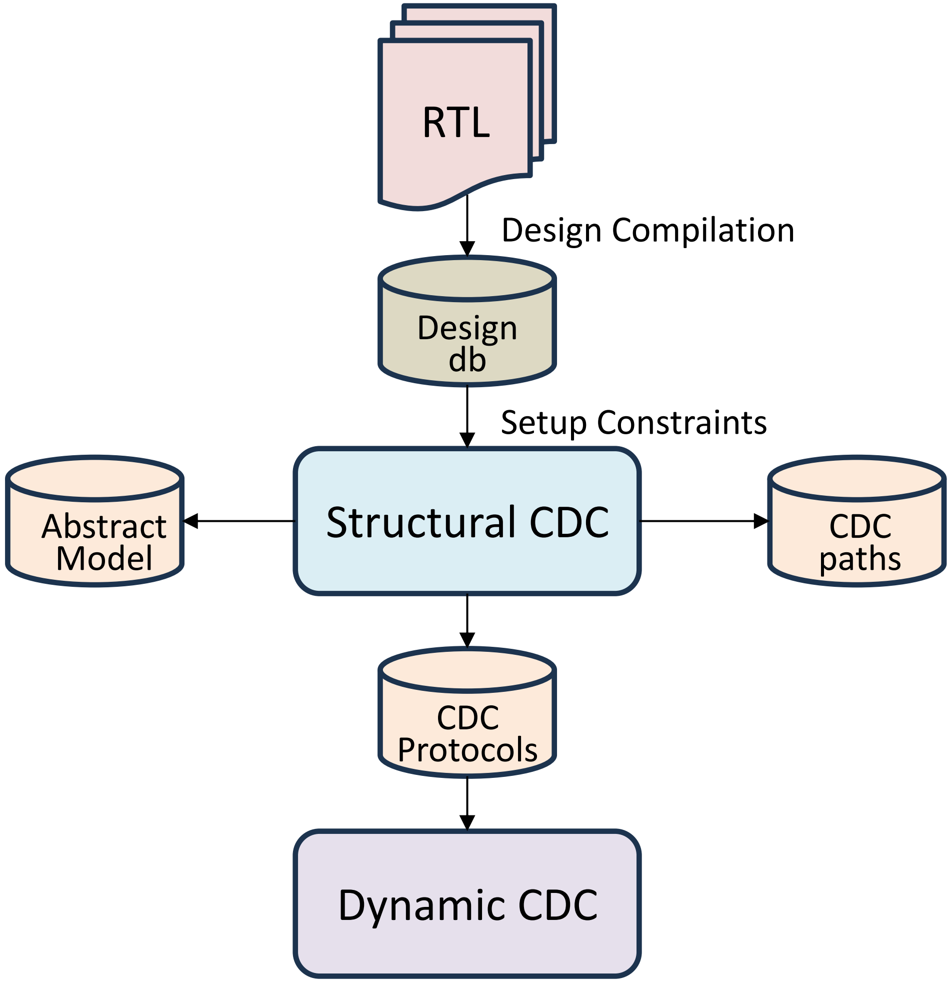
Play VIDEO - 1

- CDC Verification flow
- Setup constraints
- Challenges

1.2 CDC SETUP & CONSTRAINTS

CDC Verification flow

- Design Compilation
  - Parameters, defines
  - SV packages, SV configuration, SV interfaces
- Setup Constraints
  - Clock, reset, and IO signals
  - Configuration: stable, constant inputs
- Structural CDC Check
  – CDC schemes validation and debugging
- Abstract Model Generation
- Dynamic/Formal CDC Verification
  – CDC constraints and protocols



Setup Constraints

- The set of constraints used to guide CDC verification

- Clocks
- Resets
- Configuration signals
- Black boxes
- Primary inputs/outputs

Don’t rely blindly on timing constraints

⚠

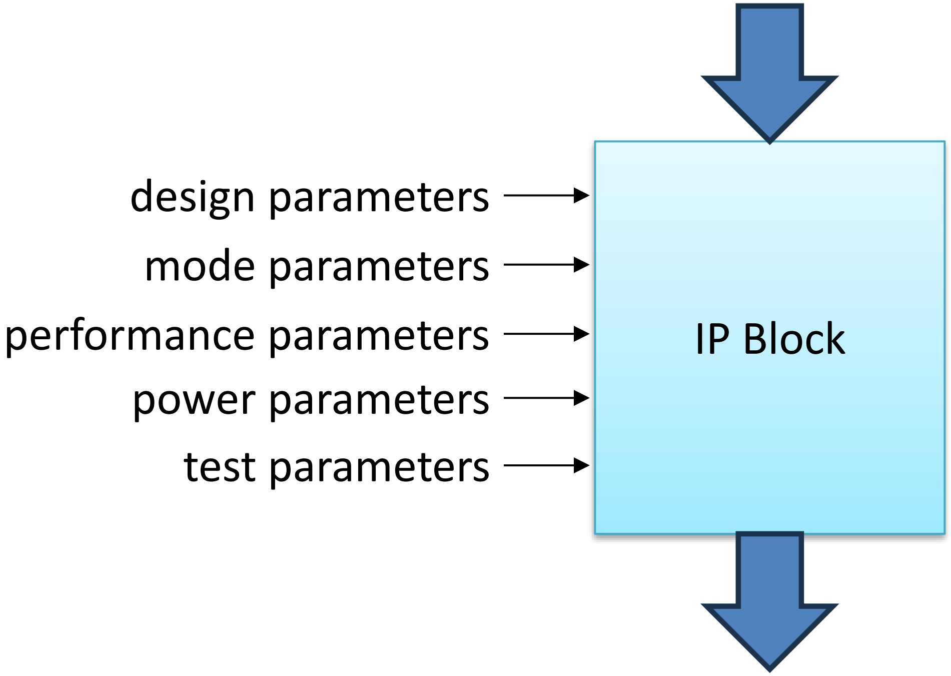
Reuse timing constraints is risky

- Pseudo-static signals
- Exclusive signals
- Gray coded buses
- Custom synchronizers
- False path

Clock groups for timing analysis =/= Clock groups for CDC analysis
Signal paths waived for time analysis =/= Signal paths waived for CDC analysis

Challenge #1: Design Parameters

- Blocks/IPs have many parameters
  - Some used for design, performance, optimization
  - Some used for integration, mode
  - Some used for DFT, DFP, DFM, etc
- Most parameters will affect CDC results
- Some parameters may not affect CDC results
  - Data_width, Addr_width
  - FIFO_depth, RAM_size
- The abstract model will become parameter-specific



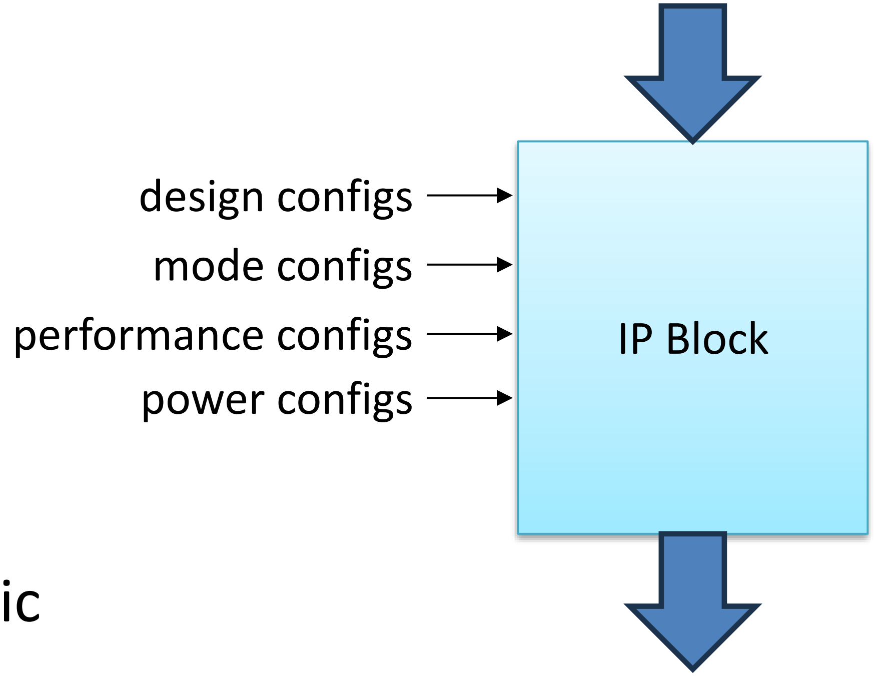
To specify or not to specify

Challenge #2: Configuration Signals

- Blocks/IPs have many configuration signals
  - Some used for design, performance, optimization
  - Some used for integration, mode
  - Some used for DFT, DFP, DFM, etc

- Most configuration signals will affect CDC results
  - Clock select, gating signals

- The abstract model will become configuration-specific



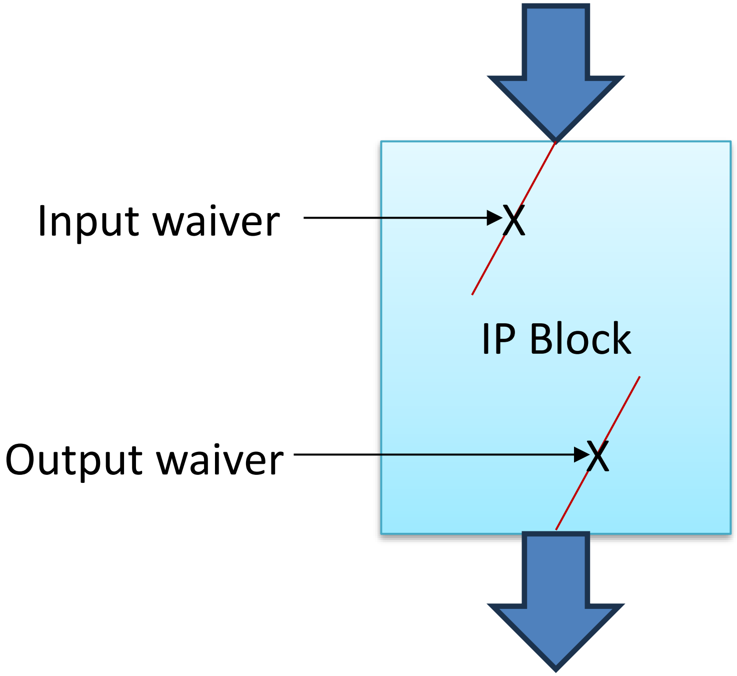
To constraint or not to constraint

Challenge #3: CDC Waivers

- Blocks/IPs have many CDC violations
  - Some are on the input signals
  - Some are on the output signals

- Some of the input violations can be waived
  - Pseudo-static input signals
  - Output signals
- Some of the input violations should not be waived

- The abstract model will become waiver-specific

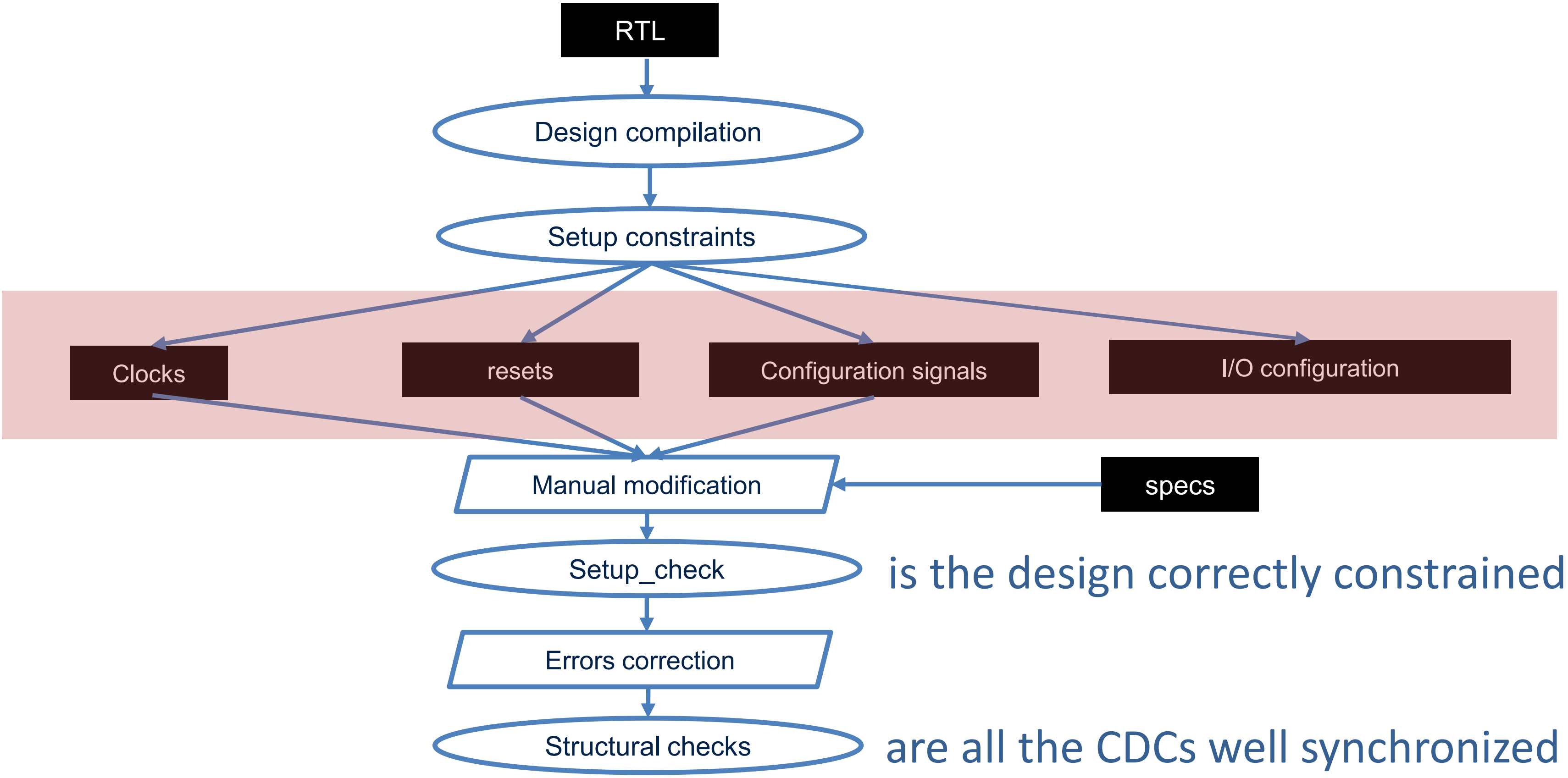


To waive or not to waive

- Structural CDC
- User defined synchronization modules
- CDC constraints
- Reset Domain Crossings

1.3 STRUCTURAL CDC/RDC

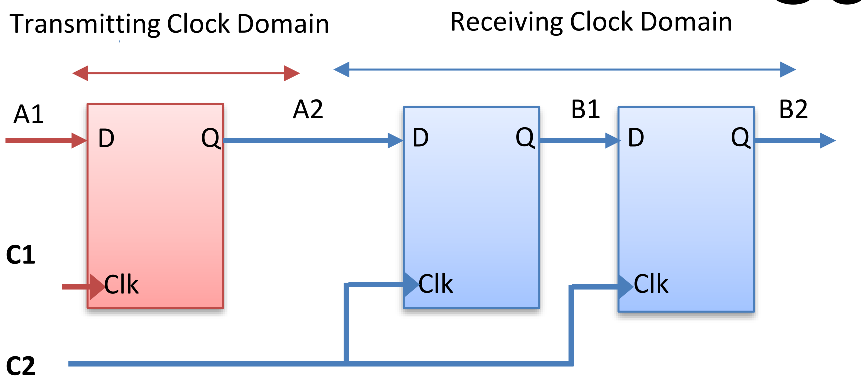
Structural CDC Analysis



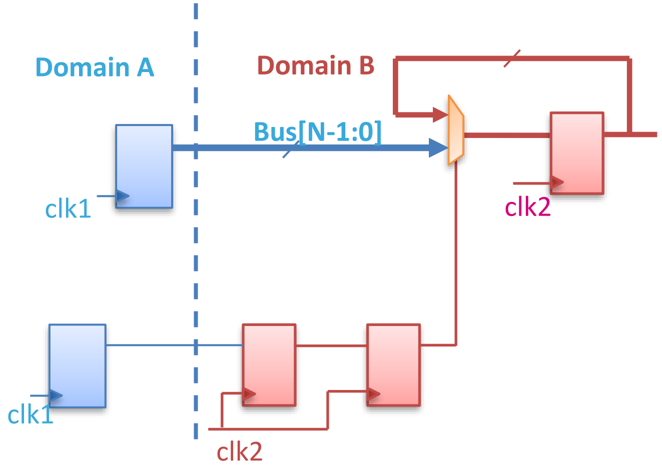
is the design correctly constrained ?

are all the CDCs well synchronized ?

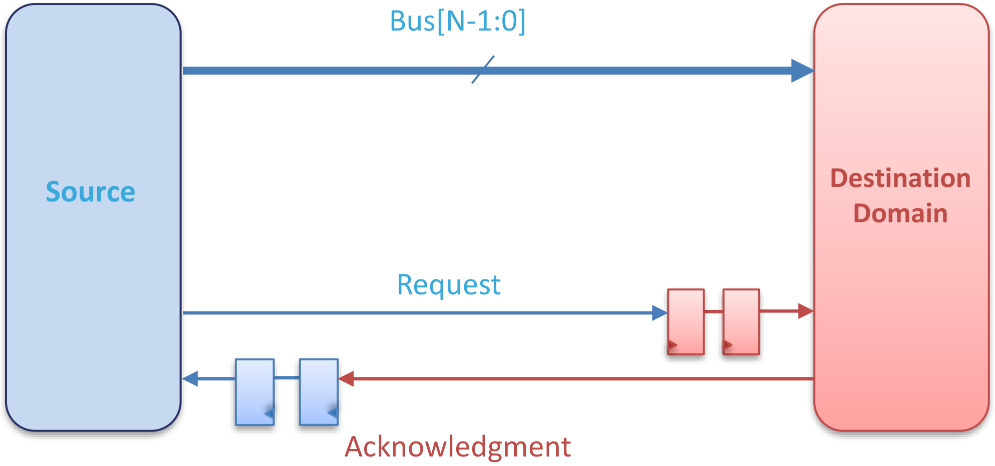
Structural CDC - Commonly Used Synchronization Schemes



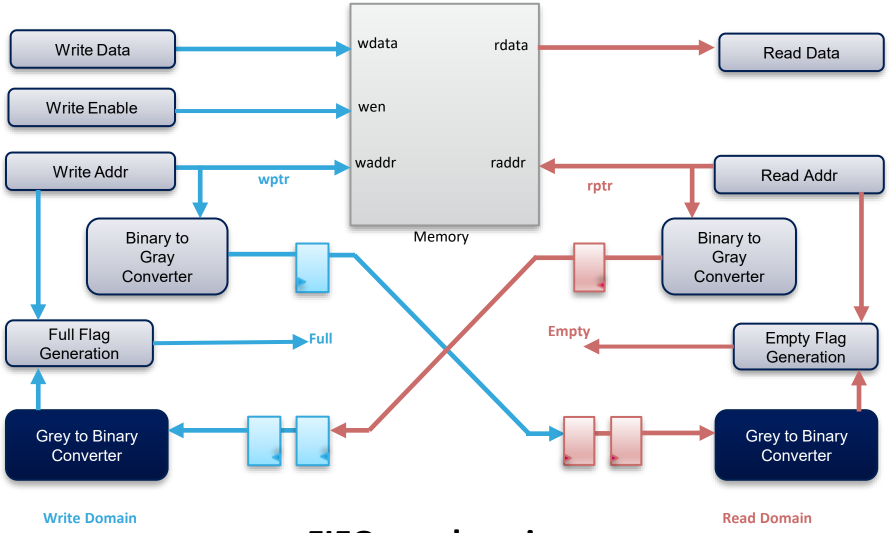
Double-FF synchronizer



MUX synchronizer



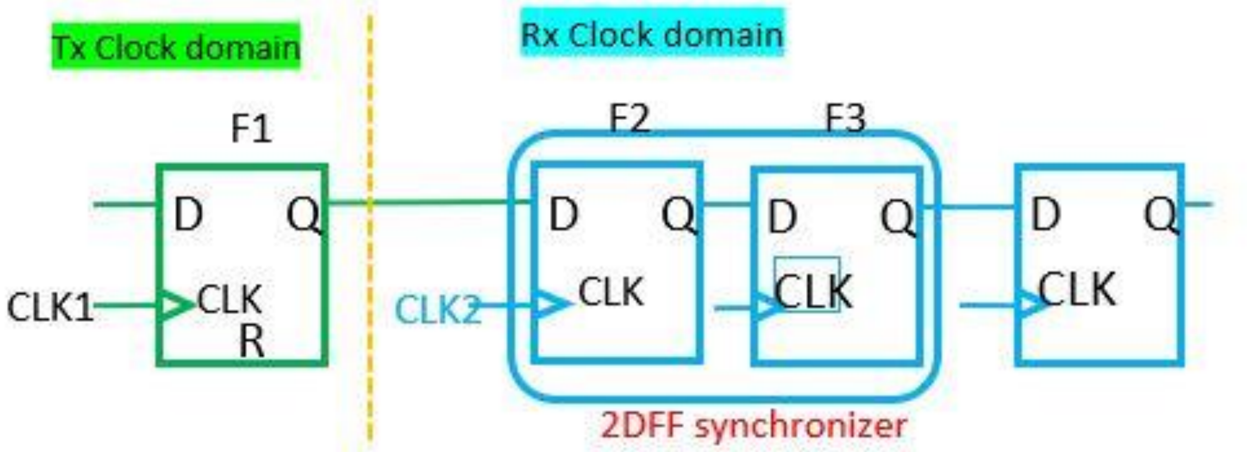
Handshake synchronizer



FIFO synchronizer

Structural CDC – User defined sync modules

- Double FF Synchronizer
  - Most design houses prefer to use their own CDC components
    - Disable automatic detection of the specific synchronizer type that you don't want the tool to recognize automatically
    - Declare your own scheme as user-defined synchronizer (before scheme detection)
  - Example: Use my own 2DFF only
    - Disable auto-detection of 2DFF
    - Declare your own module as 2DFF



Structural CDC

- Various Signal Configurations possible for structural CDC Analysis
  - Constant
  - Static
  - Mutually exclusive / Gray code
  - Externally synchronized
  - CDC False paths
    - *Not recommended (avoid using it to mask real CDCs)*
- Purpose
  - Define signal behavior that can help to reduce CDC analysis noise
    - Exclude certain paths which may not have any standard synchronizer but safe for CDC
    - Helps to speed up CDC analysis

Structural CDC

- CDC Constraints – Constant Declaration
  - It can be applied on a port or on an internal signal
  - A constant signal does not change in a given mode and hence does not cause a CDC issue

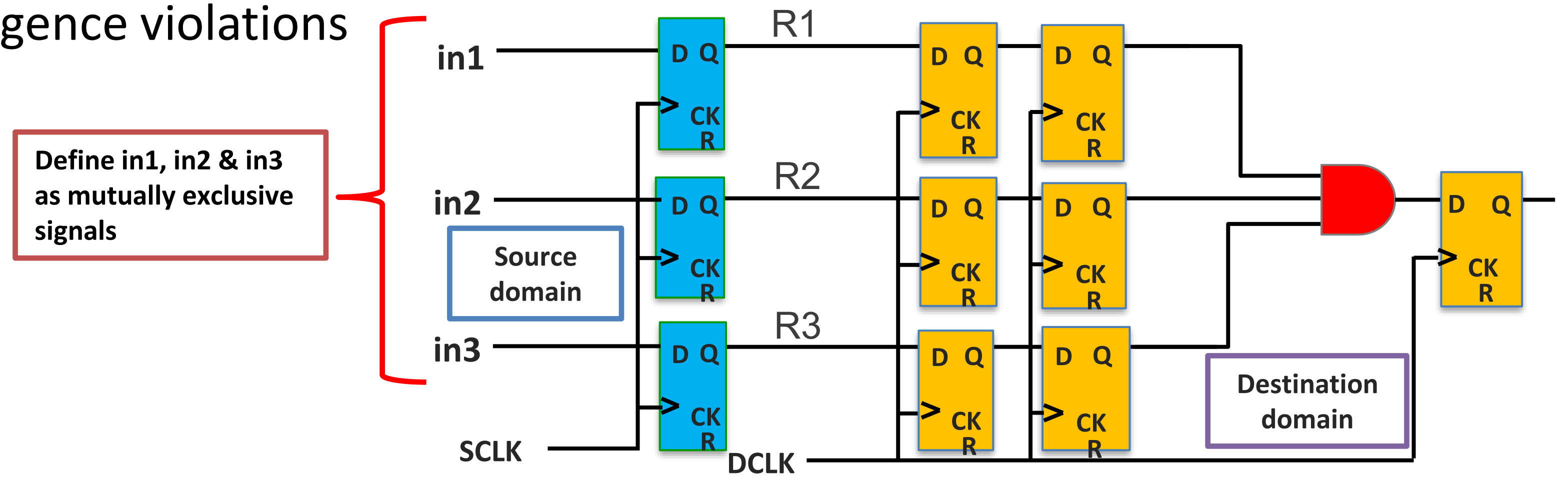
- Purpose
  - Define signal behavior that can help to reduce CDC analysis noise
    - Exclude certain paths which may not have any standard synchronizer but safe for CDC
    - Helps to speed up CDC analysis

Structural CDC

- CDC Constraints – Static Declaration
  - Any signal that does not change while the destination is active
  - Same as quasi-static or pseudo-static
  - A static signal does not cause CDC issues because
    - The receiver clock is not active
    - The receiver is under reset

Structural CDC

- CDC Constraints – Gray Coded Declaration
  - A bus can be specified as gray coded – Only one bit can toggle at a time
- CDC Constraints – Mutually Exclusive Toggle Declaration
  - A set of independent signals that can toggle only one at a time can be defined as mutually exclusive toggle
    - Helps in avoiding convergence violations

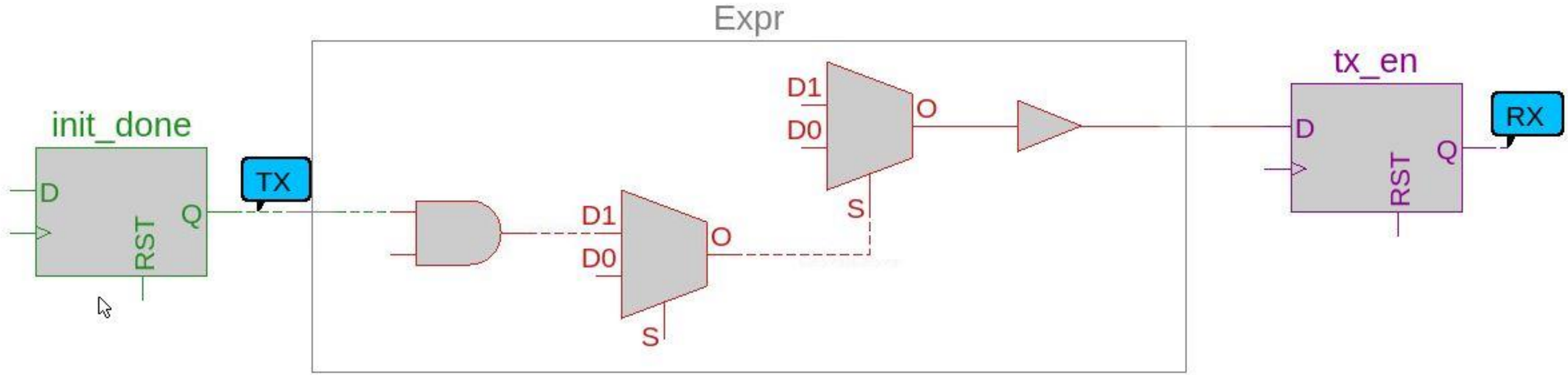

Define in1, in2 & in3 as mutually exclusive signals

Structural CDC

- CDC Constraints - Externally Synchronized
  - A block level input/output port can be declared as *externally synchronized*
    - Represents the output of a control synchronizer (2DFF/Edge/Pulse)
    - Can be used as the control path for complex synchronizers (MUX Synchronizer, Glitch Protector)
    - Helps in auto-detection of the above composite synchronization scheme types
- CDC Constraints - CDC False Path Declaration
  - CDC Checks can be disabled on certain paths by user-defined constraints
  - User can set a constraint to let the tool automatically identify a functionally false path and hence reports the path as a safe path

Structural CDC

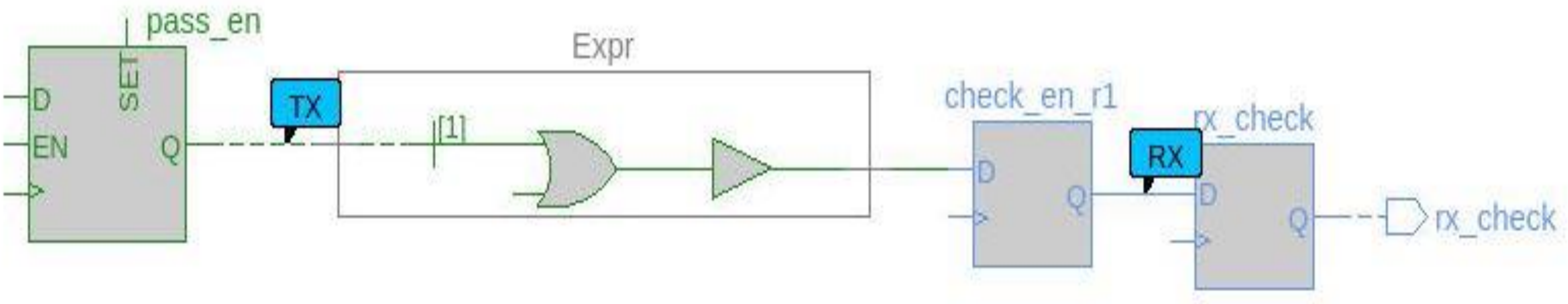
- Missing synchronizer on CDC path

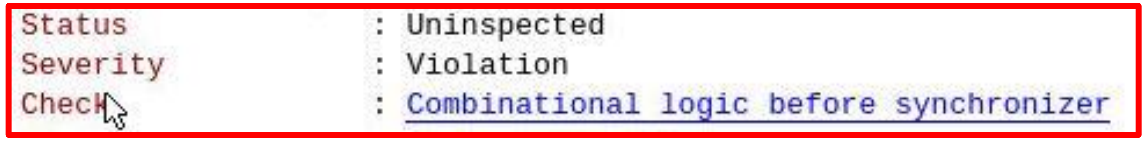


```
Status   : Uninspected
Severity : Violation
Check    : Single-bit signal does not have proper synchronizer
```

Structural CDC

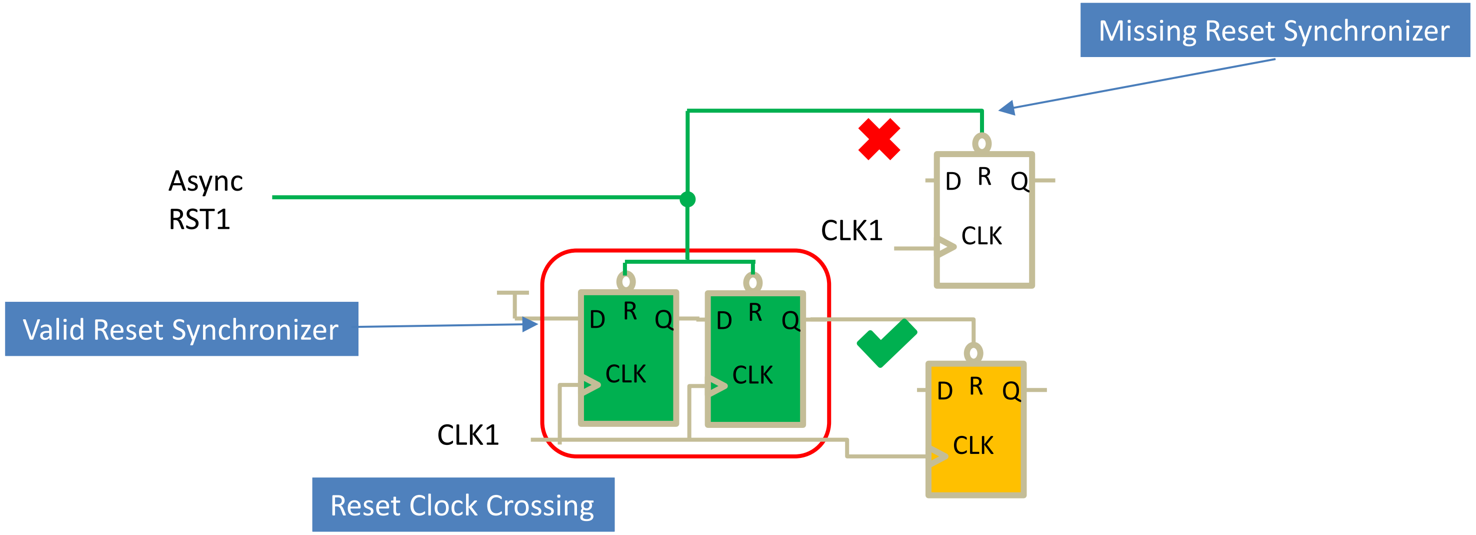
- Combo-logic before synchronizer on CDC path





```
Status                  : Uninspected
Severity                : Violation
Check                   : Combinational logic before synchronizer
```

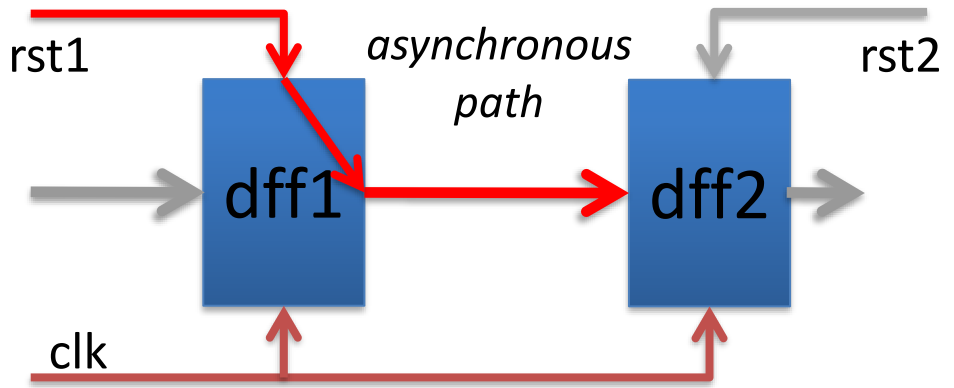
Reset-Domain Crossing



- Reset signal crossing from one clock domain to another
  - The asynchronous de-assertion of the reset signal at the destination flop can cause the signal to become metastable
  - Reset signals are required to be synchronized to destination domains for synchronous de-assertions

Reset-Domain Crossing

- Asynchronous reset domains causes meta-stability
  - – Contain registers whose resets are asserted asynchronously
  - – Originate in one asynchronous reset domain
  - – Sampled by register(s) in a different reset domain
  - – Reset ordering of different resets in the design



- Assertion Based Verification
- Overcoming Limitations

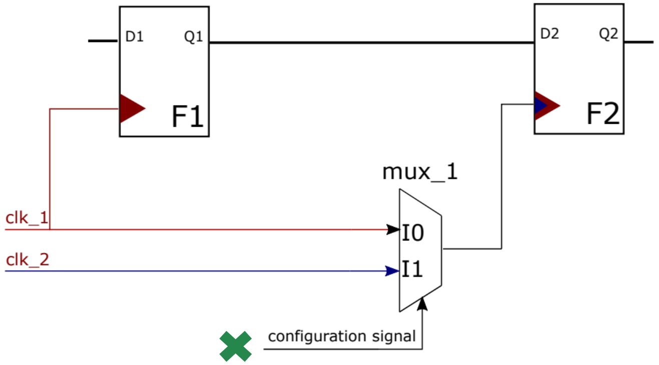
1.4 CDC ASSERTIONS

Structural CDC/RDC - Limitations

1- Constraints based static checks

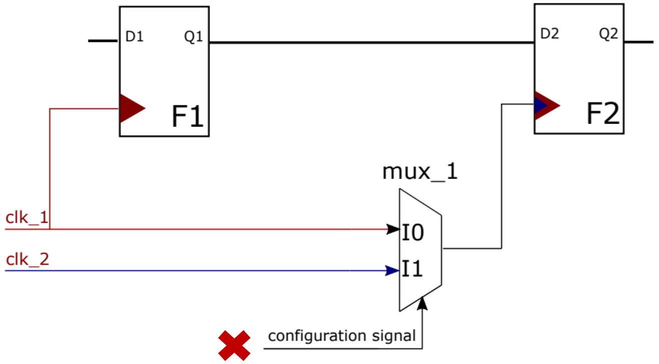
- Affect the results of the structural checks
- Are taken blindly for the structural verification
  - e.g., a CDC can be bypassed if the crossing signal is pseudo-static

✖ set_case_analysis 0 configuration_signal



Synchronous

✖ set_case_analysis 1 configuration_signal



Asynchronous

2- Rules based static checks

- Not possible to have rules for all architectures
- False positives / negatives
- Cannot verify correctness of design

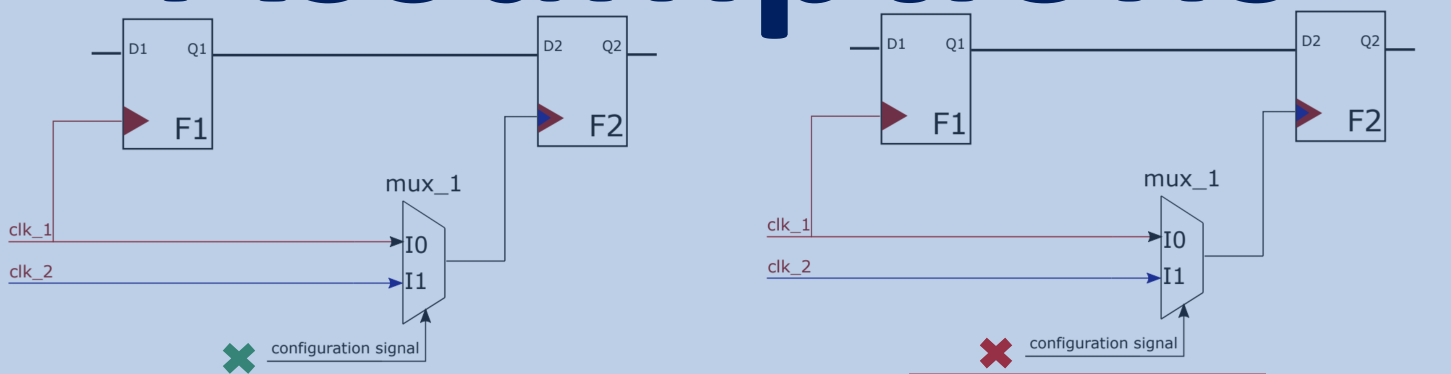
Overcoming Limitations-Assertions based Verification

1- Constraints based static checks

- Affect the results of the structural checks
- Are taken blindly for the structural verification
  - e.g., a CDC can be bypassed if the crossing signal is pseudo-static

Assumptions

✖ set_case_analysis 0 configuation_signal ✖ set_case_analysis 1 configuration_signal



Synchronous

Asynchronous

2- Rules based static checks

- Not possible to have rules for all architectures
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Assertions

Overcoming Limitations-Assertions based Verification

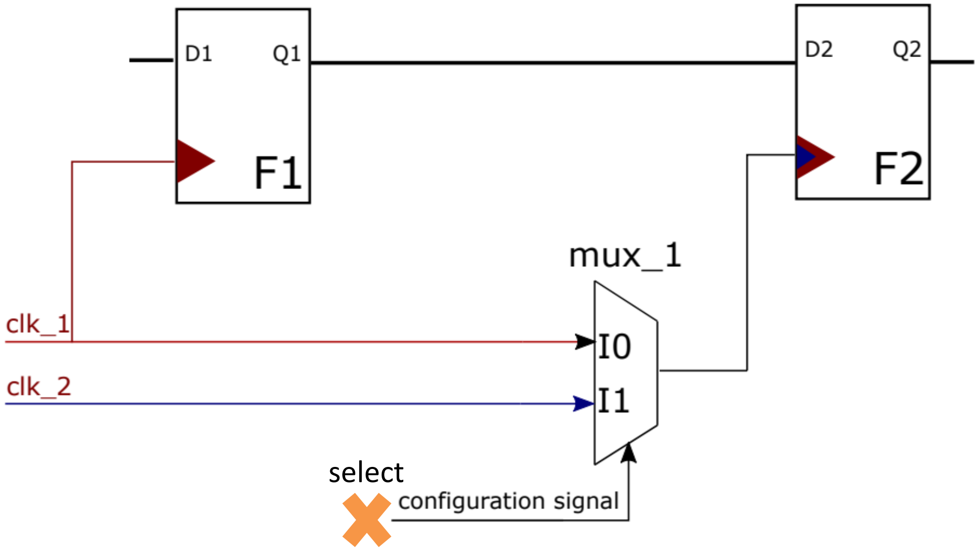
1- Constraints based static checks

- Constraints to be double checked with the functional verification

- Configuration signals

```
define_constant –value [0/1] –signal [signal name]
```

```
always@*
  begin
   assert_cdc_constant_prop : assert (select === value)
```



Overcoming Limitations-Assertions based Verification

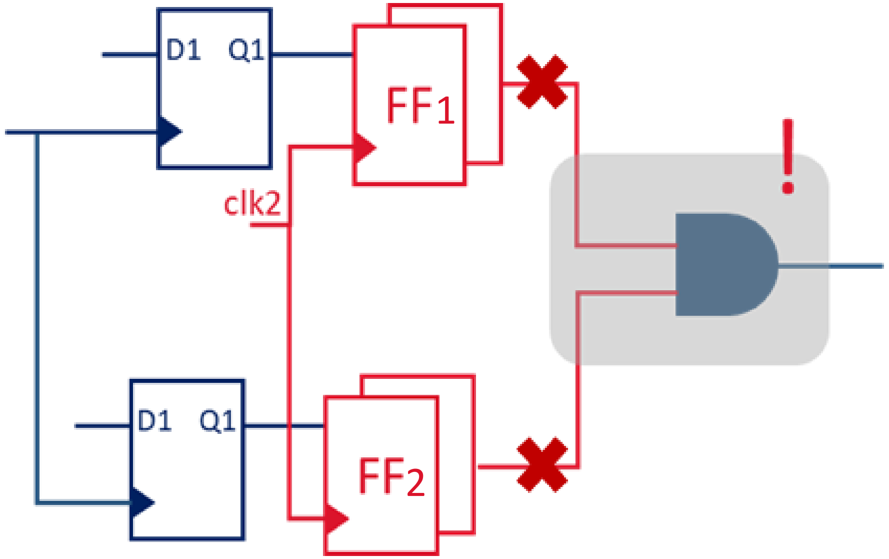
1- Constraints based static checks

- Constraints to be double checked with the functional verification

- Mutually exclusive

define_exclusive –signals [set of signals names]

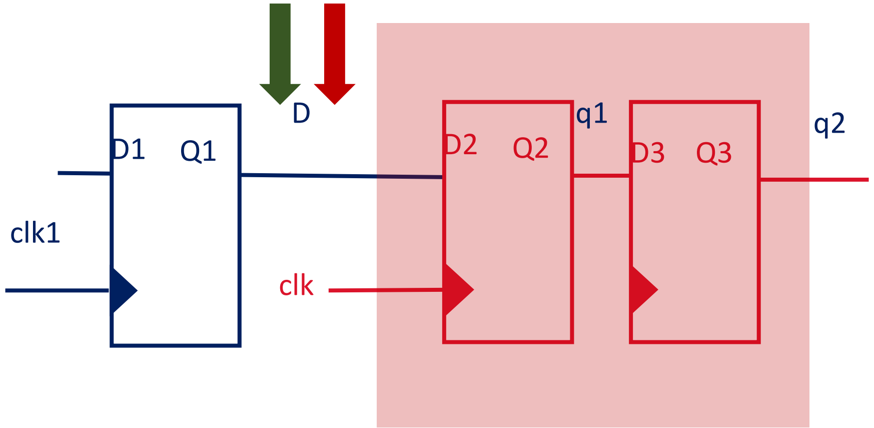
```
property mutex (data, clk);
   @(posedge clk)
     $onehot0(data ^ $past(data));
  endproperty
```



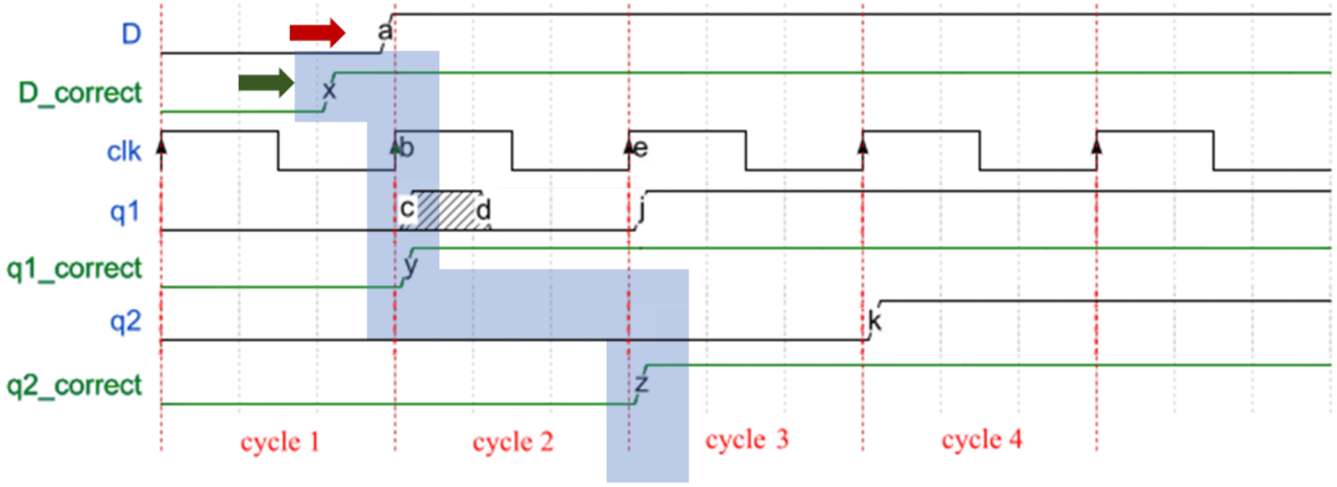
Overcoming Limitations-Assertions based Verification

2- Rules based static checks

- Fundamentally target to verify **design intent**
- CDC paths are **not covered by STA** :
  - Make sure source data is stable while crossing.



```
property cdc_data_stable (D, NUM_CYCLES);
    @(posedge clock)
     ##1 $changed(D) |-> $stable(D)[*(NUM_CYCLES-1)];
 endproperty
```

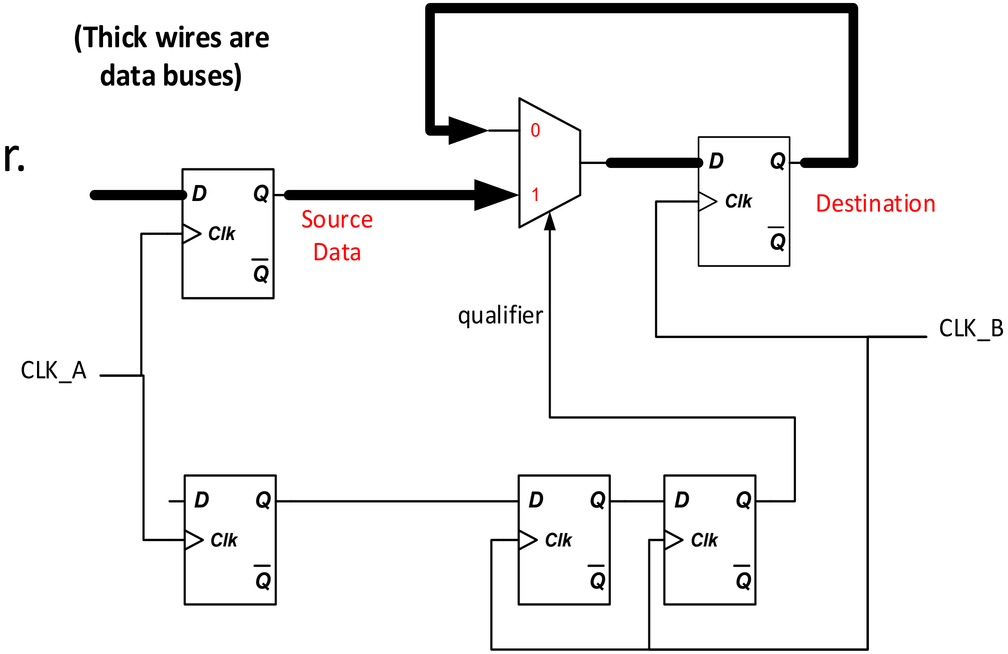


- NUM_CYCLES is based on synchronization latency

Overcoming Limitations-Assertions based Verification

2- Rules based static checks

- Fundamentally target to verify **design intent**
- CDC paths are **not covered by STA** :
  - Make sure source data is stable for several cycles.
  - Enabler : Make sure source data is stable wrt to its enabler.

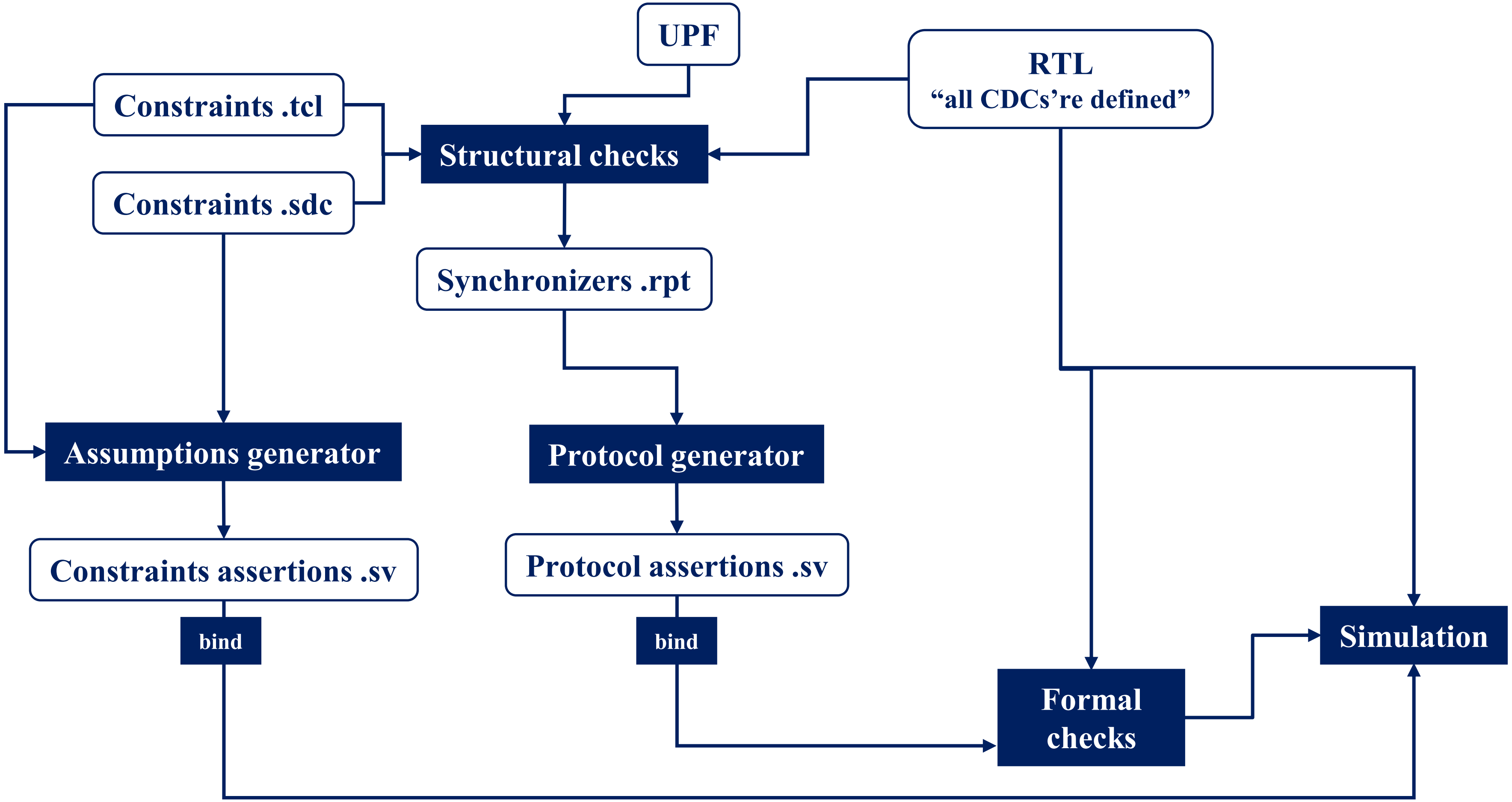


Source data must be static when CDC Control is enabling.
Source data can toggle when CDC Control is disabling.
CDC Control must be a known value

```
property qual_data_stable (SRC_DATA,QUAL,SETUP_ROOM);
   ##1 $changed(SRC_DATA) |-> (QUAL === 1’b0)[*SETUP_ROOM];
endproperty
```

- SETUP_ROOM = Synchronization Latency + Implementation Headroom

ABV - Assertions based Verification



Dynamic CDC Verification

- Dynamic verification is to ensure
  - structural CDC check is done with the proper constraints and assumptions
  - the identified CDC paths follow the protcols defined by the CDC schemes
- CDC constraint properties
  - Assertions are generated based on the setup constraints
  - Ideally, should be done concurrently with structural CDC check
  - Violations can potentially invalidate the complete structural CDC
- CDC protocol properties
  - Assertions are generated based on the CDC paths
  - Violations can potentially invalidate the CDC paths

- Hierarchical Flow

1.5 HIERARCHICAL CDC/RDC

PLAY VIDEO -2

2.1 Accellera CDC Working Group

- Presentation
- The five sub working groups
- Call for contribution

Accellera CDC WG initiative

- The WG was formed in Jan. 2023 to explore the need for the creation of a standard to converge CDC collateral integration from different tools/vendors for ease (time-to-market) and quality (bug-free silicon).

- Fundamentally, what is being proposed is a common CDC interface standard that:
  - Every vendor/tool can translate their native format to/from (maintaining their IP)
  - Every IP can run their tool-of-choice to verify and produce collateral, and generate the standard format for SOCs that use a different tool
  - Every SOC can quickly (time-to-market) and safely (quality) integrate either native collateral, or translate from the standard collateral into their tool-of-choice

- The Accellera CDC WG goal, as approved by the Accellera board is as follows:
  - Produce an LRM for publication
  - Enable all EDA vendors in developing tools that meet this specification in generated collateral
  - Enable IP companies to generate collateral using various vendor/tools
  - Enable SOC companies to consume generate collaterals from different vendor/tools into their tool-of-choice

What was the problem?

As we move from monolithic designs … to IP/SOC with IPs sourced from a small/select providers … to sourcing IPs globally (to create differentiated products) …

We must maintain quality as we drive faster time-to-market

In areas where we have standards (SystemVerilog, OVM/UVM, LP/UPF), the integration is able to meet the above (quality, speed)

But in areas where we don’t have standards (in this case, CDC), most options trade-off either quality, or time-to-market, or both :-(

Creating a standard for inter-operable collateral addresses this gap

Accellera CDC WG initiative

Pre-WG launched Sep ‘22 to evaluate need. WG launched Jan ’23

134 members from 24 companies (as of Sept 06 ‘24)

5 active sub-groups: Output-Collateral, Format, Assertions, Testing, Training

Ver	Focus	Timeline
v0.1	CDC	Oct 2023
v0.3	RDC & Assertions	July 2024
v0.5	Complexities & Extensions	Dec 2024
v1.0	Final LRM release	Mar 2025

Agnisys	Aldec	AMD	AMS	Analog Devices	ARM	Arteris	Blue Pearl Software
Cadence	Huawei	Infineon	Intel	Marvel	Microchip Technologies	Microsoft	NVIDIA
NXP	Qualcomm	Renesas	Robert Bosch	Siemens EDA	ST Micro	Synopsys	Verilab

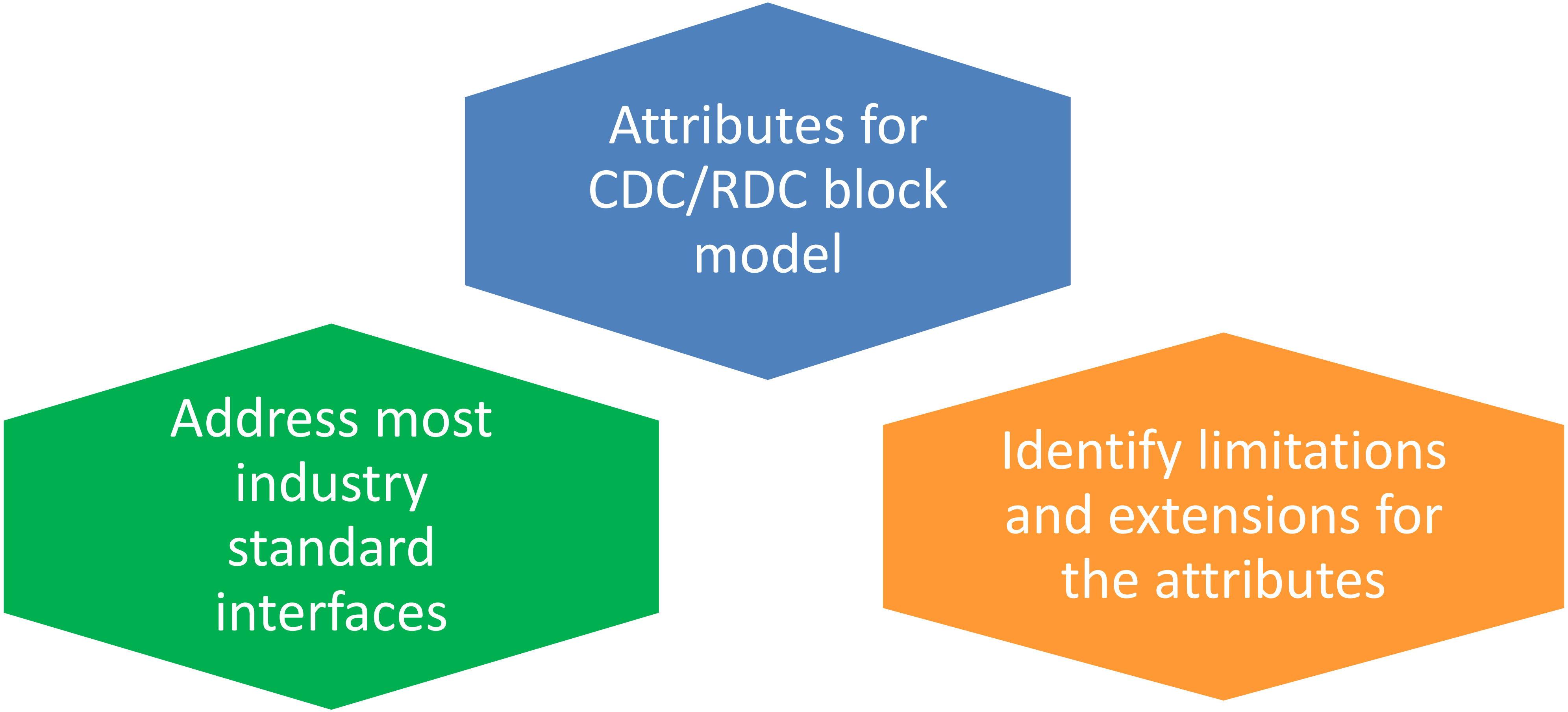
Accellera CDC WG Scope

- Tool-agnostic interoperable collateral
- Supporting hierarchical CDC/RDC/Glitch structural analysis
- Human readable, and machine parseable
- LP/UPF compliant
- Multi-mode/param/instance comppliant
- Covering majority of common interface protocols (e.g. AMBA, UCIe, etc.)
- Constraints/Assumptions can be verified with SVAs
- Can meet other needs (e.g. FPGA, Analog)

2.2 Output Collateral Subgroup

Output Collateral Subgroup

Output-Collateral



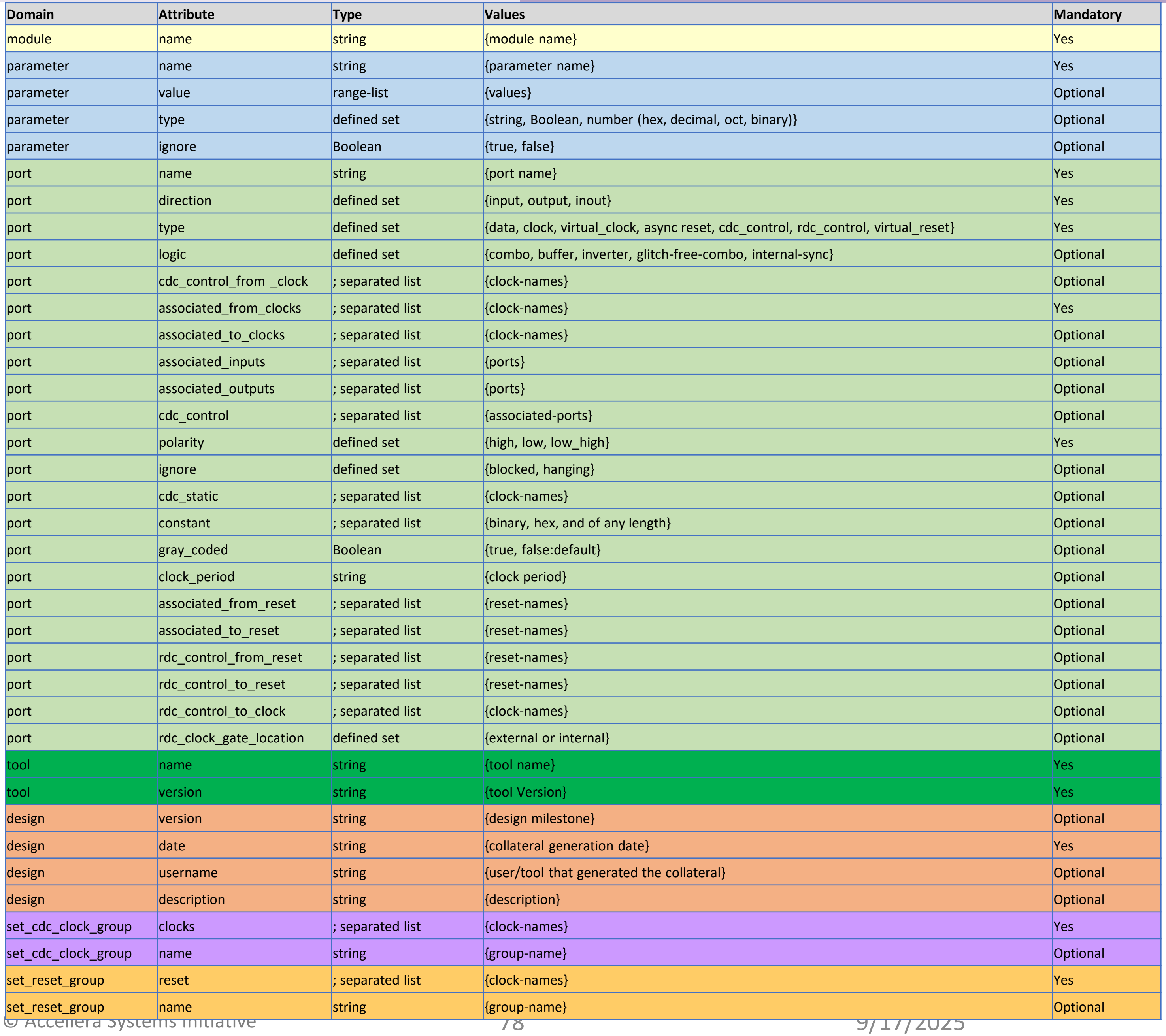
Attributes for CDC/RDC block model

Address most industry standard interfaces

Identify limitations and extensions for the attributes

Attributes Table in LRM v0.3

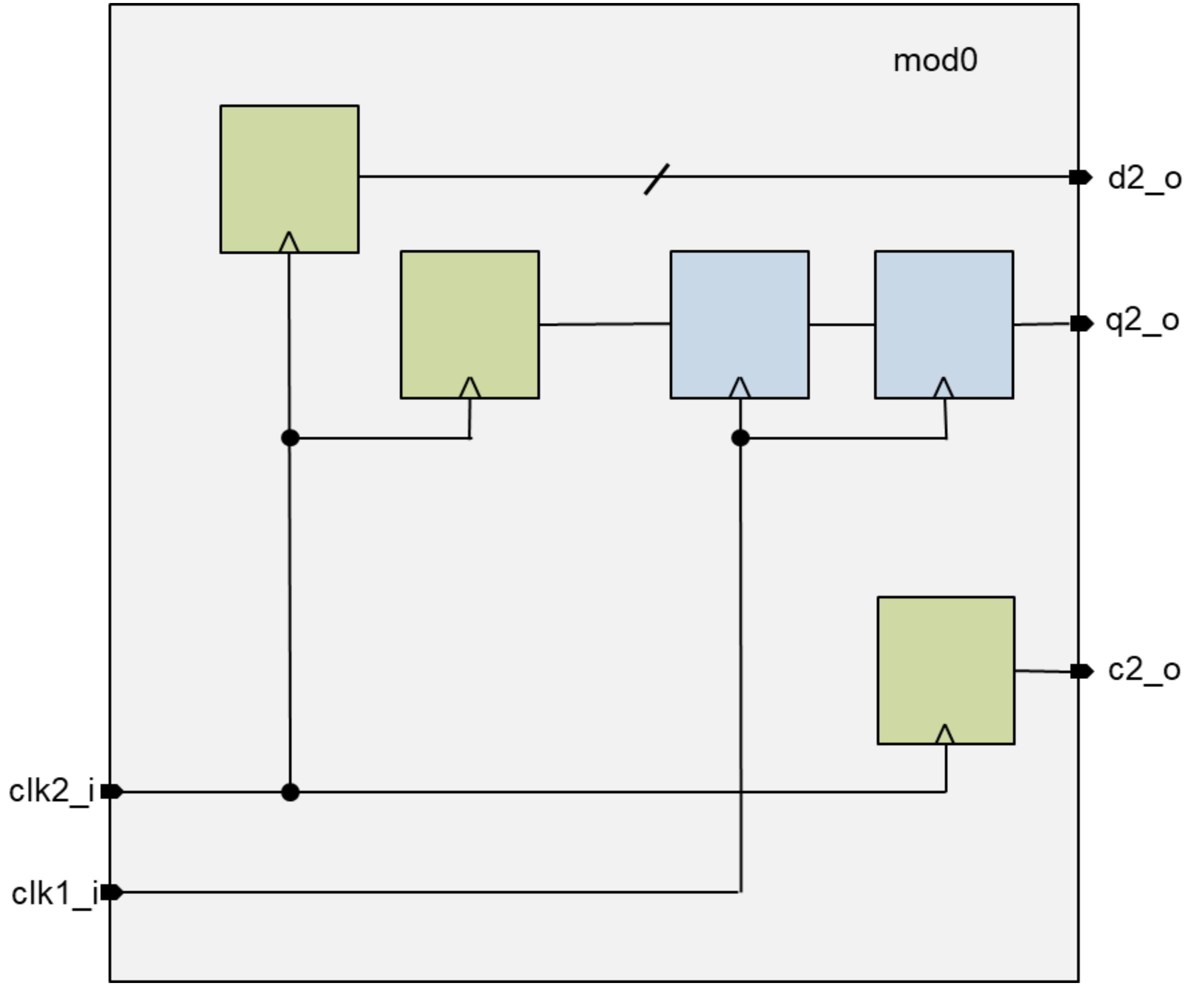
Output-Collateral



Domain	Attribute	Type	Values	Mandatory
module	name	string	{module name}	Yes
parameter	name	string	{parameter name}	Yes
parameter	value	range-list	{values}	Optional
parameter	type	defined set	{string, Boolean, number (hex, decimal, oct, binary)}	Optional
parameter	ignore	Boolean	{true, false}	Optional
port	name	string	{port name}	Yes
port	direction	defined set	{input, output, inout}	Yes
port	type	defined set	{data, clock, virtual_clock, async reset, cdc_control, rdc_control, virtual_reset}	Yes
port	logic	defined set	{combo, buffer, inverter, glitch-free-combo, internal-sync}	Optional
port	cdc_control_from _clock	; separated list	{clock-names}	Optional
port	associated_from_clocks	; separated list	{clock-names}	Yes
port	associated_to_clocks	; separated list	{clock-names}	Optional
port	associated_inputs	; separated list	{ports}	Optional
port	associated_outputs	; separated list	{ports}	Optional
port	cdc_control	; separated list	{associated-ports}	Optional
port	polarity	defined set	{high, low, low_high}	Yes
port	ignore	defined set	{blocked, hanging}	Optional
port	cdc_static	; separated list	{clock-names}	Optional
port	constant	; separated list	{binary, hex, and of any length}	Optional
port	gray_coded	Boolean	{true, false:default}	Optional
port	clock_period	string	{clock period}	Optional
port	associated_from_reset	; separated list	{reset-names}	Optional
port	associated_to_reset	; separated list	{reset-names}	Optional
port	rdc_control_from_reset	; separated list	{reset-names}	Optional
port	rdc_control_to_reset	; separated list	{reset-names}	Optional
port	rdc_control_to_clock	; separated list	{clock-names}	Optional
port	rdc_clock_gate_location	defined set	{external or internal}	Optional
tool	name	string	{tool name}	Yes
tool	version	string	{tool Version}	Yes
design	version	string	{design milestone}	Optional
design	date	string	{collateral generation date}	Yes
design	username	string	{user/tool that generated the collateral}	Optional
design	description	string	{description}	Optional
set_cdc_clock_group	clocks	; separated list	{clock-names}	Yes
set_cdc_clock_group	name	string	{group-name}	Optional
set_reset_group	reset	; separated list	{clock-names}	Yes
set_reset_group	name	string	{group-name}	Optional

Port Attribute Modelling

Output-Collateral



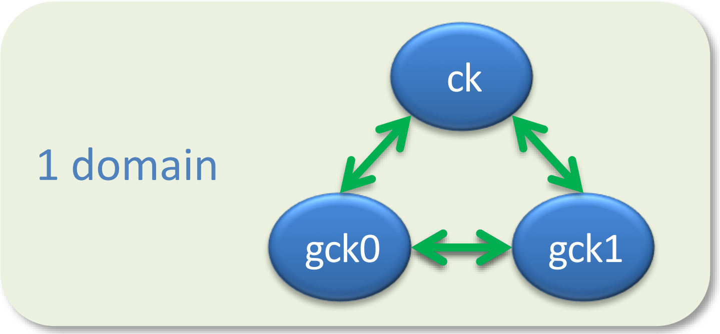
Blue boxes are in clk1_i clock domain
Green boxes are in clk2_i clock domain

example in Tcl-format for output interface

```
cdc_set_module mod0

   cdc_set_port d2_o                           \
      -type                     data    \
      -direction                output \
      -associated_from_clocks clk2_i \
      -cdc_control              q2_o

   cdc_set_port q2_o                                \
      -type                     cdc_control \
      -direction                output      \
      -cdc_control_from_clock clk2_i        \
      -associated_from_clock  clk1_i        \
      -associated_outputs       d2_o

   cdc_set_port c2_o                            \
      -type                     data     \
      -direction                output   \
      -associated_from_clock  clk2_i
```

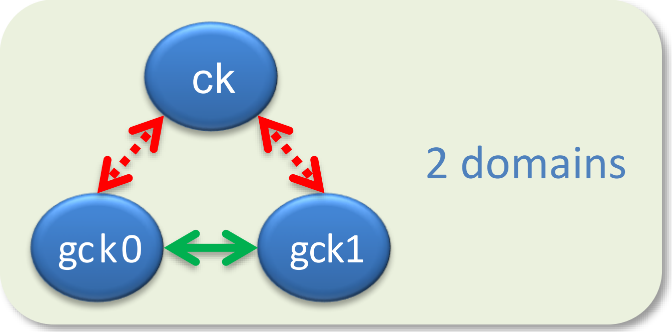
cdc_set_clock_group (Tcl format)

Output-Collateral



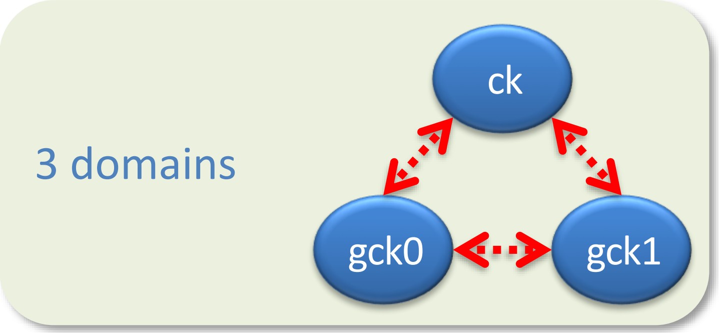
1 domain

```
cdc_set_clock_group -name common_domain -clocks {ck gck0 gck1}
```



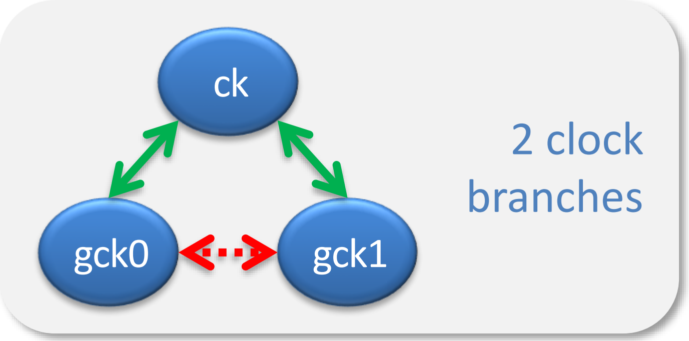
2 domains

```
cdc_set_clock_group -name small_domain -clocks {ck}
cdc_set_clock_group -name large_domain -clocks {gck0 gck1}
```



3 domains

```
cdc_set_clock_group -name domain_C -clocks {ck}
cdc_set_clock_group -name domain_0 -clocks {gck0}
cdc_set_clock_group -name domain_1 -clocks {gck1}
```



2 clock branches

compatibility sets: common members allowed

```
cdc_set_clock_group -name left_branch   -clocks {ck gck0}
cdc_set_clock_group -name right_branch -clocks {ck gck1}
```

2.3 Format Subgroup

Format Subgroup Mission

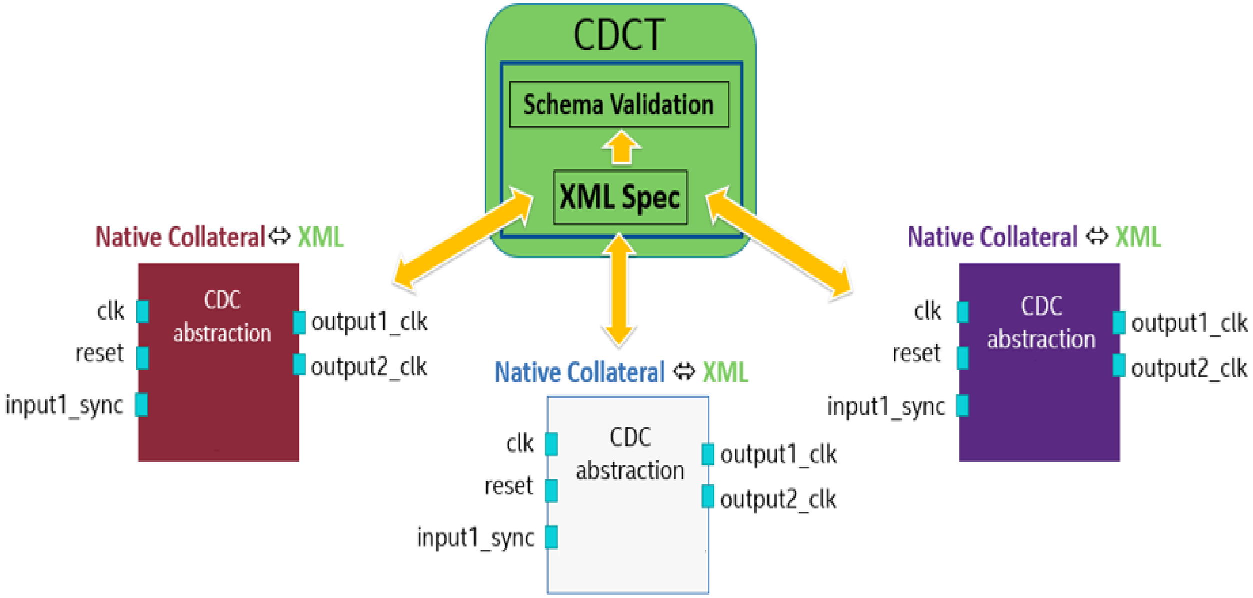
Format

- **Goal**
  1. Determine exact format for domain specific language that can be used to capture required attributes/data from input/output/verification collaterals.
  2. Ensure quality in terms of compliance to spec.
- **Methodology**
  1. List different options like IP-XACT, TCL, Excel, JSON, etc.
  2. Experiment with populating the formats to ascertain the ability to meet the requirements.
  3. Determine pros and cons for each option of format.
  4. Recommend a final format post CDC Workgroup approval

Feasibility Study

Format

- A limited feasibility study for CDC
  - conducted on a subsystem with multiple IPs connected by AMBA interfaces
  - across three different vendor tools
  - With limited support from the vendors
- Results:
  - 99.5% of what was identifiable in a flat run was also identifiable if the native abstraction collateral was replaced with an XML representation and translated across the vendor tools.



Primary Requirements

Format

- Describing IP
  - static or semi-static
  - IP-XACT is industry standard for IP definition and packaging
  - Use models of IP and Product companies
- Integration of IP
  - Dynamic environment requires programmability for CDC definition
  - Tcl is preferred and widely used in industry
  - Use models for Product and EDA companies

IP-XACT vs Tcl

Format

- IP-XACT
  - IP-XACT is perfect for static representation
  - Useful for IP Delivery and SoC Integration
  - Infrastructure required for converting existing proprietary formats to IP-XACT
- Tcl
  - Tcl handles dynamic and conditional CDC scenarios better
  - EDA companies currently supports proprietary formats that are Tcl like
  - Human readability issue

- CDC Workgroup voted to use combination of both Tcl and IP-XACT

Format Subgroup

Format

- EDA companies to provide transformers for Tcl to/from IP-XACT
  - Also provide translators to and from its native format from and to the standard format
- Standard is tool agnostic
- IP providers have option to choose tools
  - to verify and produce collateral
  - to generate the standard format for SoCs that use a different tool
- The format is released as part of LRM ver 0.3 in July
  - Tcl API commands capturing and handling clock domains and attributes
  - IP-XACT schema for CDC as Accellera vendor extensions to the IP-XACT standard

2.4 Assertion Subgroup

Assertion Subgroup Mission

Assertion

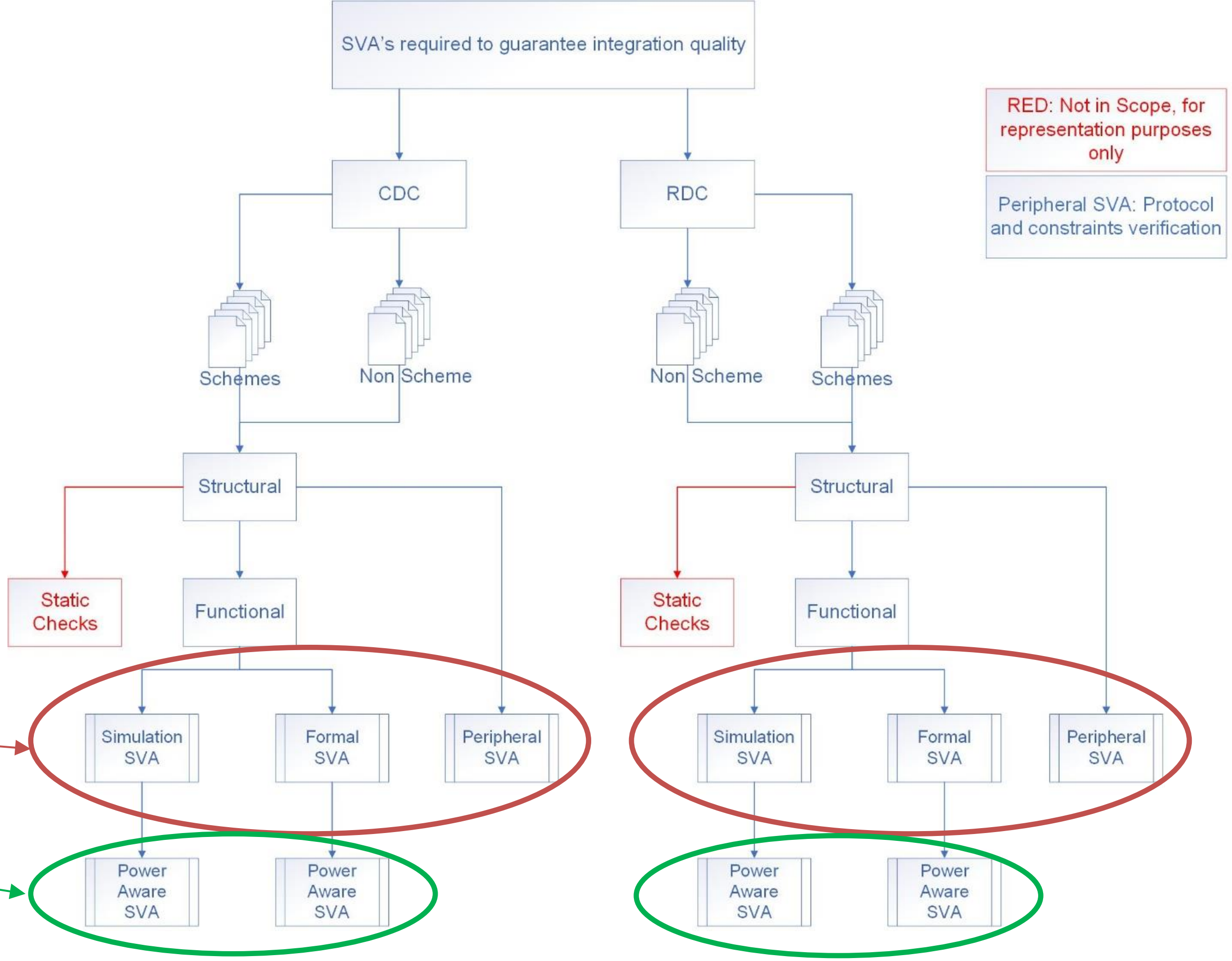
- **Goal**

1. Produce Language Reference Manual (LRM) addendum for Assertions.
2. Enable all EDA vendors in developing tools that meet specification for generating System Verilog Assertions (SVA) along with collateral.
3. Enable Intellectual Property (IP) companies to generate SVA along with collateral using various vendors/tools.
4. Enable System On Chip (SOC) companies to consume generated SVA from any vendor/tool into their tool of choice.

Assertion Subgroup

Assertion

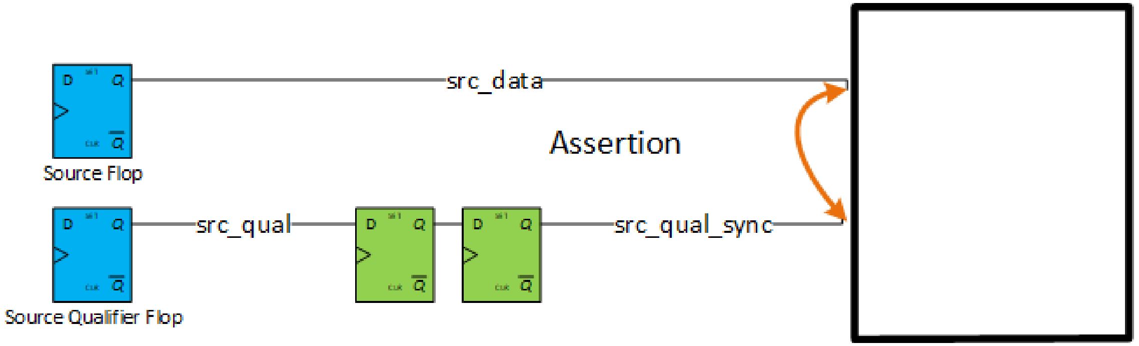
- CDC architectures are studied for possible verification strategies.
- Guidance to produce re-useable SVA for both Formal and Dynamic Verification.
- Guidance extracted from collateral.
- Guidance must follow SVA LRM.
- Guidance must be tool/vendor independent.
- Current Work
- Future Work

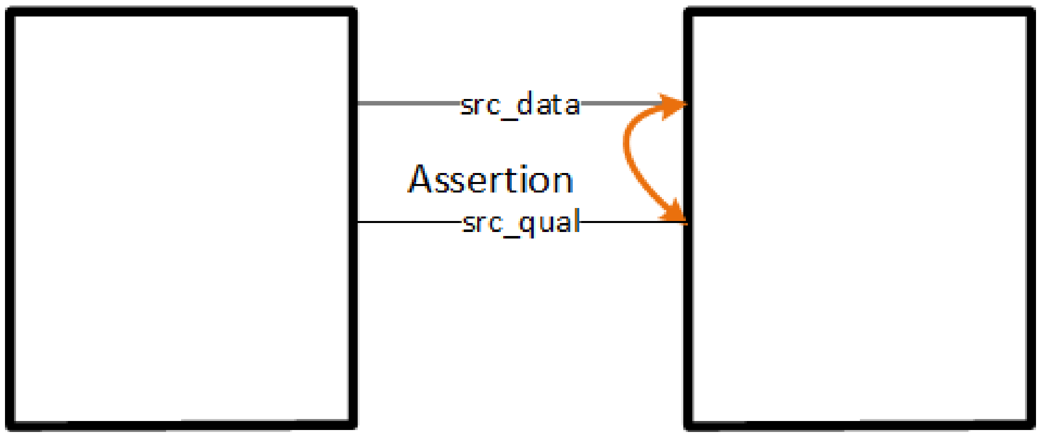


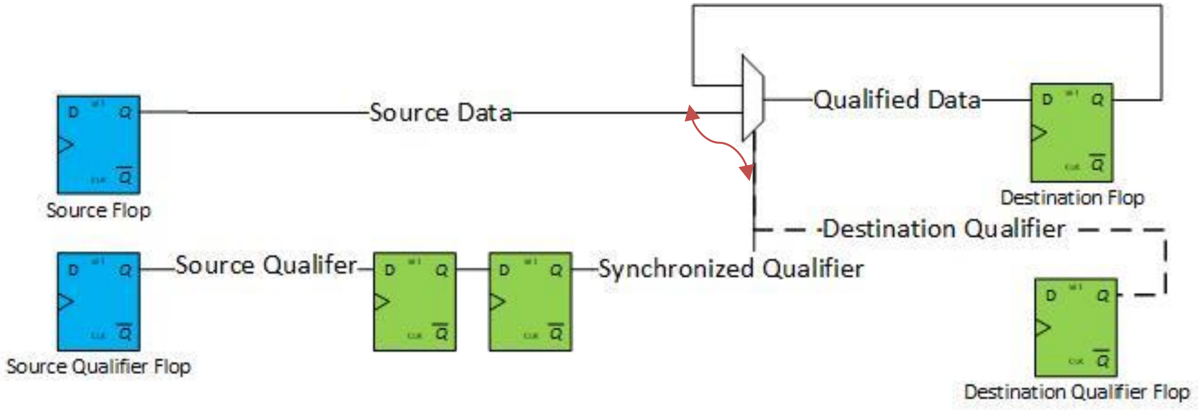
Assertion Subgroup

Assertion

- Possible Integration Scenarios under consideration:
  - Blackbox IP to Blackbox IP at SoC level.
  - SoC level glue logic to Blackbox IP.
  - Blackbox to SoC level glue logic.
  - Full Whitebox verification at IP level.







2.5 Testing Subgroup

Testing Subgroup Mission

Testing

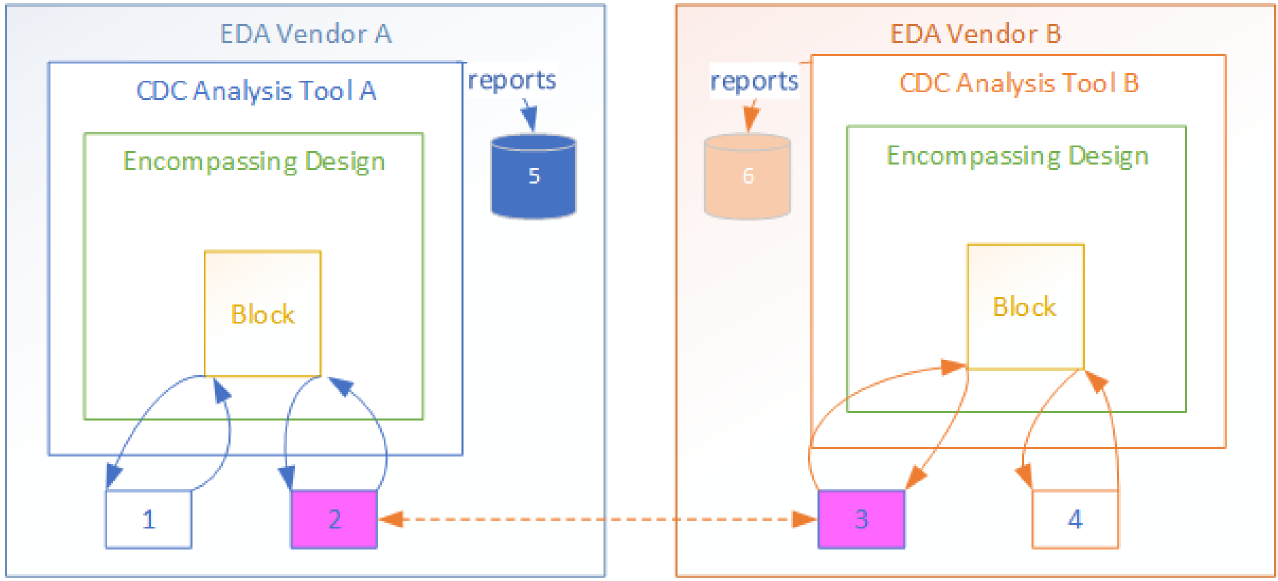
- **Goal**

    1. Evaluate the set of Accellera CDC attributes and protocols for completeness using multiple tools from multiple vendors.
    2. Demonstrate the use of the complete set of attributes and protocols as defined and formatted by other sub-groups.
    3. Provide RTL design examples within which the defined attributes and protocols can be further qualified and evaluated.

Methodology (#1)

Testing

- Testing by Tool Vendor A
  - Step#1 -Perform static flat CDC using Vendor A tool, creating the native block model (1) and Accellera abstract model (2)
  - Step#2 - Perform static hierarchical CDC using native block model (1) & using Accellera abstract model (2)
    - step#2.1 - Compare results flat vs hierarchical with native block model
    - step#2.2 - Compare results of hierarchical native vs Accellera abstract model(s)
  - Step#3 - Accellera to facilitate exchange of Accellera abstract model (2) with another tool for the same IP
    - step#3.1 - Perform static hierarchical CDC using Accellera abstract model by another tool vendor (3)
    - step#3.2 - Compare results of Accellera abstract model (2) and another tool vendor's Accellera abstract model (3)

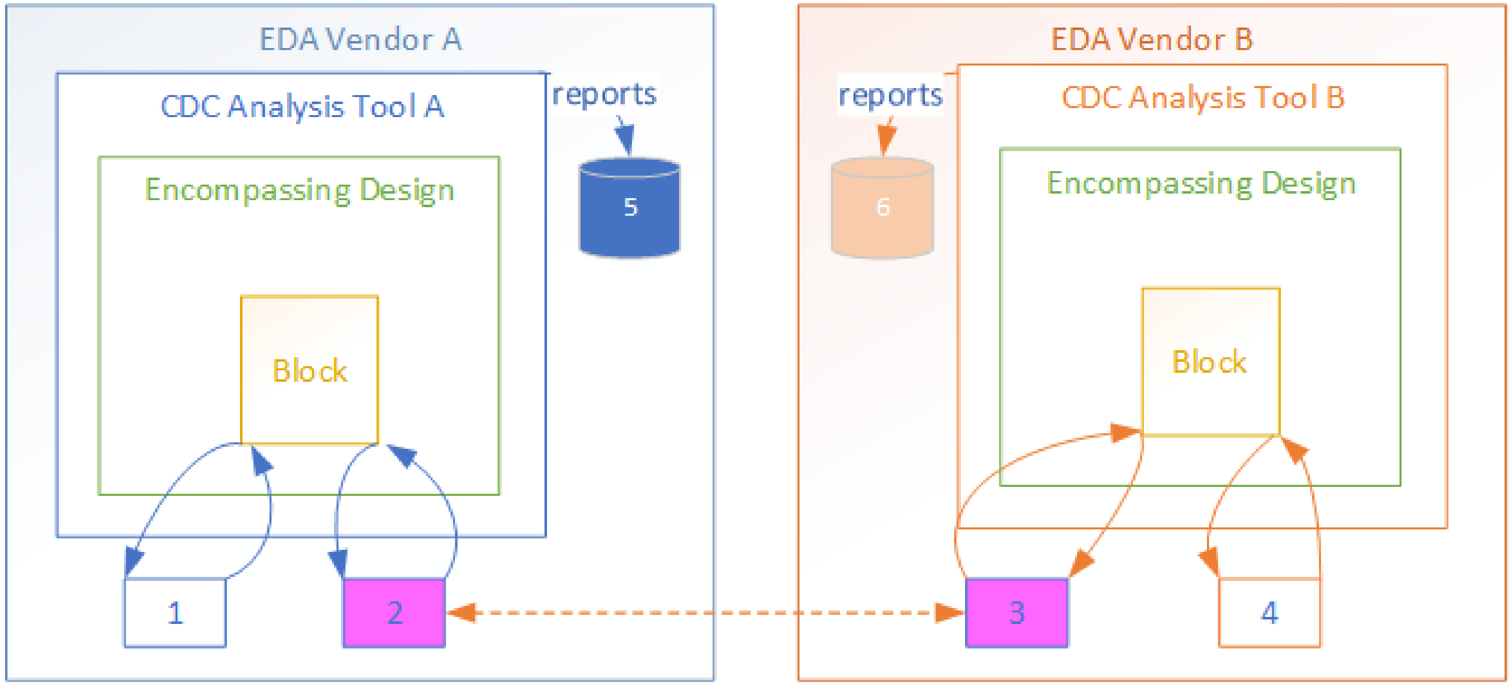


Methodology (#1) [cont…]

Testing

- Step#4 – Report fault model grading per step#2.2 and step#3.2. Fault grading information to be provided by Accellera CDC WG

- This process is of course symmetrical, and Vendor B performs tests to the above description for Vendor A



Methodology (#2)

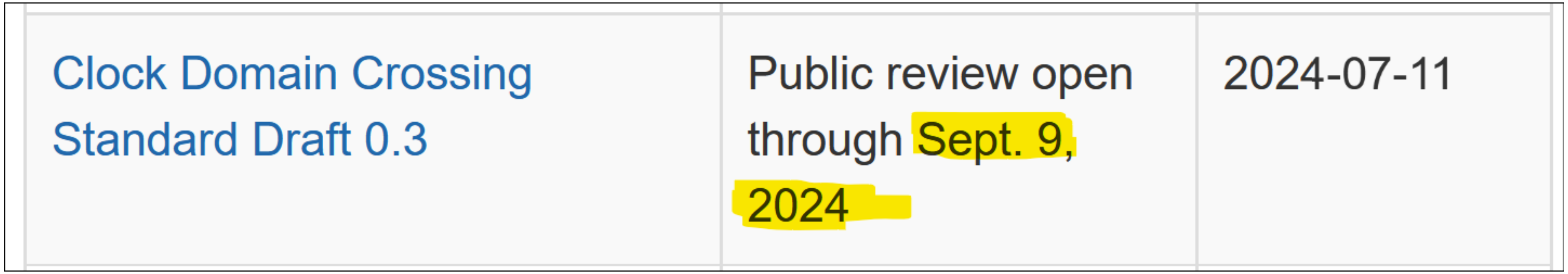
Testing

- Testing by Non-tool Vendors
  - Participants with access to more than one required CDC tool can perform cross tool testing
  - Design IP per list of required interface protocol can be either an inhouse design if available or borrowed for the testing purpose (Accellera to facilitate).
  - EDA vendors to provide their tool support to participants

2.6 Training Subgroup

PLAY VIDEO -3

CDC LRM Draft 0.3 was open for public review till Sept 9, 2024

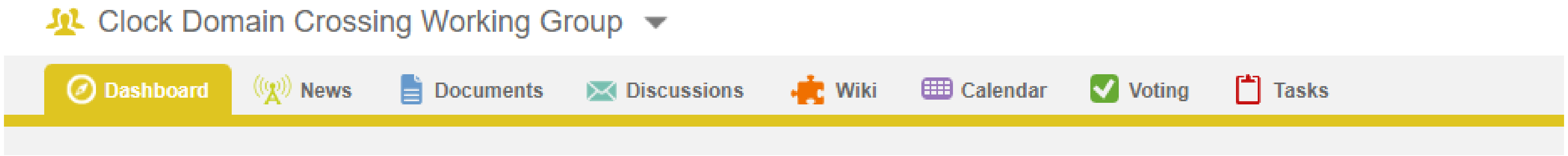


Clock Domain Crossing Standard Draft 0.3	Public review open through Sept. 9, 2024	2024-07-11

https://accellera.org/downloads/drafts-review

Call for Contribution !

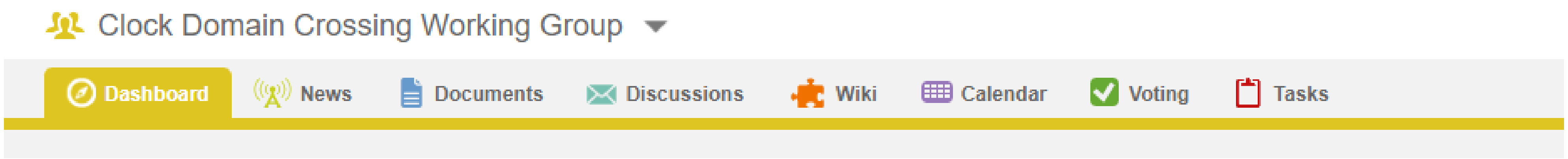
Accellera CDC Working Group



https://workspace.accellera.org/wg/CDC

Call for Contribution !

Accellera CDC Working Group



https://workspace.accellera.org/wg/CDC

Non-Accellera members can join and provide feedback on the standard:
https://www.accellera.org/community

Questions