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A data driven, shift-left CAD Automation approach for expedited integration of Digital IPs for SoCs

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Abstract-

In SoC product development process, RTL signoff is an important step. With the increasing number of products, we needed a next level revolutionary automation framework to standardize the RTL signoff process and expedite it as well for early subsystem integration. Also create a meaningful visualization of PPA output which can help digital designers to understand health of the Soft IPs in a SoC context. This paper presents a comprehensive approach to R&D data collection and management, enabling data-driven solutions and analytics in Digital IP Design Process. We discuss the importance of data collection, data management strategies, and analytics techniques to extract insights from the collected data. The proposed approach is designed to facilitate informed decision-making, improve design efficiency, and reduce time-to-market for Qualifying Digital IP products. Furthermore, proposed Metrics Collection (System) helps to get an end2end data driven view of RTL signoff phase

I. INTRODUCTION

The IP design process involves multiple stages, including synthesis, placement, routing, and verification. We needed an easy-to-use interface that automates the end-to-end process of RTL Signoff steps. Standardize the process and detect anomaly in the design at the early stage of development. Each stage generates a vast amount of data, including log files, reports, and design metrics. Traditionally, designers have relied on manual analysis of these data to identify trends and optimize their designs. However, the sheer volume and complexity of the data make it challenging to extract meaningful insights using traditional methods.

Effective R&D data collection and management are therefore critical components of IP design and development strategy, enabling the extraction of valuable insights from large datasets and informing data-driven decisions. IP data includes design specifications, netlists, and layout files, which are used to create and verify digital circuits. Performing data analytics on IP data can provide valuable insights into design efficiency, performance, and reliability. Moreover, applying machine learning algorithms to the data to identify patterns and trends can help to gain insights, to optimize the performance of their IP blocks.

II. ADVANCED CAD AUTOMATION SYSTEM

Background:

We needed an easy-to-use interface that automates the end-to-end process of RTL Signoff steps. And an advanced automation which creates a 'Push Button' solution for qualification of digital IPs. This is a hard task to create a generic solution in a multi technology mode scenario.
With the application of right software architecture with SOLID principle[1], we created this framework which would significantly reduce the manual effort of RTL Signoff process and create sockets for plugging in Metrics collection systems. This also enables to apply CI/CD software methodology in RTL sign off process.

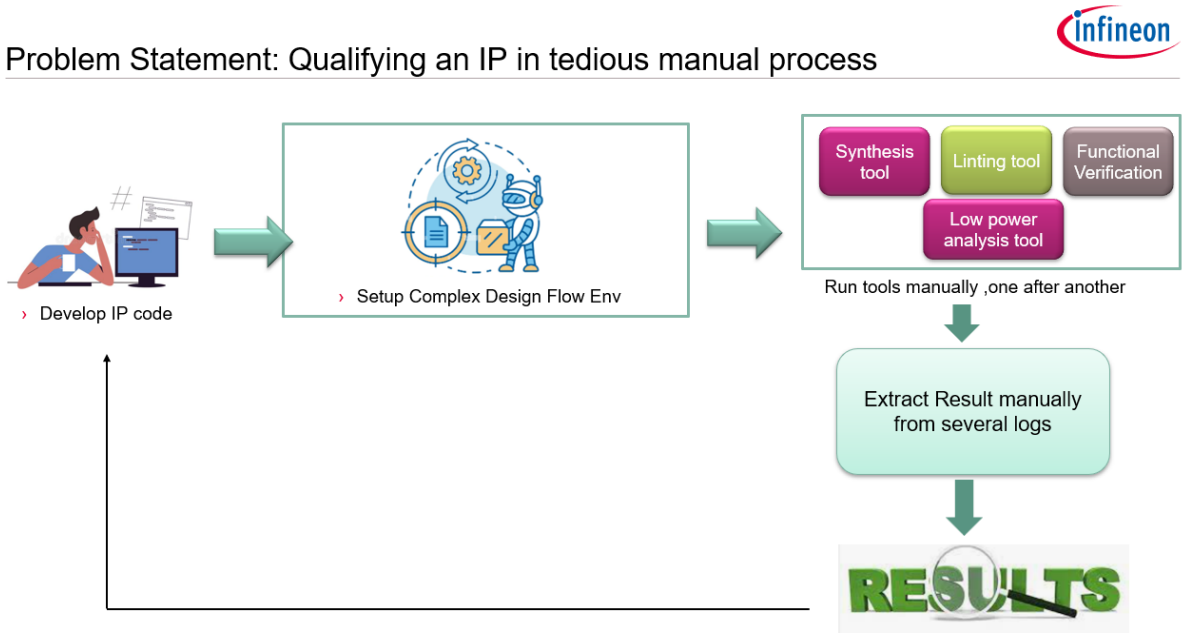

Figure-1 Problem Statement and Need for Automation

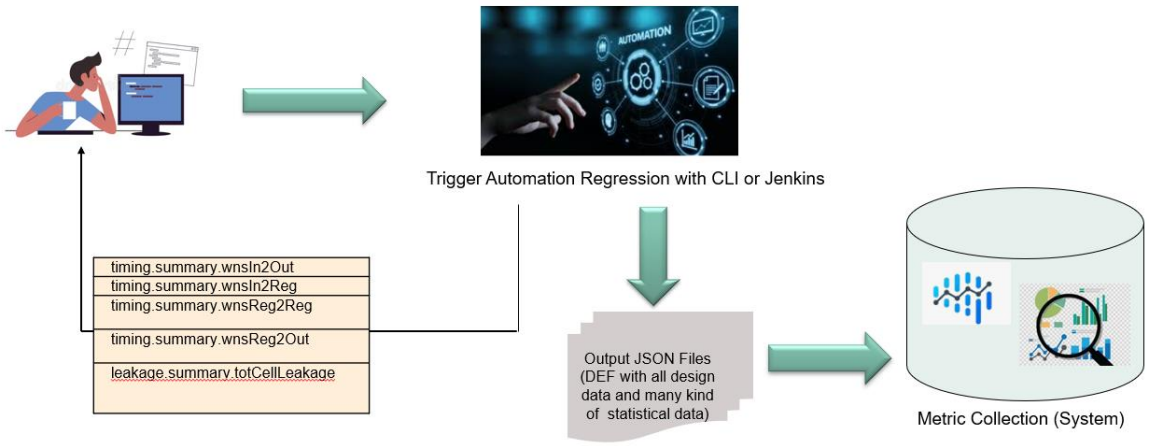

Figure-2 Proposed Automated IP Qualification Solution

Such automation framework relies on a set of standardization. Hence , the flow naturally pushes towards more and more standardization. For example standardized storage of files like floorplan, makes it accessible for automation and we can apply floorplan aware syntheis at the IP level. Another example , standars storage of FSDB files would trigger early dynamic power analysis.

Providing the automation which unifies the interface for a wide range of EDA tools is a challenge in itself. The automation seamlessly allows users to trigger an automation by specifying the minimally required inputs. This abstracts away the difficulty of setup and tool know-hows.

Another challenge in harmonizing the system is foundation IPs and their non-identical views. Its hard to define an automation without a set of standardization. In a scenario where cross vendor foundation IPs are present, we had to define a novel ‘FIP handle engine’ which will support automation on most of the FIPs.

III. Methodology: Metrics Collection System

Our proposed methodology consists of three stages: data collection, data preprocessing, and data analysis.

1. Data Collection: We collect design and process data from various stages of the IP design process, including synthesis, placement, and routing. The data includes log files, reports, and design metrics such as area, power, and timing.

Data collection is the foundation of any data-driven approach. We gather such data from various sources, including:

- Design and simulation tools (e.g., Cadence, Synopsys)
- Various design process steps (e.g., synthesis, validation)

The collected data can be categorized into two types:

- Design data: includes design specifications, netlists, and layout files

- Process data: Includes various in between process steps information

2. Data Management: We preprocess the collected data and transform the data into a suitable format for analysis and fast retrieval.

3. Data Analysis: We apply various data analytics techniques, including data visualization, to extract insights from the preprocessed data. This helps to generate actionable insights that can inform design decisions.

The collected data is stored in database (Metrics Collection (System)) for analytics and visualization. This framework collects the data from different process stages of RTL signoff, to form a holistic data driven view of the development process. Once such data driven view exists data analytics is performed on the top of it. In-depth design data collection helps the digital designers to drill-down design hierarchies & do first level root cause analysis, process effort analysis etc.

IV. RESULTS

Our analysis reveals several insights that can be used to optimize IP design. For example, we identify a strong correlation between synthesis effort and design area, indicating that optimizing synthesis effort can lead to area reduction. We also detect anomalies in routing metrics, which can be used to identify potential routing issues early in the design process.

Figure-3 Timing Total Negative Slack (TNS) Trends View across different calender weeks

Figure-4 Congestion Trends View across different calender weeks

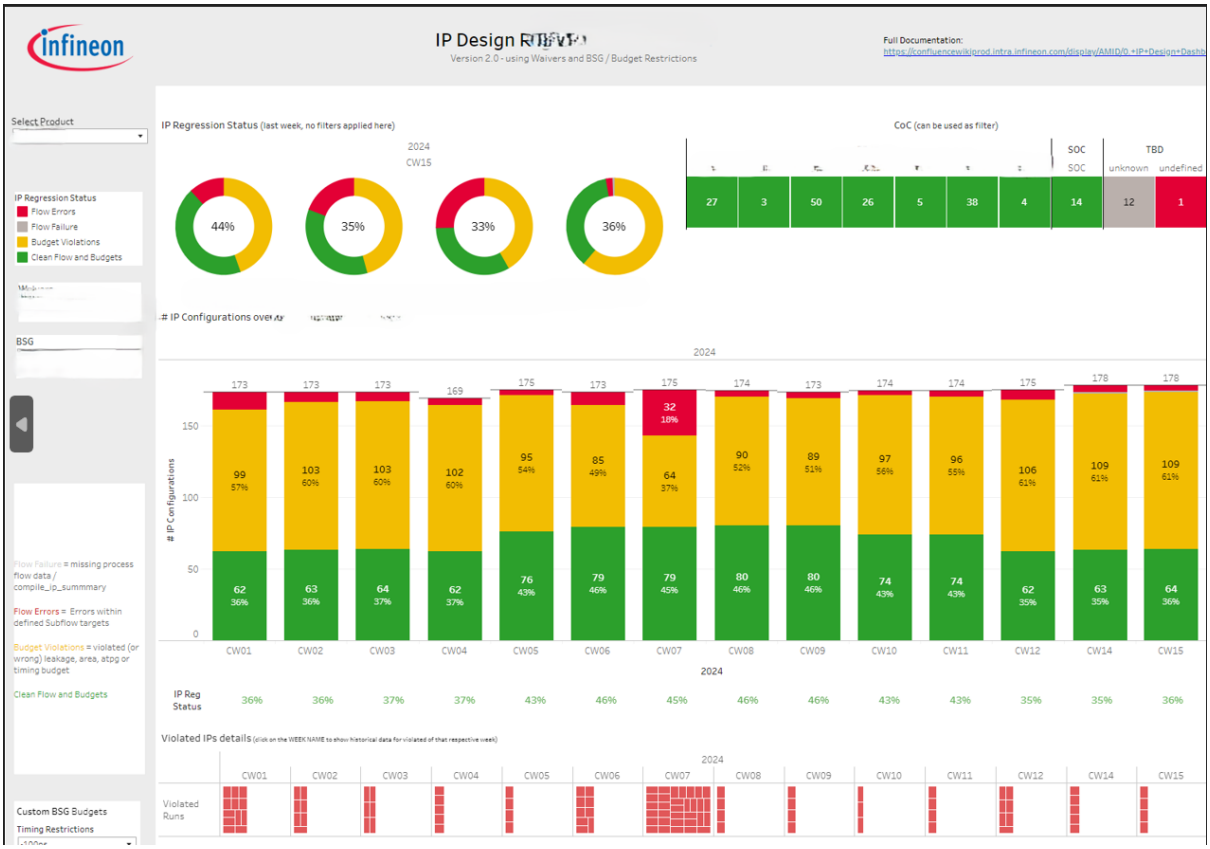

Figure-6 Traffic Lights View of different IP Regression Runs

The data gathered from synthesis runs enables the automated tracking of trends related to congestion, timing, routing, and other aspects across various sets of IP runs, providing a comprehensive and in-depth design data-driven view. This facilitates what-if analysis and allows designers to monitor the IP's progress over time in terms of area, floorplan, and other key metrics. As a result, designers are no longer required to sift through extensive EDA tool logs and reports to analyze the IP run status, thereby eliminating a significant amount of manual effort and increasing their efficiency and productivity by approximately 20%.

V. Conclusion

In this paper, we propose a data analytics framework (Metrics Collection (System)) for extracting insights from IP design data. Our framework enables designers to make data-driven decisions, reducing design time and improving IP quality. We demonstrate the application of our framework on a real-world dataset, showcasing its potential to unlock insights from VLSI design data.

By implementing a structured framework for data-driven design processes, semiconductor companies can reduce time-to-market, improve quality, and lower costs. As the semiconductor industry continues to evolve, the adoption of data-driven insights will become increasingly critical for companies seeking to stay competitive.

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