# GLS Shift Over Through Timing Constraint Verification: A Comprehensive Framework

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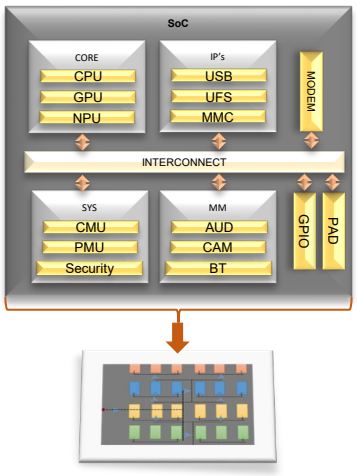
## INTRODUCTION

Modern **SoCs integrate heterogeneous IPs across multiple asynchronous clock** domains, making timing closure increasingly challenging.

While **STA and GLS are essential** sign-off steps, **STA relies on accurate SDC constraints** and **GLS is computationally expensive** and often misses constraint errors, allowing hidden timing risks to persist.

**Timing Constraint Verification (TCV)** systematically ensures constraint accuracy and completeness across the RTL-to-GDSII flow, improving timing closure efficiency and SoC reliability.

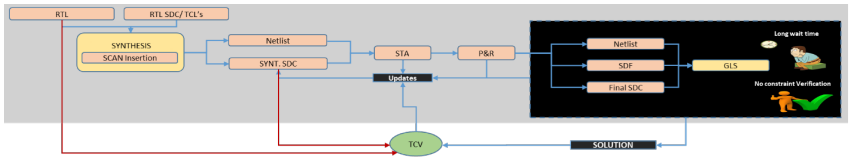



## OBJECTIVES

**Timing Constraint Verification (TCV)** introduces an automated methodology that **validates SDC timing constraints and exceptions directly against the RTL design at early stages.**

**Instead of relying solely on post-synthesis netlists**, TCV interprets SDCs in simulation, correlates them with the RTL hierarchy, and **models timing relationships for multi-cycle, false, and clock-group constraints.**

**By dynamically inserting delay and stability checks**, TCV detects incorrect or incomplete constraints early, enabling precise debug and preventing downstream design and silicon issues.

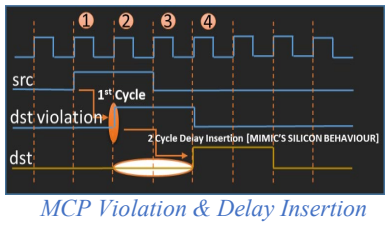



## FEATURES

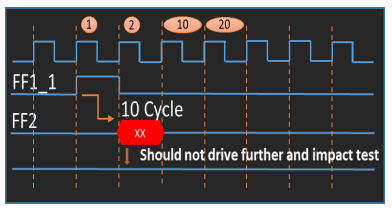
- **Multi-Cycle Path Verification:** Validates register update in define cycle
- **False Path Verification:** Detects unintended destination toggles
- **Clock Groups:** Validates async clock constraints
- **Set_Case Analysis:** Ensures correct constant propagation
- **Quasi-Static Signal Check:** Reports quasi-static signals for review
- **SDC–RTL Mapping:** Enables seamless hierarchy correlation
- **Translate_on/off:** Prevents constraint–RTL mismatches
- **SYNC Filters:** Handles reset/data sync, avoids X-propagation
- **Clock Filtering:** Excludes inactive test clocks (SCAN/BIST)
- **Async Clock Handling:** Manages same-root clocks across modes

## RESULTS

- Detection of **Missing Generated Clock** Definitions
- Identification of **Missing MCP** Constraint
- Identification of Clock Error-1 *(Wrongly marked **asynchronous clocks detected between 2 synchronous clocks**)*
- Identification of Clock Error-2 *(Wrongly marked **synchronous clocks detected between 2 asynchronous clocks**)*
- Identification of **incorrect exercised clocks**
- Observation of **Glitch Over CDC Path**
- Verification of **Double synchronizer Behavior**




*MCP Violation & Delay Insertion*



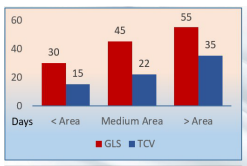

*False Path with X Insertion*

## CONCLUSIONS

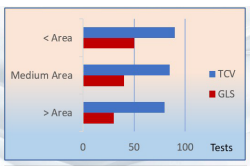
**Improved Runtime:** TCV Delivers results significantly faster than GLS, enabling earlier debug and analysis

**Higher Coverage**: TCV achieves broader verification completeness, identifying issues missed by GLS

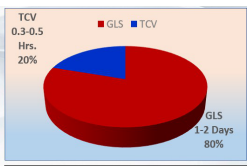
**Reduced Manpower**: TCV minimizes manual debug efforts and improves overall project efficiency




Significant improvement in Run Time




Enhanced Test Coverage with GLS v/s TCV




Reduce Debug and Manpower Time

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