RISC-V Reuse Made Easy by Interface Generation and Integration Automation

Ares Tahiraga, Said Llukaj, Wei Zhao, Endri Kaja, Sebastian Prebeck, Wolfgang Ecker

Infineon Technologies AG

accellera SYSTEMS INITIATIVE

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INTRODUCTION

IP reuse brought hardware design productivity a big step forward by simplifying reuse. Unfortunately, it is not as simple as it seems: each IP must be understood, configured and then connected with the signals of the SoC. Despite de-facto standards for on-chip busses, scan signals, etc., integration is challenging in one major way: flexible interfaces such as APB, AHB, and AXI from the ARM family allow for variations in implementation, offer numerous configuration choices, and can be often tailored to enhance performance, power, area (PPA), or to address specific safety and security needs.

For RISC-V, functional configuration is relatively easy due to its modular ISA and profiles that offer pre-configured feature sets. However, the integration of RISC-V IPs remains challenging due to the fact that each RISC-V IP comes with its own communication and infrastructure demand.

OBJECTIVES

To tackle these challenges, we have developed generic modules to connect the RISC-V to its external world. Since modern Hardware Description Languages (HDLs) like SystemVerilog lack support for generic programming concepts, such as optional ports or automated object feature propagation, we have developed a Python-based code generation framework, called MetaRTL, to provide these features as a generation step for HDLs.

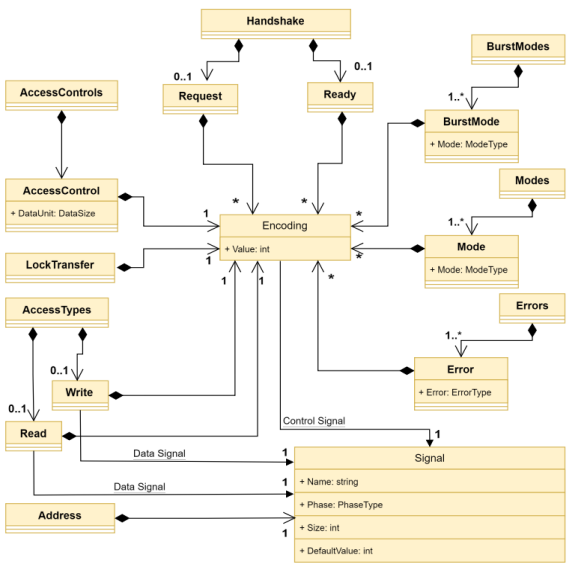
This generation framework is not only used to generate the RISC-V IP but also to generate the interface connections of the RISC-V to the SoC using introspection techniques also not supported by HDLs and HGLs. The goal is to create a framework able to generate different variants of CPU cores and to speed up the design cycles via automatic IP integration.

CONCEPT

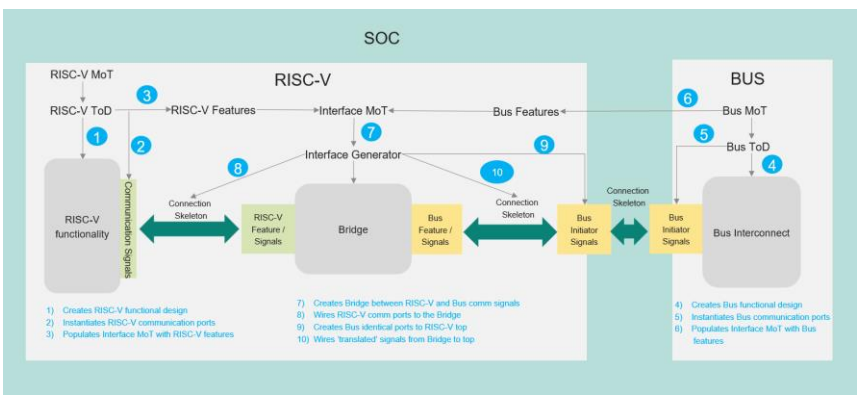
Two key observations:

1. Common bus protocols share a unified semantic model

2. CPU's communication signals implement a protocol of its own, conform to this model



RESULTS



Faster Cycles for:

1. Testing and regression
2. Benchmarking
3. Design Space Exploration
4. Product integration

CONCLUSIONS

We presented a model-driven, feature-oriented Bus Interface Generator that decouples RISC-V IP functionality from interconnect communication, enabling automated, single-pass generation of protocol-compliant interfaces across APB/AHB/AXI. This approach enables scalable exploration, benchmarking, and faster product integration. The method generalizes to other IP classes (e.g., DMA, accelerators, DSPs).

Future work will extend protocol coverage and add automated instrumentation for quantitative PPA and timing profiling. Overall, systematic interface generation makes plug-and-play RISC-V reuse practical and maintainable at scale.

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ISOLDE RISC-V