An Enhanced DV Approach for Effectively Verifying High Speed, Low Power MIPI-MPHY 5.0 Designs

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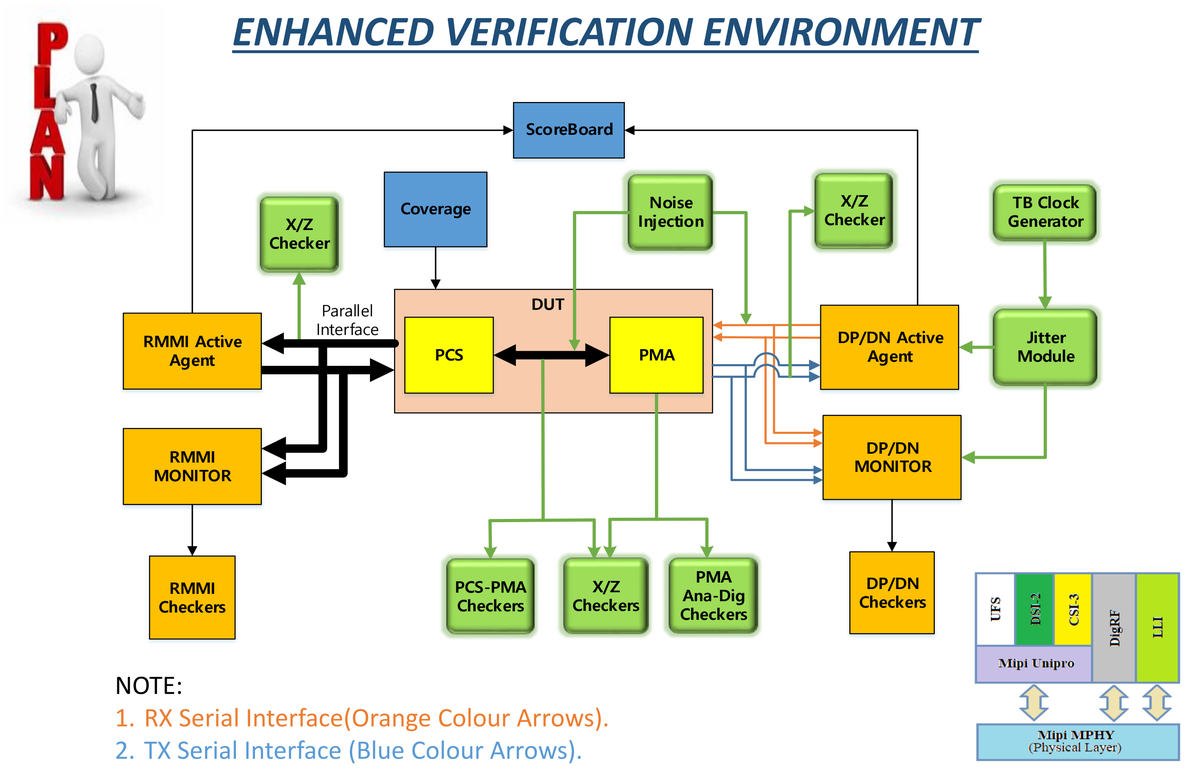
PROBLEM STATEMENT

ENHANCED VERIFICATION ENVIRONMENT

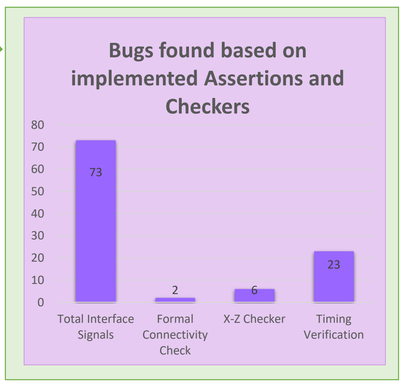


NOTE:
1. RX Serial Interface(Orange Colour Arrows).
2. TX Serial Interface (Blue Colour Arrows).
3. Components added in existing Test Bench (Green Colour Box).

IMPLEMENTATION DETAILS AND RESULTS

Interface Connectivity and Timing Checks

- MPHY Design consists of PCS and PMA (Analog-Digital) Interface.
- Signal Connectivity and protocol related checks across I/F become mandate.

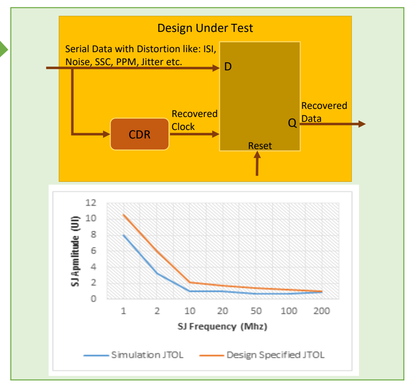


FSM Based Scalable Test Bench Architecture

- Each MPHY FSM State is defined as a separate sub-sequence.

Jitter Module for CDR Stress Testing

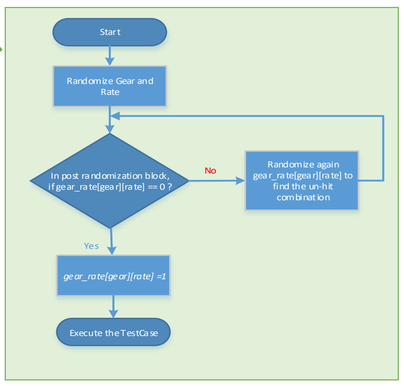
- Critical to assure Receiver Logic works well within tolerance limits set by Protocol.
- Introducing Jitter/SSC/Noise on incoming Serial Data.



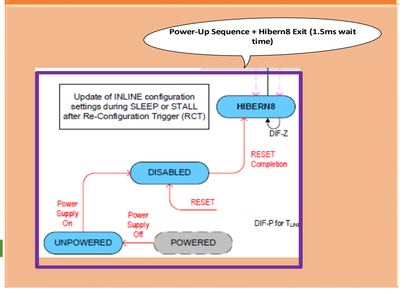
Approach for faster Functional Coverage Closure

- Test Case Ranking and custom regression suite generation
- An array based coverage collection. Ex:

Supported Gear = {1,2,3,4,5}, Rate = {0,1};



Increasing Regression Throughput using EDA Tool



- Using Snapshot Feature of simulator.
- 5.1% to 30% reduction in CPU time.
- 15% reduction in regression run time tested with a test suite of 1100 runs

IMPLEMENTATION DETAILS AND RESULTS

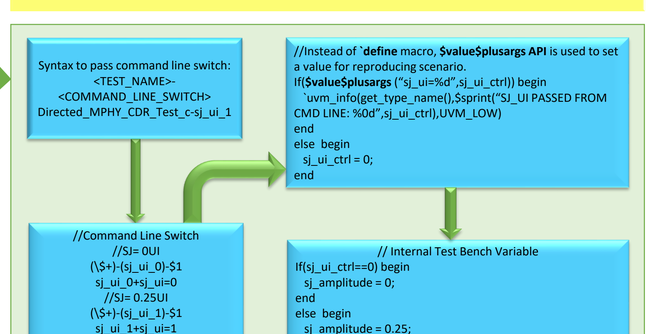
High Precision Analog Models

- MPHY PMA is a typical AMS Design.
- Analog behavior is modelled in a way to closely mimic the real functionality for digital simulation purpose using 3rd party utility.

Parameterized Test Sequences

- Reproduction of scenario needs Test Bench change and compilation.
- Maintenance and functional coverage closure with such Test Bench architecture is difficult.

Jitter		SSC	Frequency Offset
RJ	SJ		
0	0	0	0
0.12UI	0.25UI	0	+300ppm



CONCLUSIONS

- Test Bench has become **efficient and effective** in fulfilling Design requirements.
- Unearth some really critical **bugs**, which could have led to excess power consumption.
- Regressive CDR testing ensured **high quality** Jitter Tolerant Receiver.
- Runtime switches, save and restore option, coverage handling helped in **on-time** verification closure.
- The enhancements mentioned can be used as a good reference for verification of other serial protocols like **PCIE, USB** etc.

FUTURE SCOPE

- Enhanced CTS support for PRBS7 and PRBS15 patterns
- MIPI MPHY Future Generation Updates
- Further Enhancements to Coverage Module

REFERENCES

- mipi_M-phy_specification_v5-0.pdf, by MIPI Alliance
- SystemVerilog 3.1a Language reference Manual
- https://www.academia.edu/30128384/SERDES_Rx_CDR_Verification_using_Jitter_Spread_spectrum_clocking_SSC_stimulus

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