

INTRODUCTION

Portable Stimulus (PSS) is typically pitched as the solution to port test intent across different validation platforms. This paper details how one could adopt PSS into their existing UVM IP validation regime for efficient Scenario Generation, Control and Reproducibility. Test stimulus can be distributed across the PSS tool and the UVM testbench framework. Test scenario creation and orchestration can either (1) entirely be done in PSS, where handoff happens at the UVM atomic sequences OR (2) in a hybrid PSS-UVM setup, where handoff is at the UVM virtual sequence. This PSS to UVM handoff point could be a sliding scale, tailored to any IP or SoC validation goals. Stimulus intent could be modeled in DSL, and a PSS processing tool can generate stimulus/tests from the model. The coverage from PSS tests can be analyzed prior, and the best tests selected for UVM mapped simulations.

An Intel Memory-IP library testplan was executed and other validation capabilities, tested using a PSS/DSL's OOP & AOP constructs. This paper highlights this unique PSS flow, leveraging Synopsys' VC Portable Stimulus (VCPS) tool capabilities to supplement a robust framework, facilitating deterministic & reproducible randomness in continuous integration systems (Gatekeeper) – saving Intel dollars!

PROBLEM STATEMENT / OBJECTIVES

Drawbacks of conventional UVM based Functional Verification:

Test Redundancy: SV random seed-based stimulus may partly or wholly retake the same values across different seeds. This results in redundant simulations that wastes compute cycles with no coverage improvement.

Test Reproducibility: SV UVM test-suites and their associated testbench counterparts may change multiple times throughout a project lifecycle. As code changes across validation milestones and bug fixes, test behavior may change. The same seed may produce different stimulus across different versions of the simulation, making reproducibility difficult and loss of feature-specific tests.

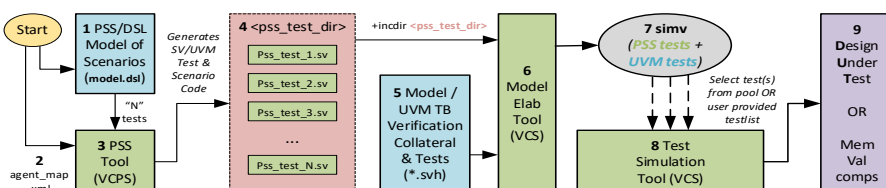
UVM sequence transition & branching coverage: Modeling and tracking coverage to gain visibility at a sequence transition level in an easy, scalable and effective way is non-existent. Focused UVM tests are only as good as the test-writer's ability or how a scenario is depicted in the test plan. There is no real indicator to a validator that all paths or trajectories a test *could take* have been taken, tested and most importantly covered.

This paper showcases how PSS can be used in an existing UVM framework to overcome the above issues by generating unique and reproducible tests from validation scenarios. Pre-elab / pre-sim coverage, can be used as a metric to QA stimulus even before a simulation is run.

RESULTS - I

Mode 1: Scenario Orchestration in PSS and UVM handoff at atomic sequence: In Fig below, DSL Modeled Scenarios (1&2) fed to the VCPS PSS Tool (3), generates multiple tests (4) with unique test paths & random sequences. These are included in the existing UVM Model (5) along with hand-written UVM tests. All tests/code are elaborated using VCS (6). The resulting simv (7) contains all test possibilities. Validator picks test (8) to inject into DUT/IP (9).

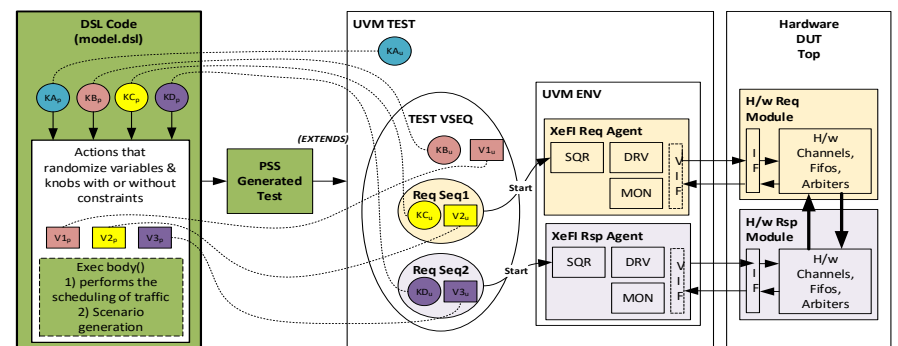
These can be fixed-behavior UVM tests or a coverage-report-based PSS test that accurately hits a test plan scenario. Each PSS test, contains fixed intent (modeled in DSL) while UVM only implements the target IP bus protocol. Almost all of randomization happens in PSS, tests are unique by generation, fully reproducible once mapped and provide sequence transition path coverage in addition to functional coverage of stimulus.



RESULTS - II

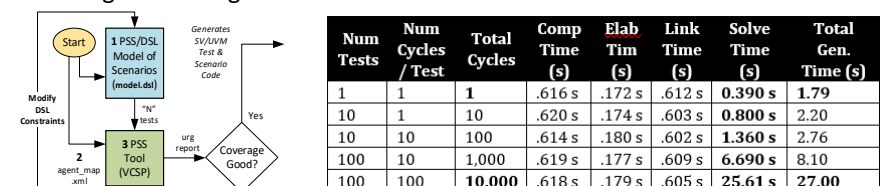
Mode 2: PSS-UVM Hybrid Solution, UVM handoff at Virtual Sequence:

The Fig below shows how PSS (K^*) knobs control their UVM counterparts (K^*). Test flows are generated by VCPS (deterministically) while UVM provides transaction randomization. (**Hybrid solution!!**) Test writers may thus use PSS without knowledge of the UVM TB. Tests are fully reproducible up to the PSS/UVM control knob level and simulations perform additional controlled randomizations.



RESULTS - III

VCPS URG reports are generated for solve or pre-run-time analysis. PSS scenario model could be iteratively modified, or tool could generate more tests from same scenario to improve stimulus and path coverage. Tool generation times are also shown. Single test template with 1 random cycle takes 0.3s to generate stimulus, while 100 test templates with 100 random variations per template takes only 25.6s. Thus, stimulus coverage indicators can be analyzed prior to launching even a single simulation.



Iteration #1: PSS generation coverage for 10 tests

Category	Expected	Uncovered	Covered	Percent
Variables	42	2	40	94.44
Crosses	480	293	187	38.96

Crosses for Group pss_top::base_fm1_a::fi_pkt_cg

Cross	Expected	Uncovered	Covered	Percent	Goal	Weight	At Least	Print	Missing	Comment
CR_cmds1	480	293	187	38.96	100	1	1	0		

Iteration #2: PSS generation coverage for 30 tests (Improved)

Category	Expected	Uncovered	Covered	Percent
Variables	42	1	41	97.22
Crosses	480	293	187	38.96

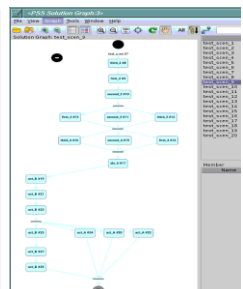
Crosses for Group pss_top::base_fm1_a::fi_pkt_cg

Cross	Expected	Uncovered	Covered	Percent	Goal	Weight	At Least	Print	Missing	Comment
CR_cmds1	480	293	187	38.96	100	1	1	0		

CONCLUSIONS

Employing PSS to supplement a UVM framework overcame the shortcomings of a typical SV env setup. 300 automatically generated PSS tests beat the black/white box functional UVM coverage compared to Manual UVM tests, cutting down development time significantly. Tool also provides a visual depiction of the test trajectories previously not seen in simulation.

Case I: UVM Testplan / Testsuite Coverage Results - I	Case 2: PSS Auto-Generated Test Coverage Results - II
(Average = 98.34%) (Total tests = 300)	(Average = 99.58%) (Total tests = 300)
Functional Black Box Coverage I(a)	Functional Black Box Coverage II(a)
fi_bb_cov1::cg_cmd_pkt 96.34%	fi_bb_cov1::cg_cmd_pkt 96.76%
fi_bb_cov1::cg_comp_pkt 100.00%	fi_bb_cov1::cg_comp_pkt 100.00%
fi_bb_cov1::cg_data_rsp_pkt 100.00%	fi_bb_cov1::cg_data_rsp_pkt 100.00%
Functional White Box Coverage I(b)	Functional White Box Coverage II(b)
fi_req_to_arb_wb_cov1::req_to_arb_2ch 99.80%	fi_req_to_arb_wb_cov1::req_to_arb_2ch 99.95%
fi_req_to_arb_wb_cov1::write_arb_2ch 90.61%	fi_req_to_arb_wb_cov1::write_arb_2ch 100.00%
fi_rsp_protocol_layer_wb_cov1::protocol_layer_cmd 100.00%	fi_rsp_protocol_layer_wb_cov1::protocol_layer_cmd 100.00%
fi_rsp_protocol_layer_wb_cov1::protocol_layer_rsp 100.00%	fi_rsp_protocol_layer_wb_cov1::protocol_layer_rsp 100.00%
fi_rsp_protocol_layer_wb_cov1::protocol_layer_state 100.00%	fi_rsp_protocol_layer_wb_cov1::protocol_layer_state 100.00%



REFERENCES

- PSS - https://www.accellera.org/images/downloads/standards/Portable_Test_Stimulus_Standard_v20.pdf
- DSL - https://en.wikipedia.org/wiki/Domain-specific_language
- VCPS - https://spdocs.synopsys.com/dow_retrieve/latest/vp/vc_ps/PDFs/vcps_user_guide.pdf
- <https://www.synopsys.com/content/dam/synopsys/verification/datasheets/costart-portable-stimulus-ds.pdf>