

Average outstanding requests

DRAM Refresh Counts

Average

Average

Unlike funct

simulations

unique and self

descriptive error

or throughput

Notably, 90% of

falling into a "<mark>Big</mark>

DDR Activate count

failures arise from

nmon bottlenecks

et" category

discrepancie

signatures, showing up

DRAM Page Hits

DRAM

Role of AI in SoC Performance Verification(PV)

Sharada Vajja, Raghu Alamuri, Saksham Mehra

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Time to run full usecase v/s only cluster centre snippets

GOOGLE LLC



0.0

1.0

2.0

2

4 4.0 0.0

20.0

52.0

23.0

Each row of the table represents the stats captured co window in the complete usecase

0.0

13.0

3.0

1.0

0.0

755.2

627.2

985.6

883.2

2.5 5.0

7.5 10.0 12.5 15.0

on the plot represents a snippet(time i full usecase run (plotted in terms of the ents calculated from window stats). Each esents a cluster and each cross is the

515.0

4995.0

2146.0

989.0



IP Max Outsta (IP MO)

(FAR MO)

Sample statistics/configuration settings captured for every failing test

during runtime

along with RTL configuration

Each of the failing

test thus becomes

a datapoint, with collected stats as

features/dimension

settings.

average_outst (wr_avg_os)

DRAM Cac Hits

MMU Hits

n a usecase

Prioritizing Debugs

houahput

Elbow method is

optimum k, and

the reduced

dimensionality

dataset is fed

model

into the k-means

Fixed AxID (sameaid)

it enable (SLC Hit

used to

determine



Address pattern (Linear/Random)

(FAB VC)

t2 😽 🏲

4>

4 1

t4 🕌

time



Google

Authors' contacts : msaksham, raghualamuri, sharadav @google.com