System-Level Power Estimation of SSDs under Real Workloads using Emulation

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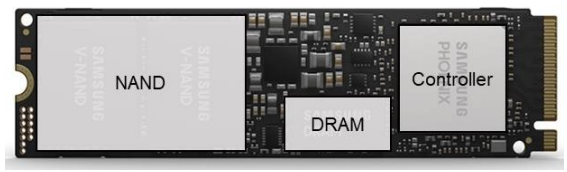
2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES
SAN JOSE, CA, USA
FEBRUARY 27-MARCH 2, 2023

INTRODUCTION

- Motivation
  - Due to faster data transfer speed requirements, the performance of Solid-State Drives (SSDs) is constantly increasing
  → PCIe 5.0 protocol SSD Seq. Read: 13,000 MB/s [1]
  -Higher performance often results in higher power consumption, which is why accurate power estimation is important.

- Objective: Power estimation of SSDs under real workloads
  - SSD components: Controller (SoC), NAND (Memory storage), DRAM (Cache)
  - Realistic scenarios: Seq. Read/Write, Random Read/Write

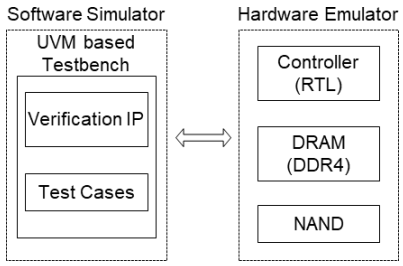


Components of an SSD

VERIFICATION METHODOLOGY

Requirements
- Handle large design size of SSD controllers (tens of millions of instances).
- Supports the firmware.
- Simulation time needs to be relatively long (100ms) (peak power can occur on corner cases).

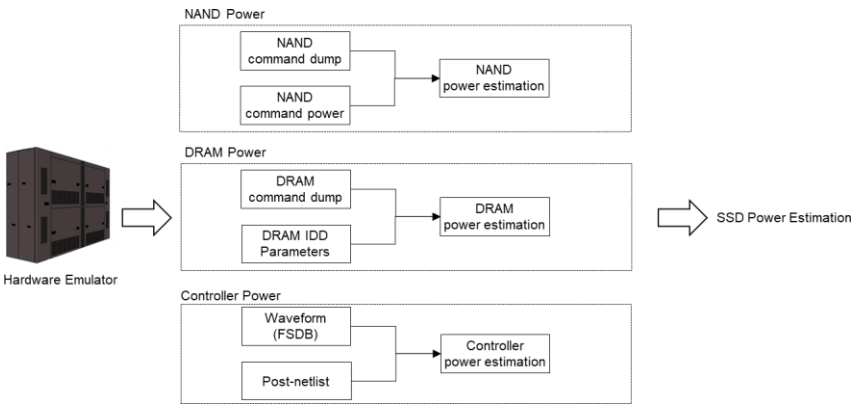
→ Our solution: Emulation based hardware/software co-verification



Verification Environment

SSD SYSTEM-LEVEL POWER ESTIMATION

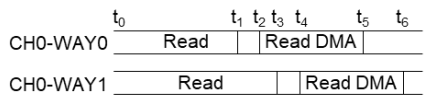
- Estimate each component's power
- NAND/DRAM: Use silicon measured command power
- Controller: Standard SoC power estimation flow



Overview

NAND/DRAM POWER ESTIMATION

Memory subsystems
- Command info: modify behavior models to dump internal status register value changes (NAND: tPROG/tR/tERS/DMA, DRAM: PRE/ACT/RD/WR)
- Calculate each command's power



CH0 Dump Log
Time, Way0, Way1
t_0, Read, Read
t_1, Idle, Read
t_2, Read DMA, Read
t_3, Read DMA, Idle
t_4, Read DMA, Read DMA
t_5, Idle, Read DMA
t_6, Idle, Idle

Example of NAND Operation

RESULTS

Applied to commercial SSD and compared estimations with silicon measured power
- Identical product F/W used during estimation and measurement
- Maximum 5% error for average power
- Maximum 8% error for peak power

Power estimation error (%)

Component	Sequential Read		Sequential Write		Random Read		Random Write	
	Average	Peak	Average	Peak	Average	Peak	Average	Peak
NAND	-3	-12	5	-5	-9	-7	5	-3
DRAM	-6	-22	5	-9	-10	-16	-10	-13
CTRL	1	0	0	-2	0	-4	-3	-5
Total	-2	-8	3	-4	-5	-5	2	-4

CONCLUSIONS AND REFERENCES

We use silicon measured command power to estimated memory subsystems of an SSD. We obtain the command info by modifying the memory behavior models. Emulation is used to accelerate the verification time. Results show that the average and peak power was estimated with a maximum error of 8%.

[1] Samsung Press Release, "Samsung Develops High-Performance PCIe 5.0 SSD for Enterprise Servers", 2021.
[2] A. Jain, P. Gupta, H. Gupta and S. Dhar, "Accelerating System Verilog UVM Based VIP to Improve Methodology for Verification of Image Signal Processing Designs Using HW Emulator," International Journal of VLSI design & Communication Systems, vol. 4, no. 6, Dec. 2013.
[3] Synopsys, "PrimePower User Guide," 2021.
[4] C. Selvidge and V. Chobisa, "The Veloce Strato Platform: Unique Core Components Create High-Value Advantages," Whitepaper, Siemens EDA

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