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Functional Coverage Closure in SoC Interconnect Verification with Iterative Machine Learning

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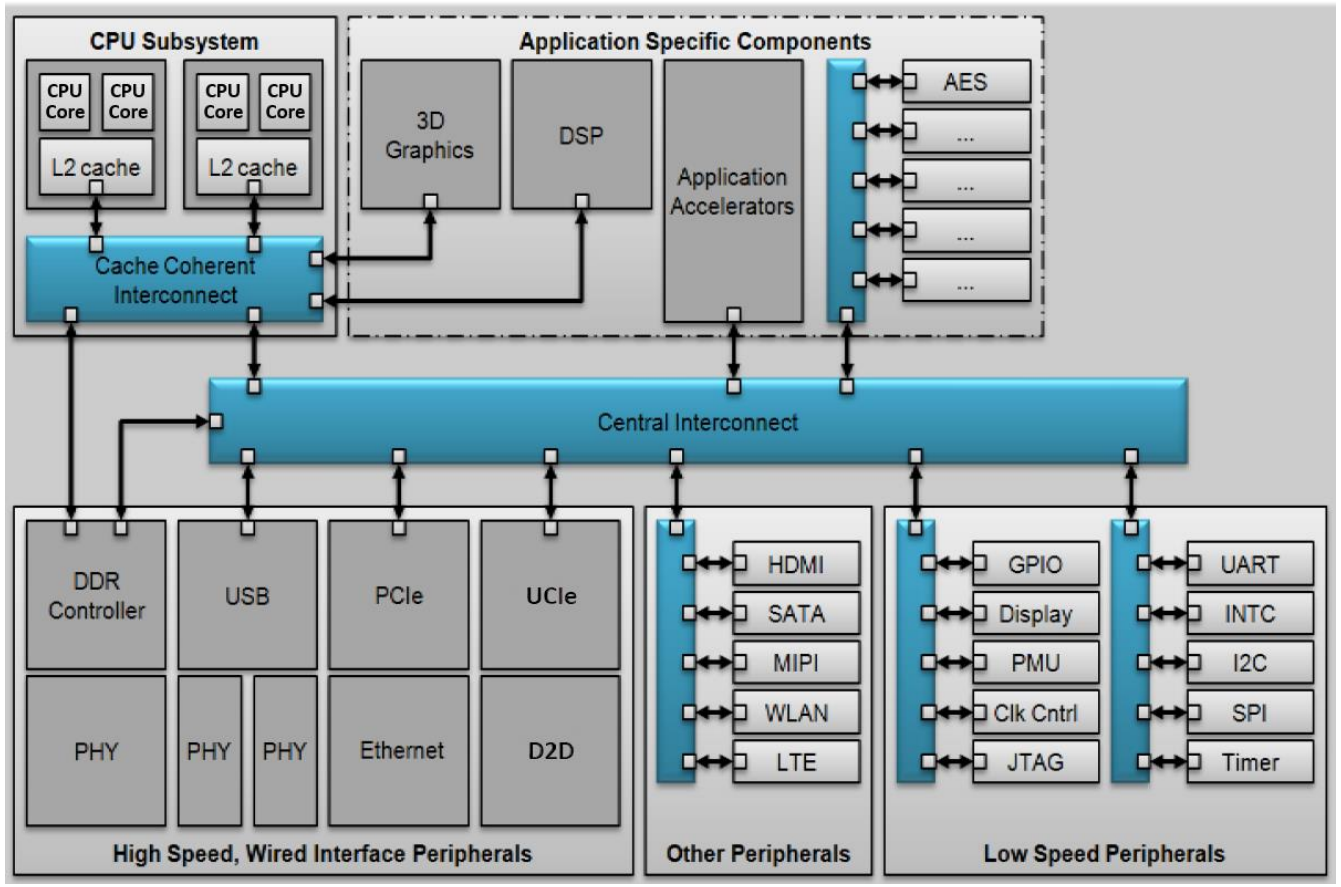
SoC Interconnect

- Interconnects subsystems on a System-on-Chip
  - Numerous components
  - Diverse protocols
- Demands high performance & power efficiency
- Requires early verification



Challenges in SoC Interconnect Verification

- Design complexity
  - Hundreds of masters and slaves connected
  - Multiple bus interface protocols (e.g., AXI, AHB, ACE, CHI)
  - Various attributes of transactions (e.g., address, direction, size)
- Verification complexity
  - Enormous number of routing scenarios

➡ Huge & thorough functional coverage model

Constrained Random Simulation

- Generates random transactions
  - Random routing paths & transaction attributes
  - Simulated & validated according to design specification
- A coverage bin for testing a specific routing/transaction scenario
  - Full randomization → Repetition, CPU time ↑
  - Directed tests → Human engineering effort ↑

➡ Iterative Machine Learning approach

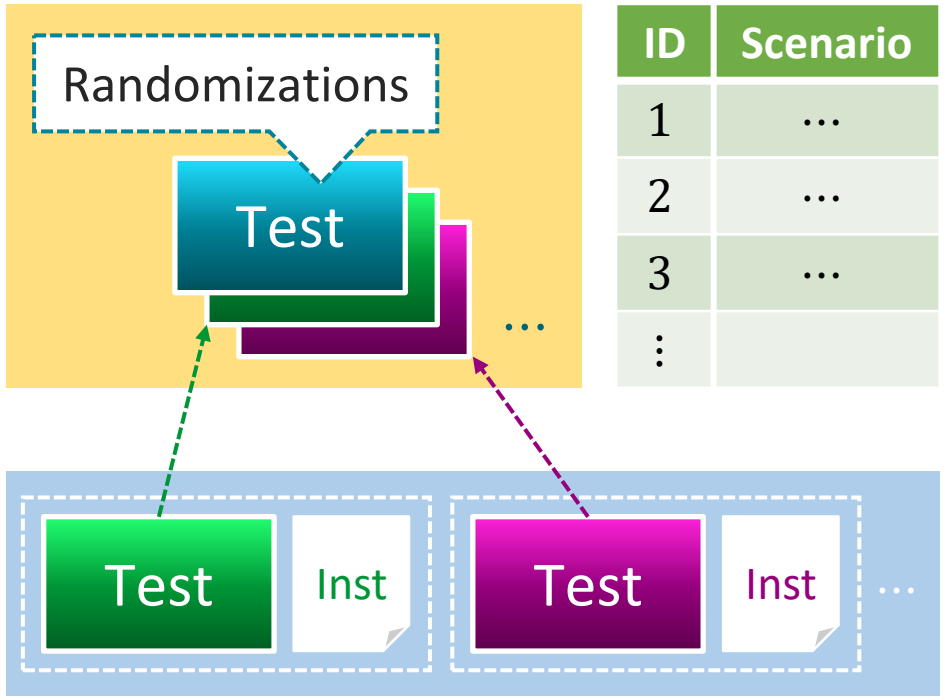
Proposed Iterative Machine Learning

Input (Initial)

- A Regression: Suite of random tests
- Target specification: List of target scenarios
  - Simulation settings of tests
  - Combinations of values of random variables

Output (Each iteration)

- A new regression that extends the original
  - Subset of tests + Instructions for Simulator



Proposed Iterative Machine Learning Flow

1. Simulate regression

2. Collect results

- Simulation traces
- Status information
- Coverage results

ID	Scenario	Satisfied?
1	…	No
2	…	Yes
3	…	No
⋮		

3. Learn from data
   - Which scenarios satisfied?
   - How difficult?

Steps 2 - 5: A feature of SimAI

Proposed Iterative Machine Learning Flow

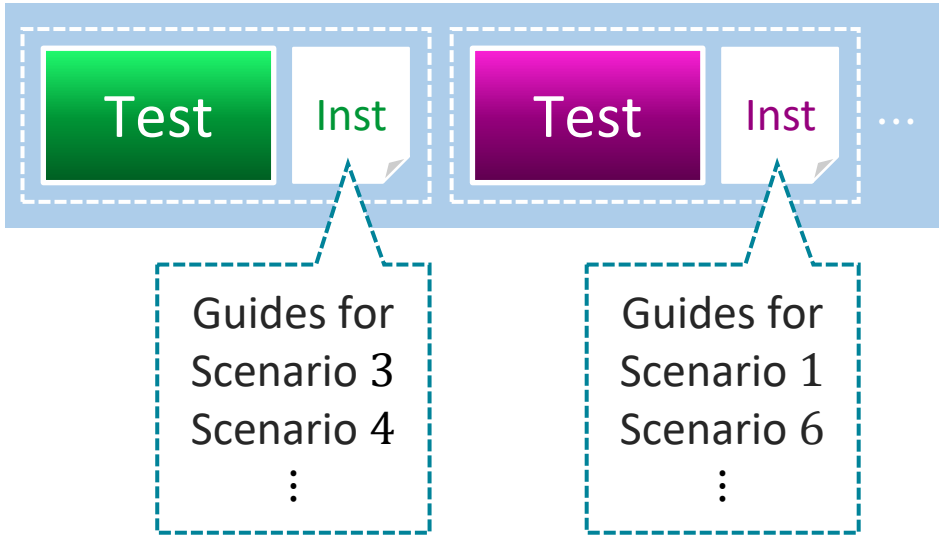
4. Adjust targets

ID	Scenario	Satisfied?
1	$X = 1, Y = 0, Z = 1$	No
2	$\cdots$	Yes
3	$A = 1$	No
4	$B = 0$	No
5	$\cdots$	Yes
6	$B = 100$	No
$\vdots$		

Independent

Contradictory

5. Generate a new regression



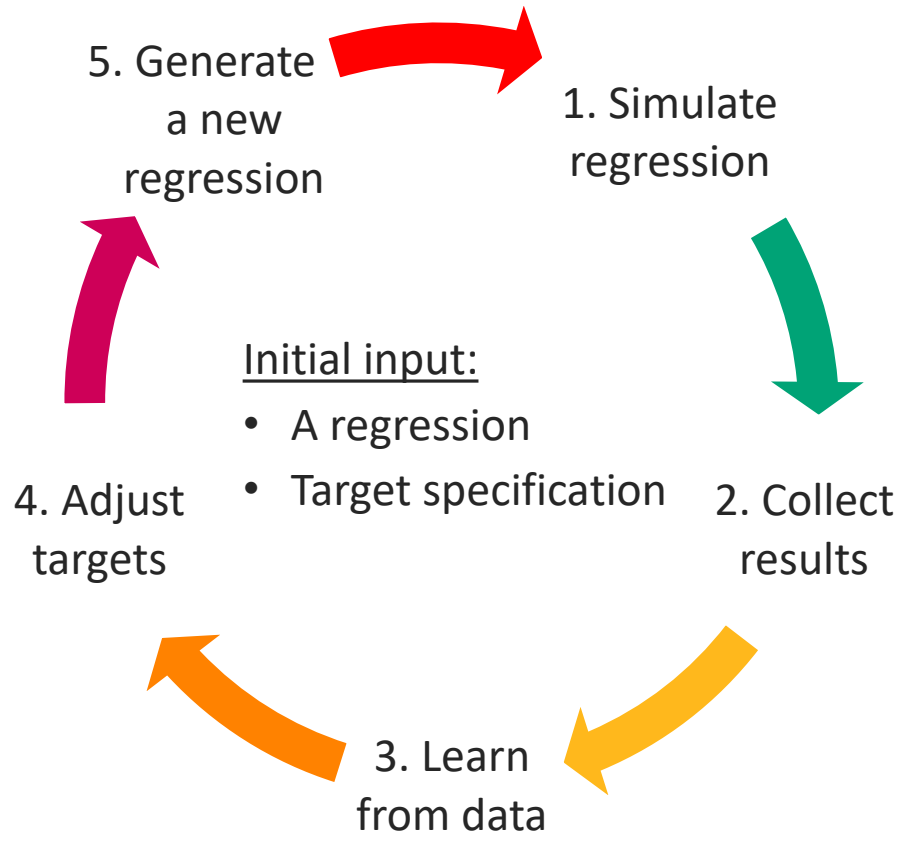
Steps 2 - 5: A feature of SimAI

Proposed Iterative Machine Learning Flow

- Iterate until all target scenarios satisfied

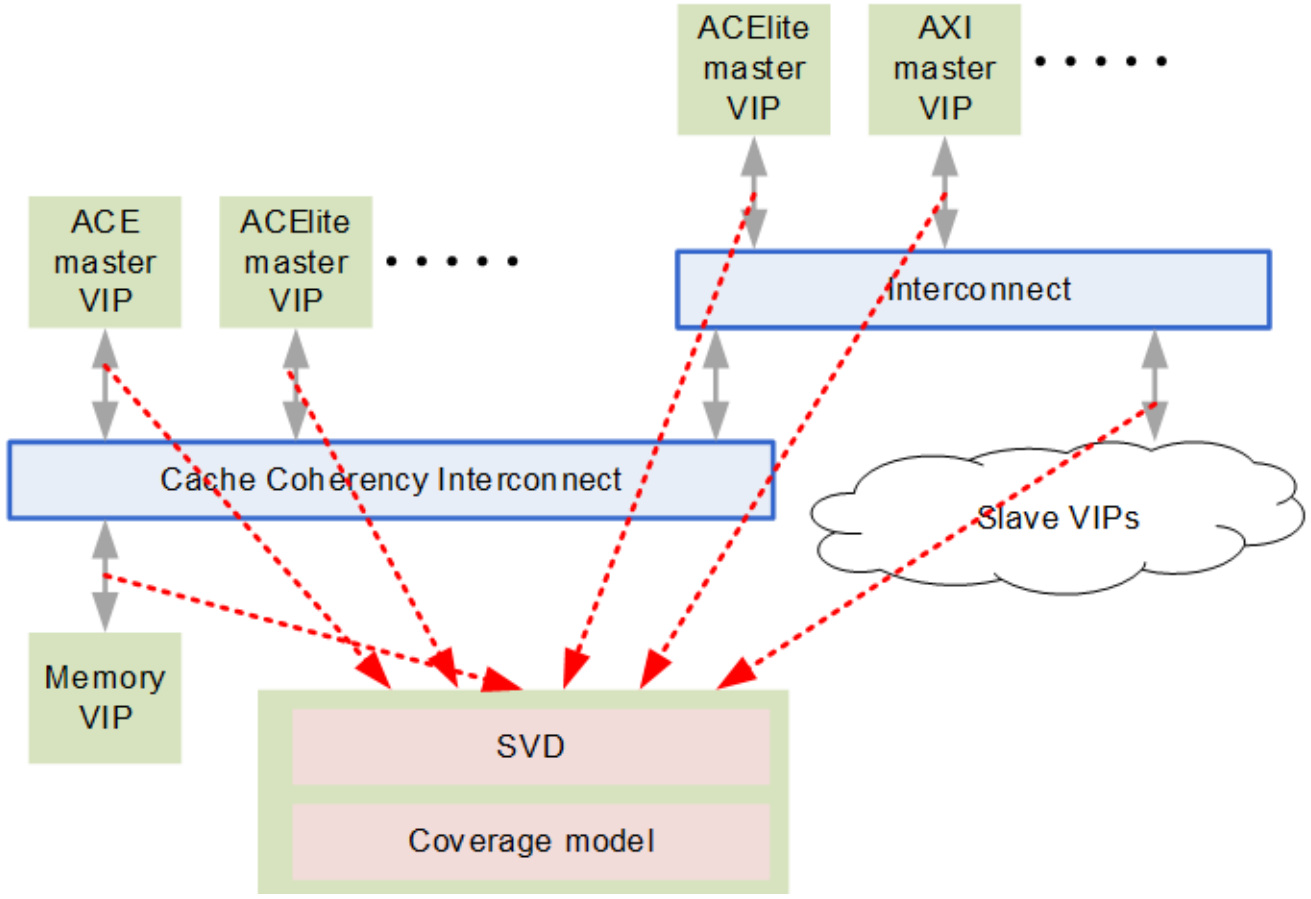
➡ Functional coverage closure

- Possibly address many target scenarios in a single simulation run
  - CPU time for the single run may increase
  - Total CPU time for coverage closure greatly ↓



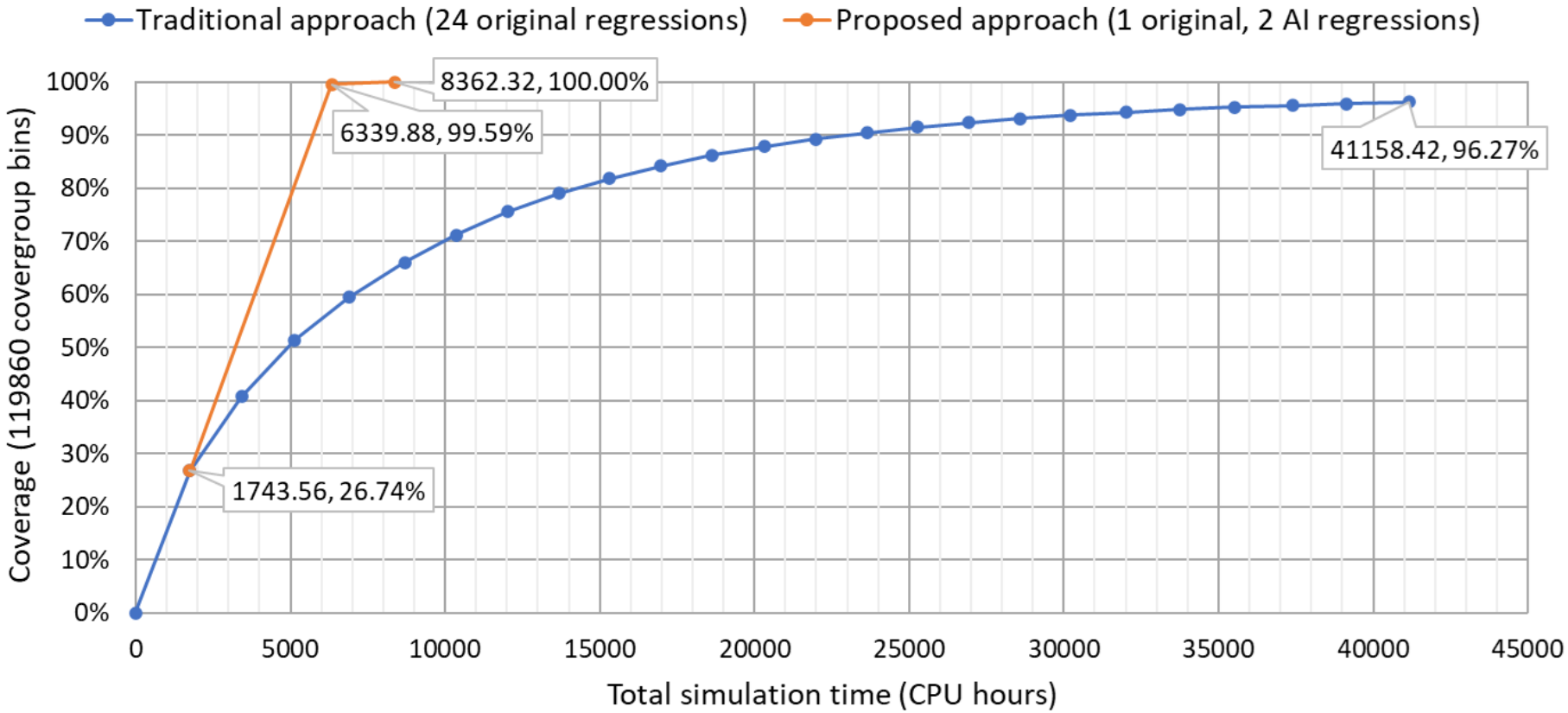
Production DV Project

- Cascade of interconnects
- Verification IPs (VIPs)
  - Active VIPs in early stage
  - Passive VIPs with DUTs later
- Scoreboard (SVD)
  - Checks end-to-end correctness
- Coverage model
  - Hundreds of thousands of coverage elements



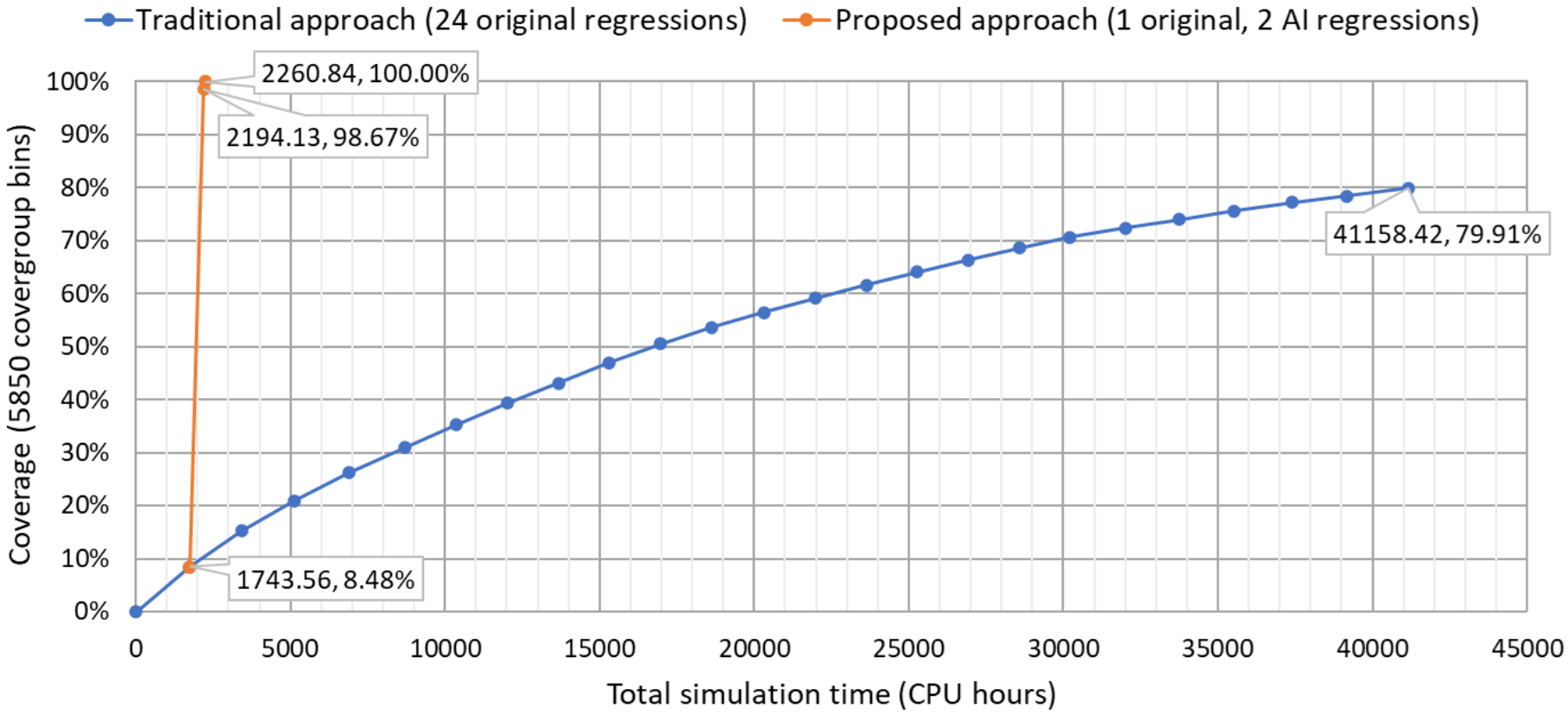
Production Project: Experiments 1

- Checks master and slave control signals w.r.t. reachability
- CPU time reduction 4.92x
- Coverage increase 3.73 %pt
- Extra effort for traditional approach to close this coverage



Production Project: Experiments 2

- Checks QoS values transmitted from masters
- CPU time reduction 18.20x
- Coverage increase 20.09 %pt
- Human engineering required for traditional method



Concluding Remarks

- Iteratively addressed remaining target scenarios to close coverage
- Closed challenging sets of coverage items in production project
- Significantly reduced CPU time, resources, human effort

- If target specification is incomplete, this approach may not be effective
- Future work includes deriving target specification automatically

Questions

- Thank you very much for your attention & interests!